DATA HANDBOOK

ICs for Telecom
Bipolar, MOS
Subscriber sets
Cordless telephones

BOOK IC03 1989

Philips Components

PHILIPS

ICs for Telecom
Bipolar, MOS

Subscriber sets
Cordless telephones

SELECTION GUIDE

FUNCTIONAL INDEX

NUMERICAL INDEX

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PCD3320D	dialler with several mute signals	DIL18; SOT133B	207
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PCD3321D	dialler with two automatic access pauses	DIL18; SOT133B	207
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PCD3347P	microcontroller with on-chip DTMF generator; 1.5K ROM; 64 x 8 RAM; 13 I/O lines; I^2C-bus	DIL20; SOT146	263
PCD3347T	microcontroller with on-chip DTMF generator; 1.5K ROM; 64 x 8 RAM; 13 I/O lines; I^2C-bus	SO20; SOT163A	263

FORTHCOMING NEW PRODUCTS

The types listed below are not included in this handbook. Information will be available at a later date.

PCD3315/513	CMOS redial and repertory dialler; 1.5K ROM; 160 x 8-bit RAM
PCD3344/002	microcontroller with on-chip DTMF generator
PCD3344/004	microcontroller with on-chip DTMF generator
PCD3348	microcontroller for telephone sets; 256 x 8-bit RAM; 8K ROM
PCD4413A	pulse and DTMF dialler
PCF8584	8-bit parallel-bus to I^2C-bus protocol converter

The PCD332X family of ICs comprises the following types:

PCD3320	dialler with several mute signals
PCD3321	dialler with two automatic access pauses
PCD3322	variant of PCD3320
PCD3323	dialler for sophisticated PABX applications
PCD3324	dialler with one automatic access pause
PCD3325A	dialler with manual access pause control
PCD3326	variant of PCD3321
PCD3327	variant of PCD3325A for ceramic resonator with automatic reset of access pause

functional survey		PCD							
		3320	3321	3322	3323	3324	3325A	3326	3327*
Number of pins		18	18	18	28	18	18	18	18
Dialling pulse frequency	10 Hz	●	●	●	●	●	●	●	●
selectable with F01, F02	16, 20 Hz		●		●	●	●	●	●
Mark/space ratio	3:2	●	●	●	●	●	●	●	●
selectable with M/S	2:1		●		●	●	●		●
Inter-digit pause duration	8 x T_{DP}	●	●	●	●	●	●	●	●
selectable with IDP	9 x T_{DP}				●				
Reset delay for line power breaks	1,6 x T_{DP}	●	●	●	●	●	●	●	●
selectable with RDS	3,2 x T_{DP}				●				
Access pauses repeated during redial			●		●	●	●	●	●
Manual insertion of access pauses			●		●	●	●	●	●
Automatic access pause insertion	1 max.					●			
	2 max.		●		●			●	
Access pause duration	32 x T_{DP}		●		●	●		●	
selectable with APD	64 x T_{DP}				●			●	
not automatically terminated							●		●
$\overline{M1}$, inverted mute output		●		●	●				
M2, strobe output				●	●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs		●			●				
CL, clock output					●				
APO, access pause output					●				
HOLD, dialling-interrupt input		●		●	●				
APO + HOLD, internally connected			●			●	●	●	●
APR, access pause reset input					●				
AAE, automatic access pause enable					●				

T_{DP} = dialling pulse period.

* PCD3327 for ceramic resonator

Features common to all PCD332X family

OSC IN, OSC OUT } on-chip oscillator input and output

COL1 to COL3, column keyboard inputs with on-chip pull down

ROW1 to ROW4, row keyboard inputs with on-chip pull-up

CE, chip enable input

DP, dialling pulse drive output to external line-switching transistor or relay

M1, mute output

COMPARISON OF TRANSMISSION ICs

	60	61	64	66T	67	68
Microphones						
low sensitivity dynamic or magnetic	*			*		*
medium sensitivity magnetic or dynamic	*		*	*	*	*
electret with preamplifier		*	*	*	*	*
piezo electric		*	*	*	*	*
very accurate microphone matching			*		*	*
dynamic limiter			*			
Receivers						
dynamic or magnetic or piezo (17-39 dB)	*	*		*		*
dynamic or magnetic or piezo (20-45 dB)			*		*	
Power-down input	*	*	*	*	*	*
DTMF and mute inputs	*	*	*	*	*	*
Voltage regulator						
adjustable DC voltage/resistance	*	*	*	*	*	*
parallel operation			*		*	
Peripheral supply						
unregulated - limited power	*	*		*	*	*
unregulated - extended power			*			
stabilized - extended power			*			
Automatic line loss compensation AGC	*	*	*	*	*	*

CMOS MICROCONTROLLERS FOR TELEPHONE SETS

Type	ROM (bytes)	RAM (bytes)	I^2C-bus	Pre-programmed version	Customized versions
PCF84C00	–	256	Yes		
PCF84C21	2 K	64	Yes		
PCF84C41	4 K	128	Yes		
PCF84C81	8 K	256	Yes		
PCD3343	3 K	224	Yes	PCD3341	PCD3343/0XX
PCF3346	4 K	128 256	Yes (2)		
PCD3315C	1.5 K	160	No	PCD3315/503	PCD3315/5XX
PCF3344	2 K	224	No (1)	PCD3344/004	PCD3344/0XX
PCF3347 (3)	1.5 K	64	No (1)		
PCF3349 (4)	4 K	224	No (1)		

(1) Includes DTMF generator
(2) Includes 256 x 8 EEPROM planned for mid-1988
(3) Development samples planned for mid-1988
(4) Development samples planned for QIV-1988.

GENERAL

Product status definitions

for type numbers with prefixes MC, NE, SA, SE

Ordering information

for type numbers with prefixes MC, NE, SA, SE

Type designation

for type numbers with prefixes PCD, PCF, TDA, TEA

Rating systems

for type numbers with prefixes PCD, PCF, TDA, TEA

Handling MOS devices

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
- $1000 per order
- $250 per line item per order

Military Product:
- $250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (– 55°C to + 125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5537N	LF398	LIN	Sample & Hold Amp

- NE5537N: Package Descriptions—See Table 2; Device Number; Device Family and Temperature Range Prefix—See Tables 3 & 4
- LF398: Description of Product Function
- LIN: Product Family — LIN Analog Products; MIL Military Products

Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to + 70°C
S	– 55° to + 125°C
NE	0° to + 70°C
SE	– 55° to + 125°C
SA	– 40° to + 85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line
W : Lead chip-carrier (LCC)
X : Leadless chip-carrier (LLCC)
Y : Pin grid array (PGA)

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

MC3361
Low Power FM IF

Objective Specification

Linear Products

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SOL (surface-mounted miniature package).

FEATURES

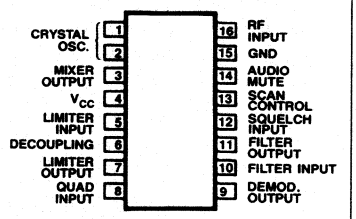
- **2.0V to 8.0V operation**
- **Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}**
- **Excellent sensitivity: 2.0μV for −3dB limiting typ**
- **Low external parts count**
- **Operation to 60MHz**

APPLICATIONS

- **Cordless telephone**
- **Narrow band receivers**
- **Remote control**

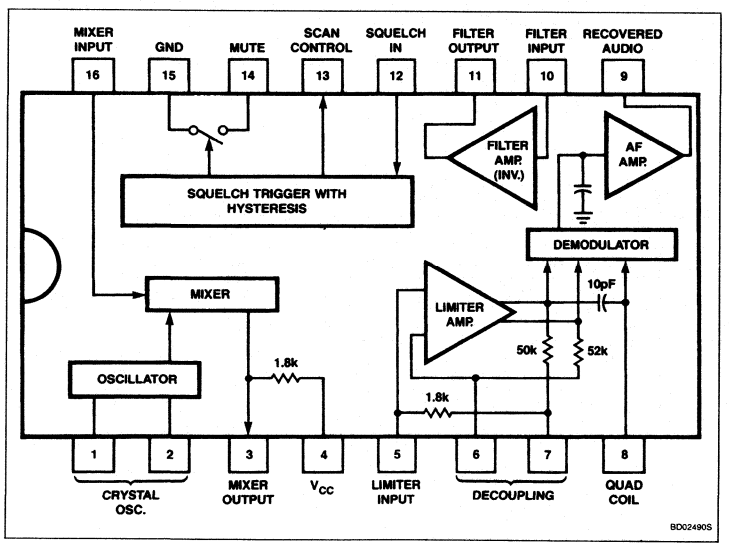
PIN CONFIGURATION

D[1] and N Package



NOTE:
1. Available in 16-pin SOL package.

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40 to +85°C	MC3361N
16-Pin Plastic; SOL	−40 to +85°C	MC3361D

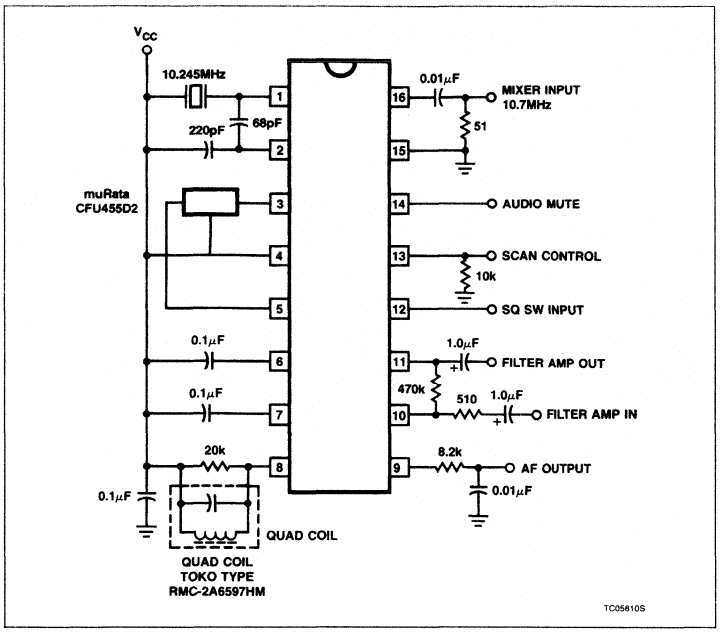
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	−0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature range		−40 to +85	°C
T_{STG}	Storage temperature range		−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = ±3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.)

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off squelch on	4			 4.2 5.4	 7.0 9.0	mA
Input limiting voltage	16	−3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	V_{IN} = 10mV_{RMS}	100	150	270	mV_{RMS}
Filter gain (10kHz)		V_{IN} = 1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13	V_{12} = 1.0V_{DC}			0.5	V_{DC}
Scan function high (mute on)	13	V_{12} = GND	3.5			V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



NE/SE567
Tone Decoder/Phase-Locked Loop

Product Specification

Linear Products

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

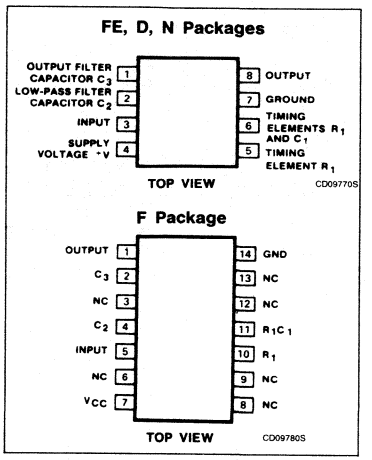
FEATURES

- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14%)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20–to-1 range with an external resistor**
- **Military processing available**

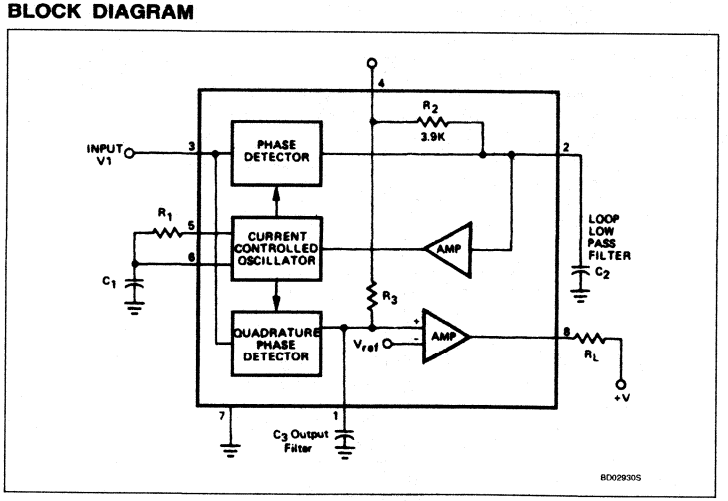
APPLICATIONS

- **Touch-Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

PIN CONFIGURATIONS



BLOCK DIAGRAM



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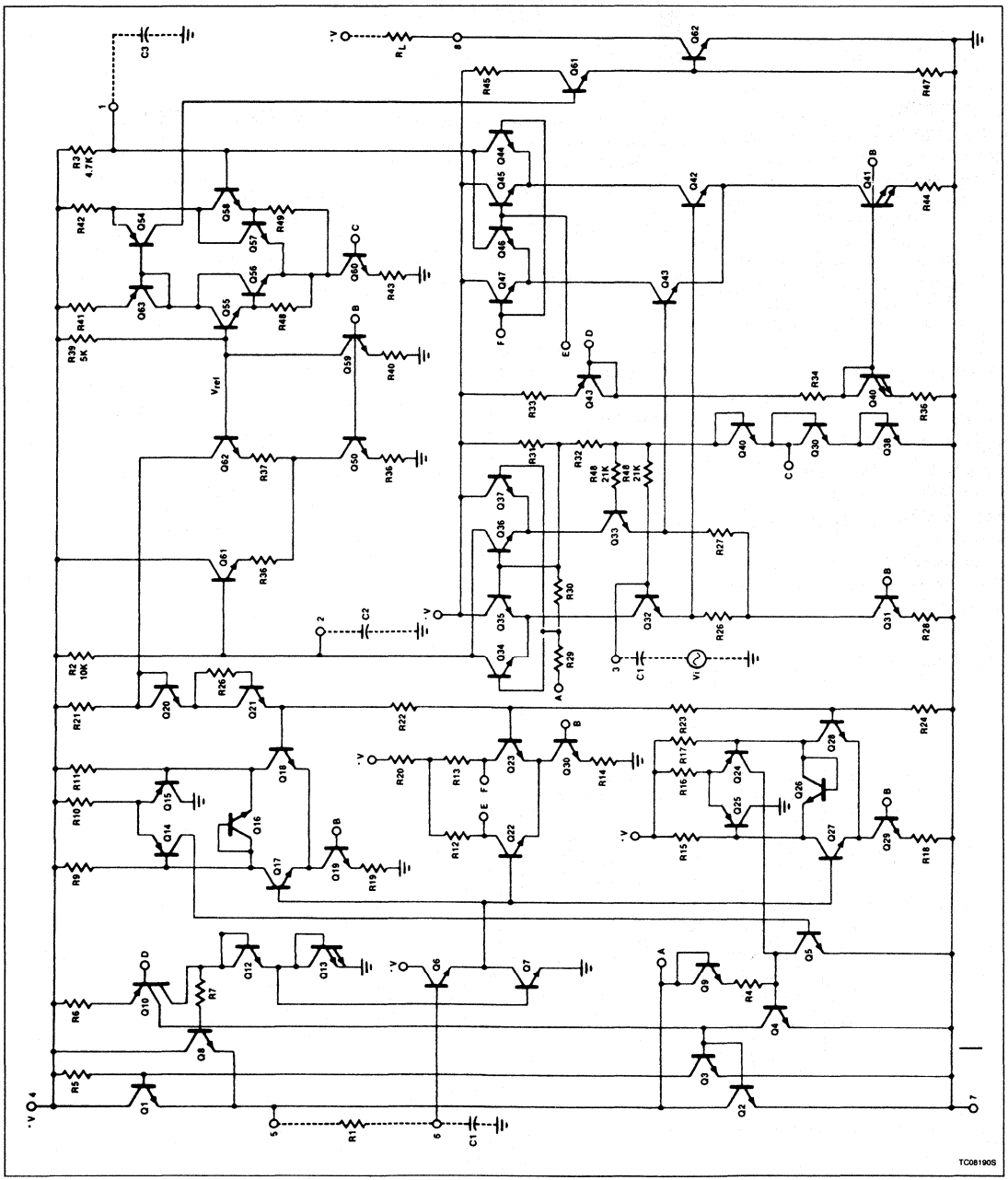
EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE567D
14-Pin Cerdip	0 to +70°C	NE567F
8-Pin Cerdip	0 to +70°C	NE567FE
8-Pin Plastic DIP	0 to +70°C	NE567N
14-Pin Cerdip	−55°C to +125°C	SE567F
8-Pin Cerdip	−55°C to +125°C	SE567FE
8-Pin Plastic DIP	−55°C to +125°C	SE567N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature NE567 SE567	 0 to +70 −55 to +125	 °C °C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 + V_S	V
V−	Negative voltage at input	−10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	300	mW

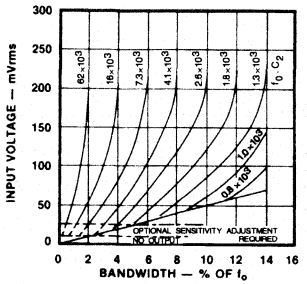
DC ELECTRICAL CHARACTERISTICS V+ = 5.0V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	−55 to +125°C 0 to +70°C		35 ±140 35 ±60			35 ±140 35 ±60		ppm/°C ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	−10	0	+10	−10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth — variation with temperature	$V_I = 300mV_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detectionbandwidth — variation with supply voltage	$V_I = 300mV_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L = 100mA, $f_I = f_O$		20	25		20	25	mV_{RMS}
	Largest no-output input voltage[4]	I_L = 100mA, $f_I = f_O$	10	15		10	15		mV_{RMS}
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n = 140kHz		−6			−6		dB
Output									
	Fastest on-off cycling rate			$f_O/20$			$f_O/20$		
	"1" output leakage current	V_8 = 15V		0.01	25		0.01	25	μA
	"0" output voltage	I_L = 30mA I_L = 100mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V V
t_F	Output fall time[3]	R_L = 50Ω		30			30		ns
t_R	Output rise time[3]	R_L = 50Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current — activated	R_L = 20kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:
1. Frequency determining resistor R_1 should be between 2 and 20kΩ.
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2 = 130kΩ from Pin 1 to V+. See Figure 1.

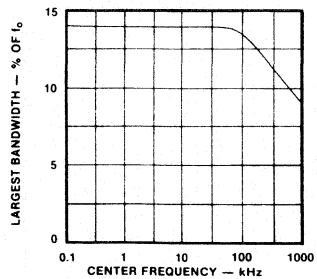
TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Input Signal Amplitude



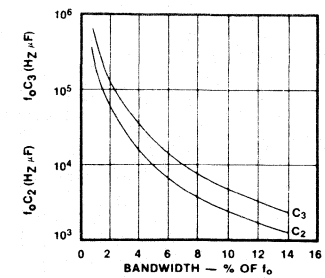
OP04280S

Largest Detection Bandwidth vs Operating Frequency



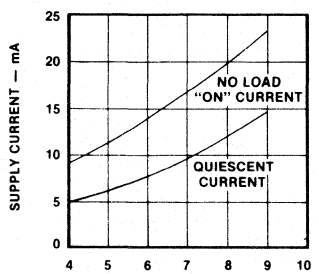
OP04290S

Detection Bandwidth as a Function of C_2 and C_3



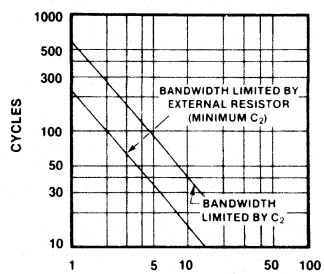
OP04300S

Typical Supply Current vs Supply Voltage



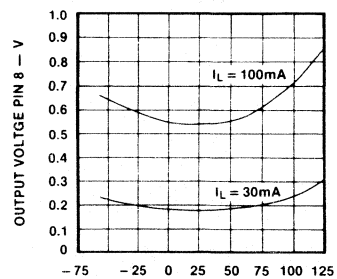
OP04310S

Greatest Number of Cycles Before Output

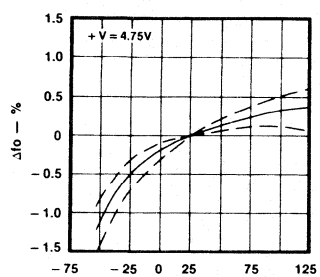


OP04320S

Typical Output Voltage vs Temperature

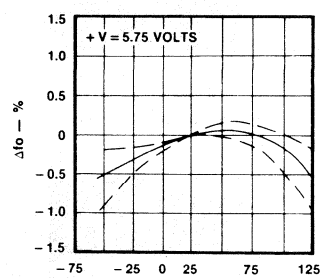


Typical Frequency Drift With Temperature (Mean and SD)



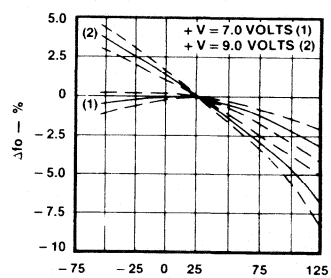
OP04340S

Typical Frequency Drift With Temperature (Mean and SD)



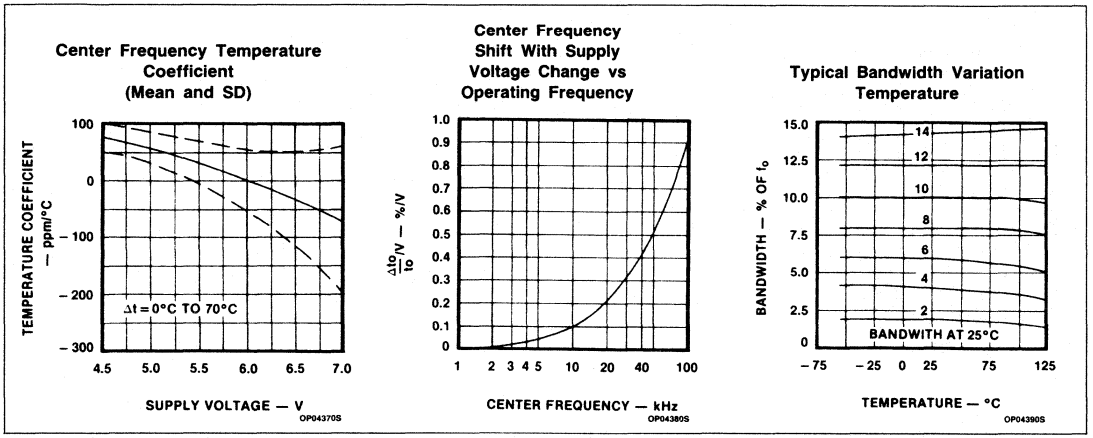
OP04350S

Typical Frequency Drift With Temperature (Mean and SD)



OP04360S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



DESIGN FORMULAS

$$f_O \cong \frac{1}{1.1R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_I}{f_OC_2}} \text{ in \% of } f_O,$$

$$V_I \leqslant 200mV_{RMS}$$

Where

V_I = Input voltage (V_{RMS})

C_2 = Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

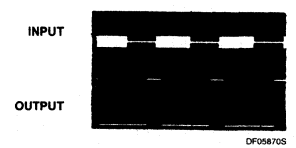
A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

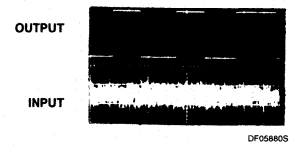
1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

TYPICAL RESPONSE



NOTE:
$R_L = 100\Omega$

Response to $100mV_{RMS}$ Tone Burst



NOTES:
S/N = –6dB
$R_L = 100\Omega$
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of f_OC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constand bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_OC_2 product (f_O (Hz), $C_2(\mu F)$).
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the

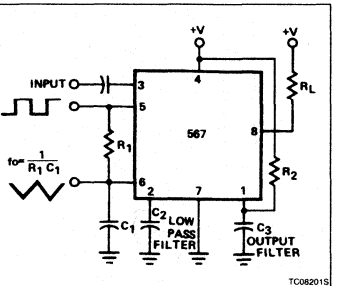


Figure 1

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R_2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \approx (+V - 1.4V)$ having a DC average of $+V/2$. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of $+V/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

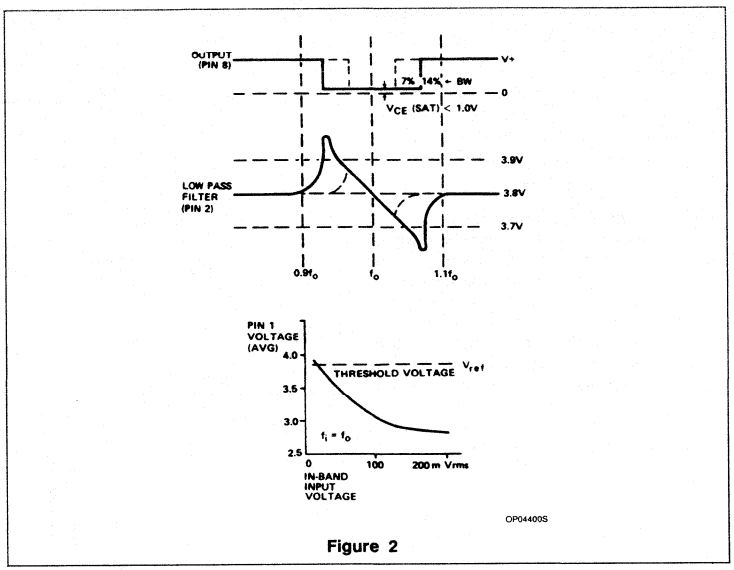


Figure 2

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n + 1)$ f_O, and will give an output for signals near $(4n + 1)$ f_O where $n = 0, 1, 2$, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can

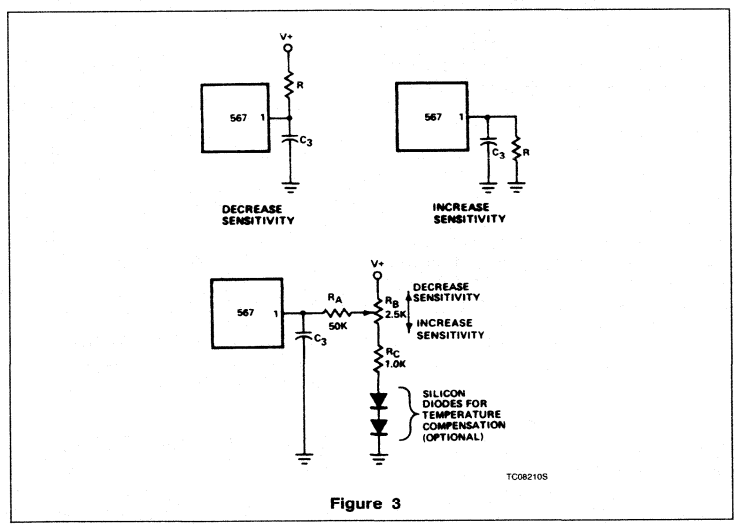


Figure 3

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O}\mu F$$

$$C_3 = \frac{260}{f_O}\mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

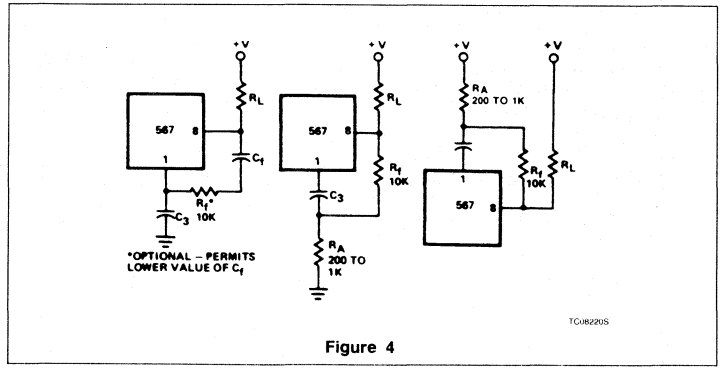


Figure 4

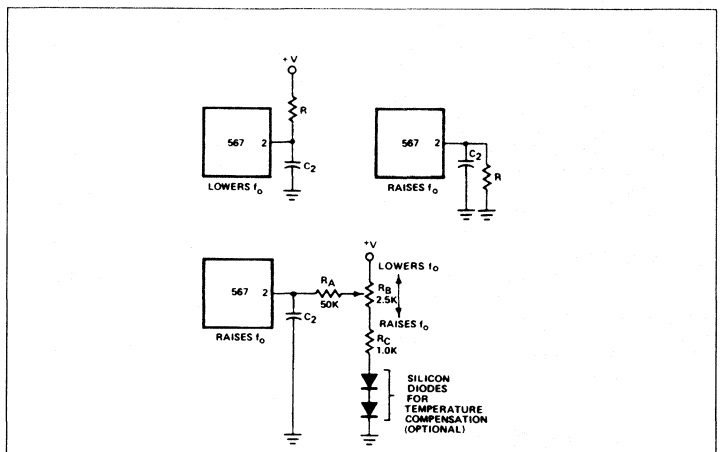


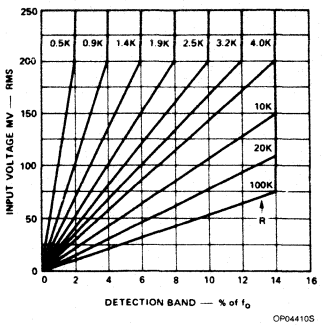
Figure 5

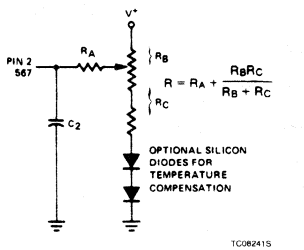
SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.





NOTE:

$$\frac{130}{f_O}\left(\frac{10k+R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k+R}{R}\right)$$

Adjust control for symmetry of detection band edges about f_O.

Figure 6

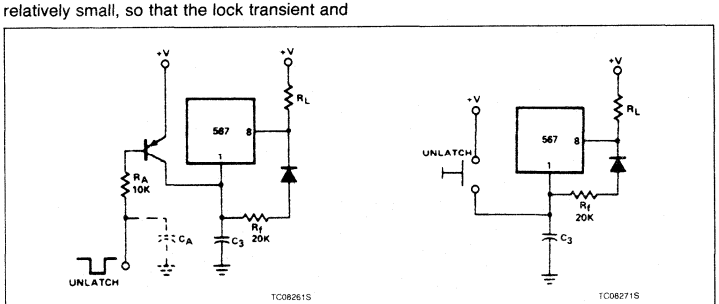
CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.



NOTE:
C_A prevents latch-up when power supply is turned on.

Figure 7. Output Latching

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C1 VALUE

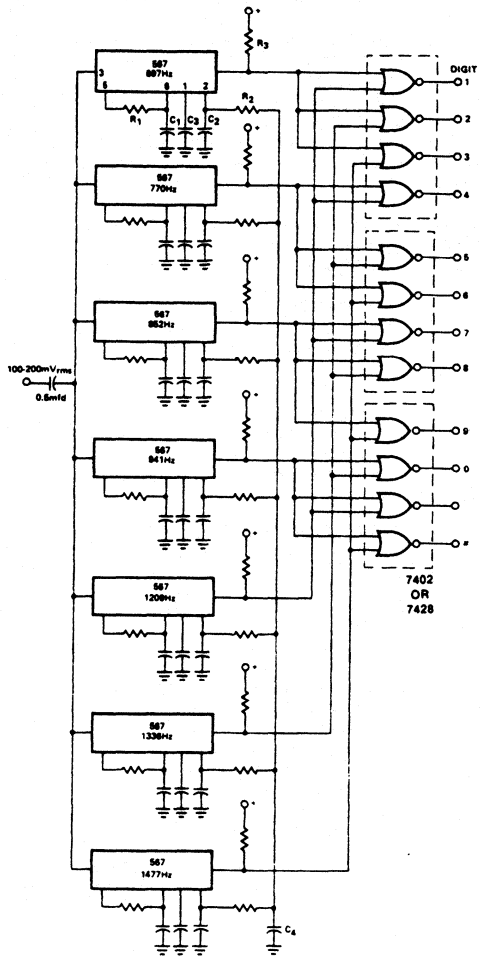
(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.

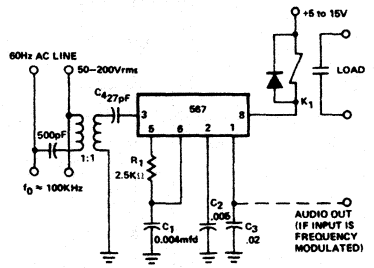
TYPICAL APPLICATIONS



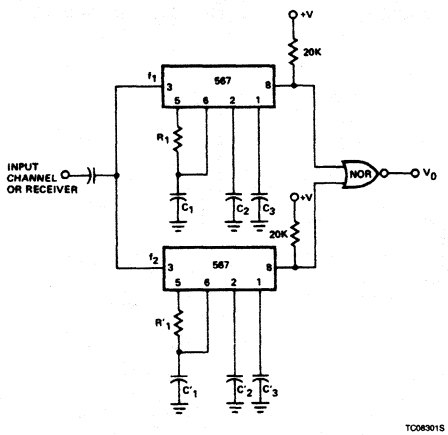
Touch-Tone® Decoder

NOTES:
Component values (Typical)
R_1 = 26.8 to 15kΩ
R_2 = 24.7kΩ
R_3 = 20kΩ
C_1 = 0.10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250μF 6V

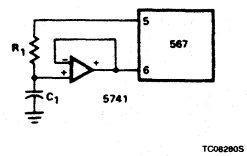
TYPICAL APPLICATIONS (Continued)



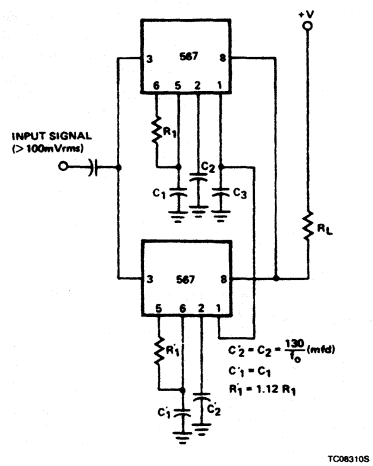
Carrier-Current Remote Control or Intercom



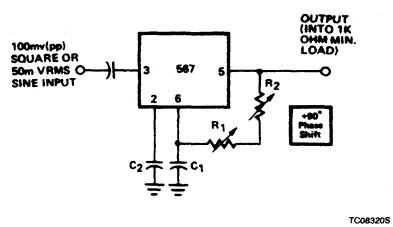
Dual-Tone Decoder



Precision VLF



24% Bandwidth Tone Decoder

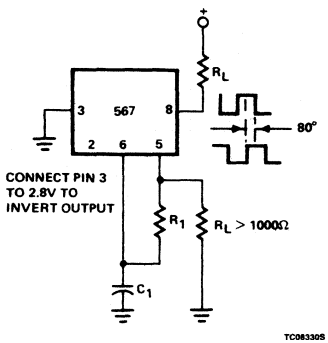


NOTES
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

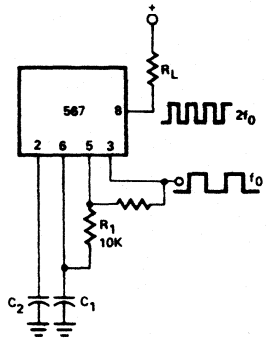
0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

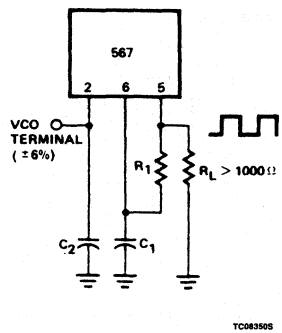
TYPICAL APPLICATIONS (Continued)



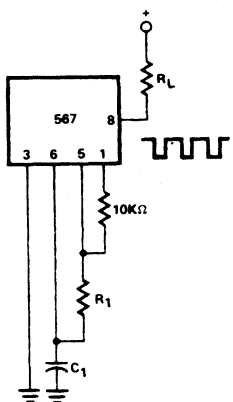
Oscillator With Quadrature Output



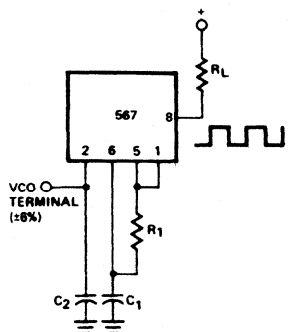
Oscillator With Double Frequency Output



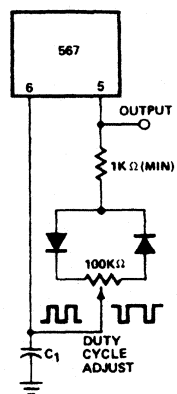
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator

NE575
Low Voltage Compandor

Preliminary Specification

Linear Products

DESCRIPTION

The NE575 is a dual gain-control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

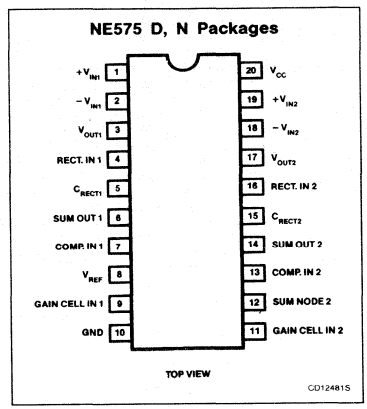
FEATURES

- **Operating voltage range from 3 to 7V**
- **Reference voltage of 100mV$_{RMS}$ = 0dB**
- **One dedicated summing op amp per channel and two extra uncommitted op amps**
- **600Ω drive capability**
- **Single or split supply operation**
- **Wide input/output swing capability.**

APPLICATIONS

- **Portable communications**
- **Cellular radio**
- **Cordless telephone**
- **Consumer audio**
- **Portable broadcast mixers**
- **Wireless microphones**
- **Modems**
- **Electric organs**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE575N
20-Pin Plastic SO	0 to +70°C	NE575D

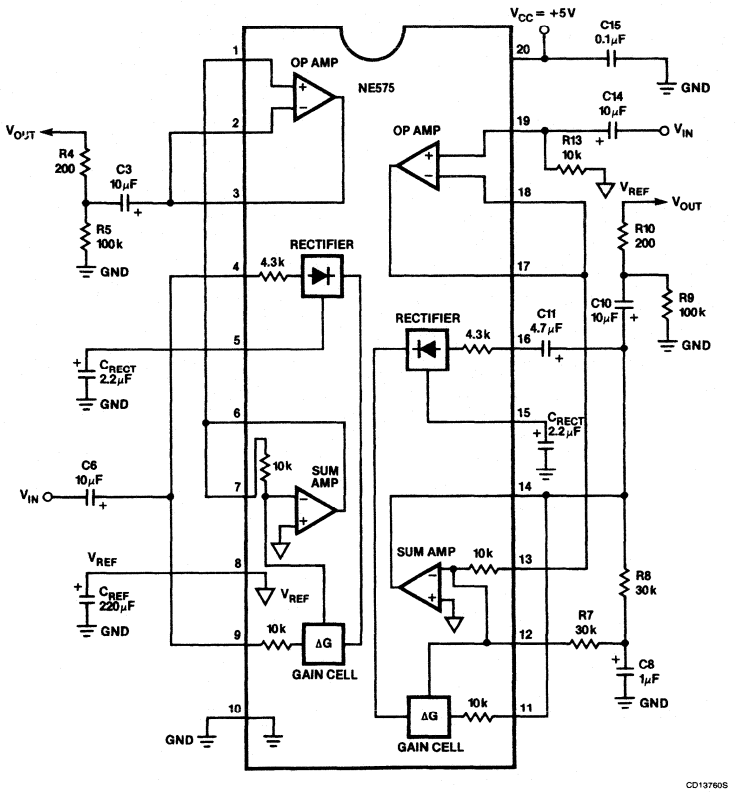
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	8	V
T_A	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, 0dB = 100mV, expander mode, $V_{CC} = 5V$, Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
For compandor, including summing amplifier						
V_{CC}	Supply voltage[1]		3	5	7	V
I_{CC}	Supply current	No signal	3	4	5.5	mA
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.13	1.0	%
eno	Output voltage noise	BW = 20kHz, $R_S = 0Ω$		6	20	μV
0dB	Unity gain level	1kHz	−1.0		1.0	dB
V_{OS}	Output voltage offset	no signal	−100		100	mV
	Output DC shift	no signal to 0dB	−50	10	50	mV
	Tracking error	1kHz, +6dB to −30dB	−0.5		+0.5	dB
	Crosstalk	1kHz, 0dB, $C_{REF} = 220μF$		−80	−65	dB
For operational amplifier						
V_O	Output swing	V_{P-P}, $R_L = 10kΩ$	$V_{CC}-0.4$	$V_{CC}-0.2$		V
R_L	Output load	1kHz	600			Ω
CMR	Input common-mode range		0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		dB
I_B	Input bias current	$V_{IN} = 0.5V - 4.5V$	−0.3		0.3	μA
V_{OS}	Input offset voltage		−10	3	10	mV
A_{VOL}	Open-loop gain	$R_L = 10kΩ$	80	90		dB
SR	Slew rate	unity gain		1		V/μs
GBW	Bandwidth	unity gain		3		MHz
eni	Input voltage noise	BW = 20kHz		2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60		dB

NOTE:
1. The IC remains functional down to 2V.



NOTE:
Left channel in expander mode; right channel in compressor mode.
For additional information, call the factory.

Figure 1. Typical Application

NE612
Double-Balanced Mixer and Oscillator

Product Specification

Linear Products

DESCRIPTION

The NE612 is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

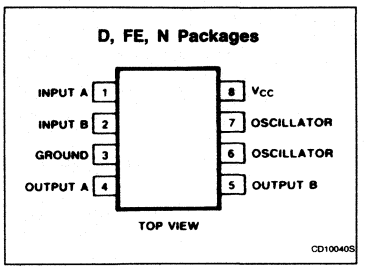
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

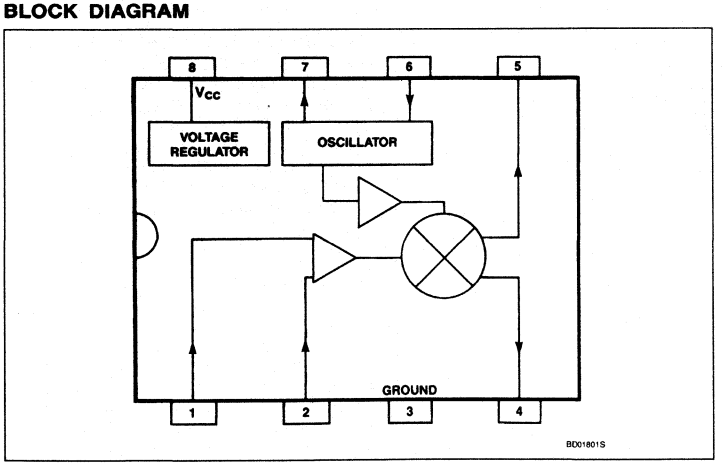
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LANs**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612N
8-Pin Plastic SO	0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 49MHz			5.0		dB
	Third-order intercept point at 49MHz	RF_{IN} = −45dBm		−15		dBm
	Conversion gain at 49MHz		14			dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

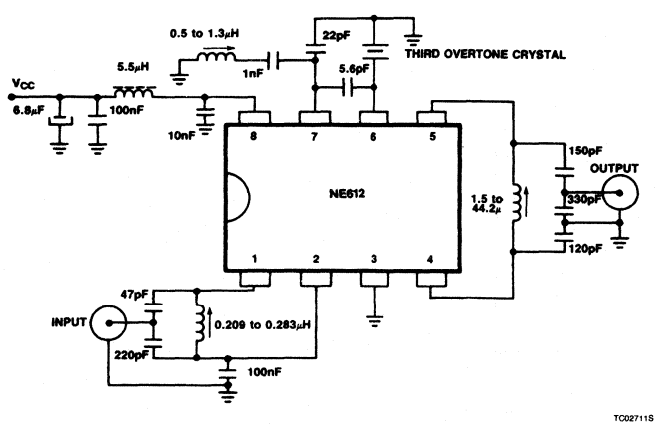


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ‖ 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless telephones. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

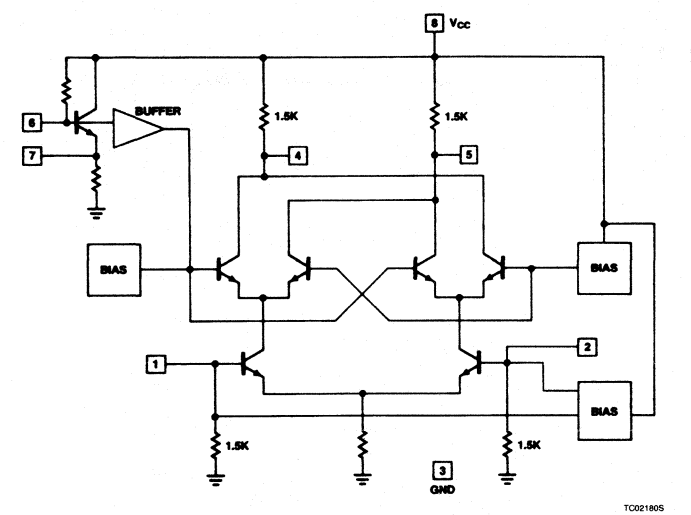
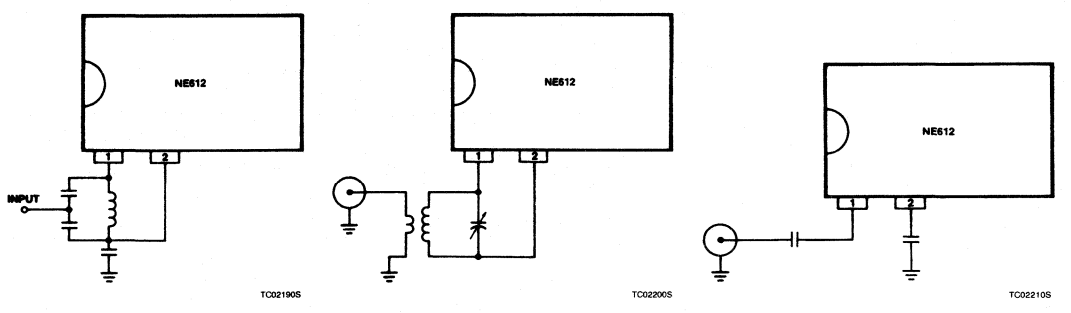


Figure 2. Equivalent Circuit

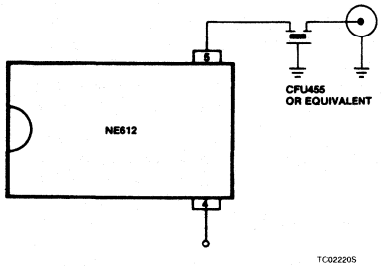


a. Single-Ended Tuned Input

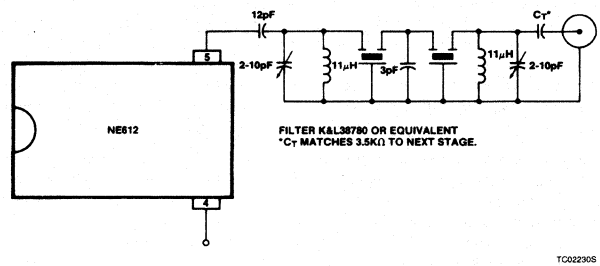
b. Balanced Input (For Attenuation Of Second Order Products)

c. Single-Ended Untuned Input

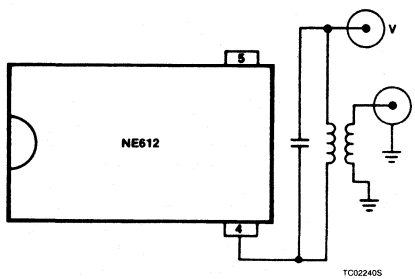
Figure 3. Input Configuration



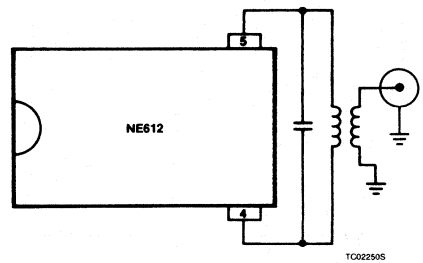
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

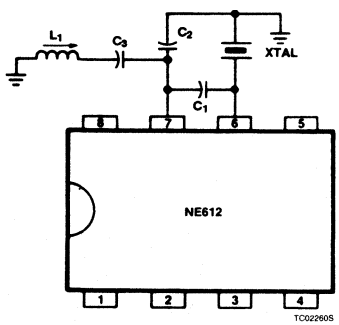


c. Single-Ended IFT

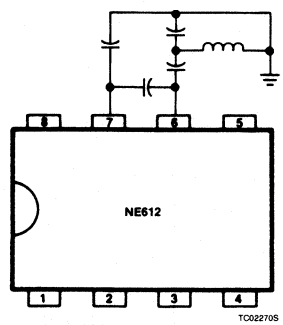


d. Balanced Output

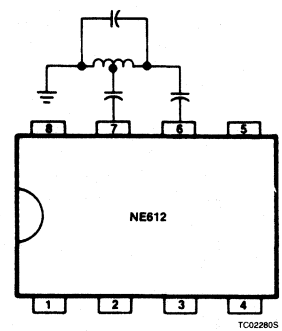
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

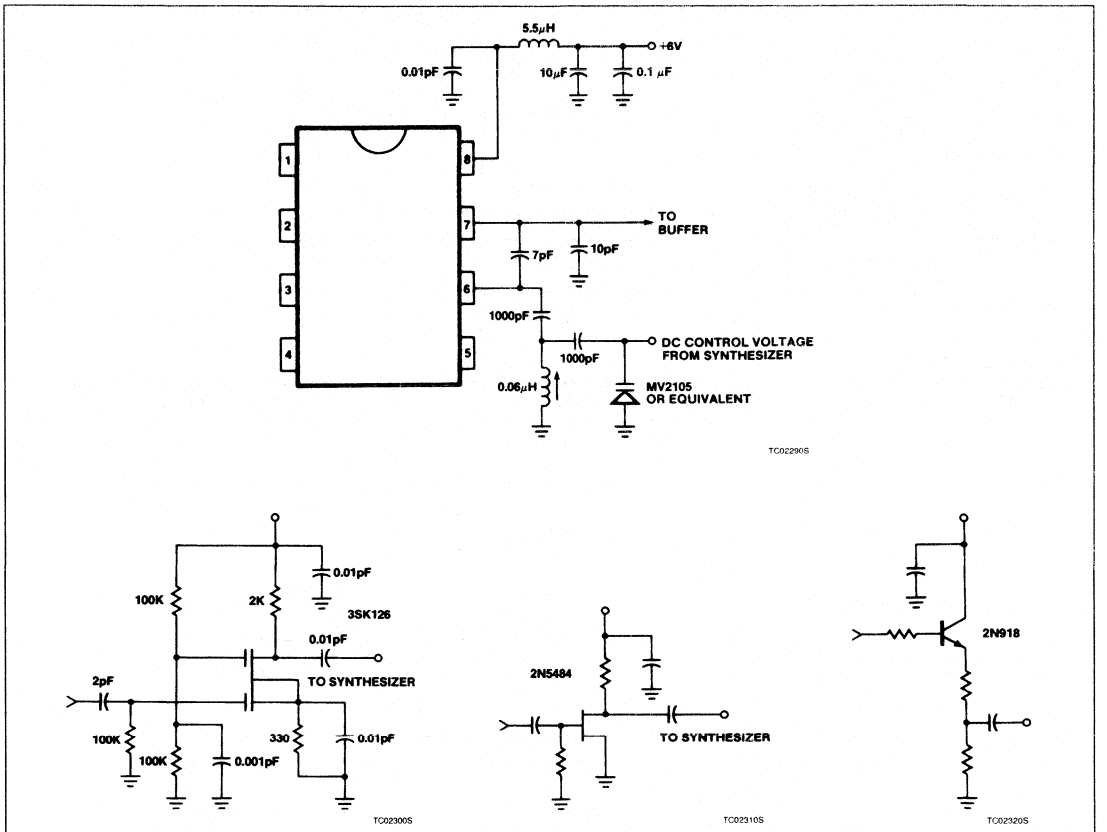


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

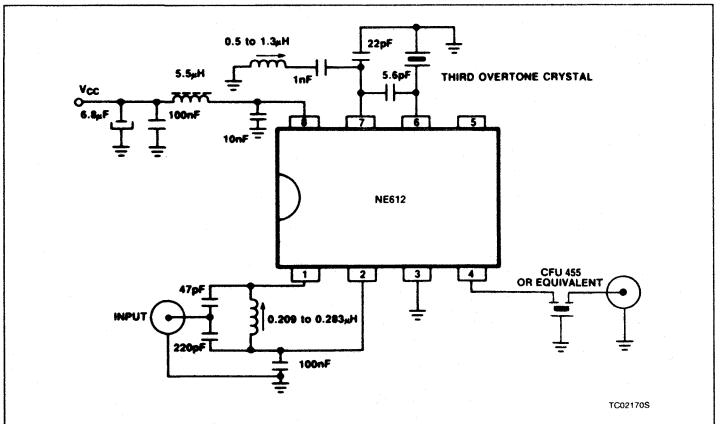


Figure 7. Typical Application for 46/49MHz Cordless Telephone

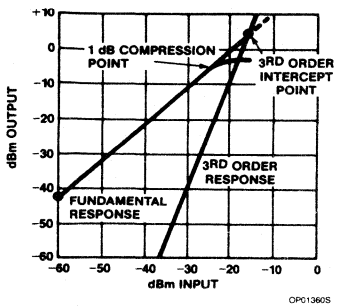


Figure 8. NE612 Third-Order Intermod And 1dB Compression Point Performance

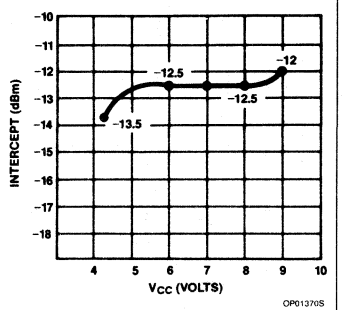


Figure 9. Input Third-Order Intercept Point vs V_{CC}

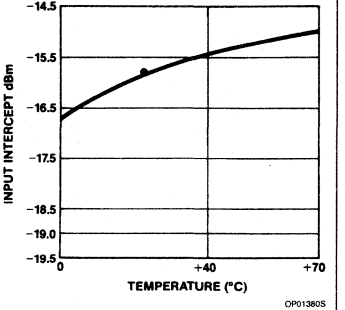


Figure 10. Third-Order Intercept Point vs Temperature

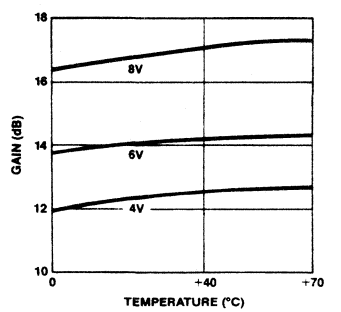


Figure 11

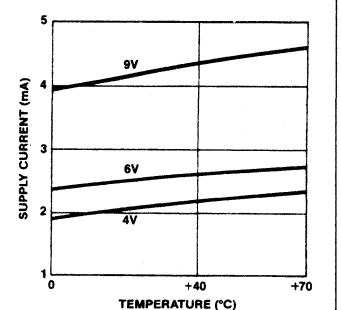


Figure 12

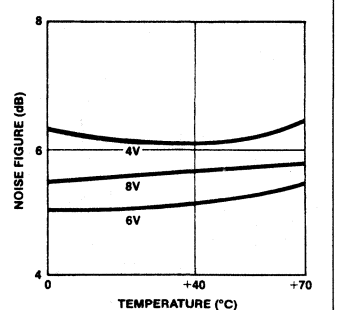


Figure 13

NE614
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE614 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual in-line plastic package and 16-lead SO (surface-mounted miniature package).

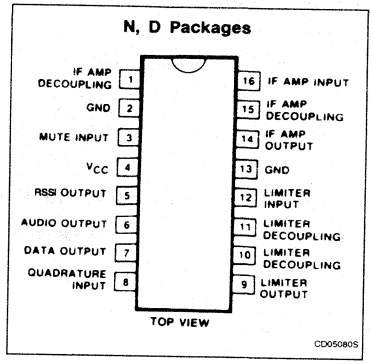
FEATURES

- **Low power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

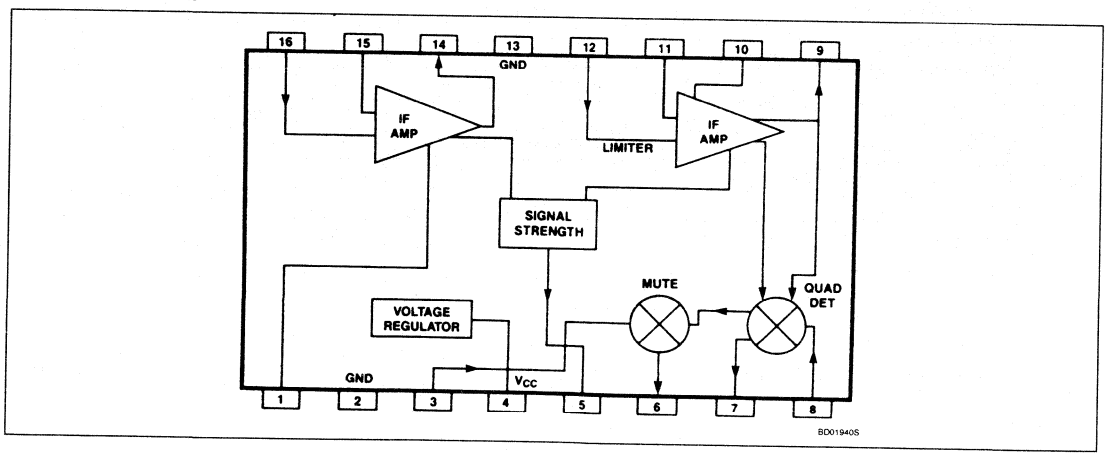
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614N
16-Pin Plastic SO	0 to +70°C	NE614D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE614	0 to +70	°C

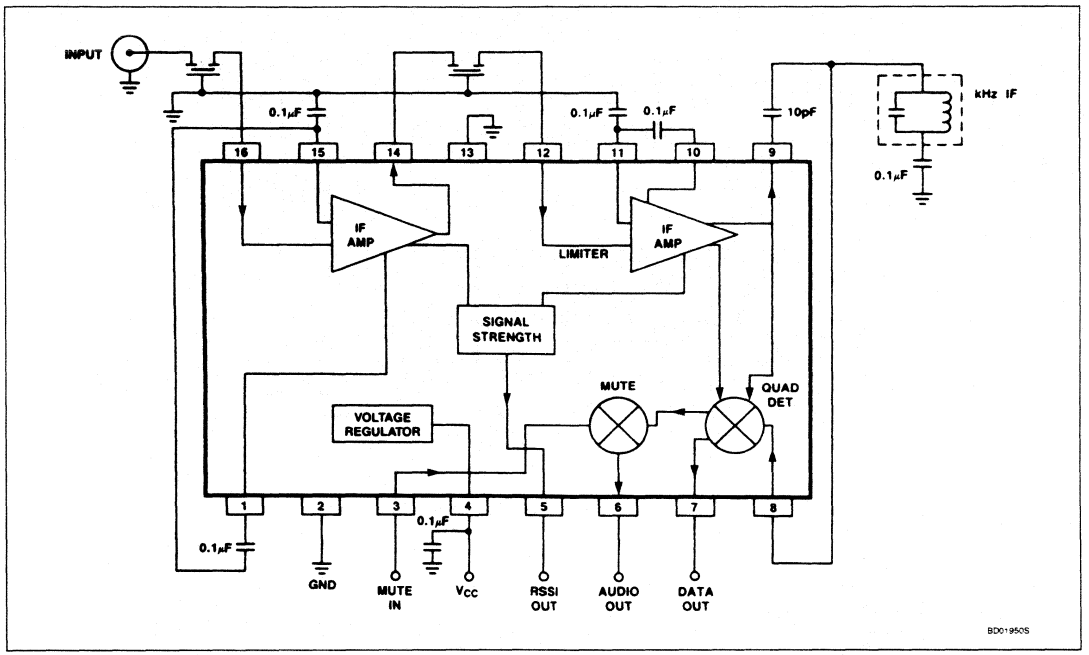
DC ELECTRICAL CHARACTERISTICS T_A = 25°C; V_{CC} = +6V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain				3.0	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	 V V

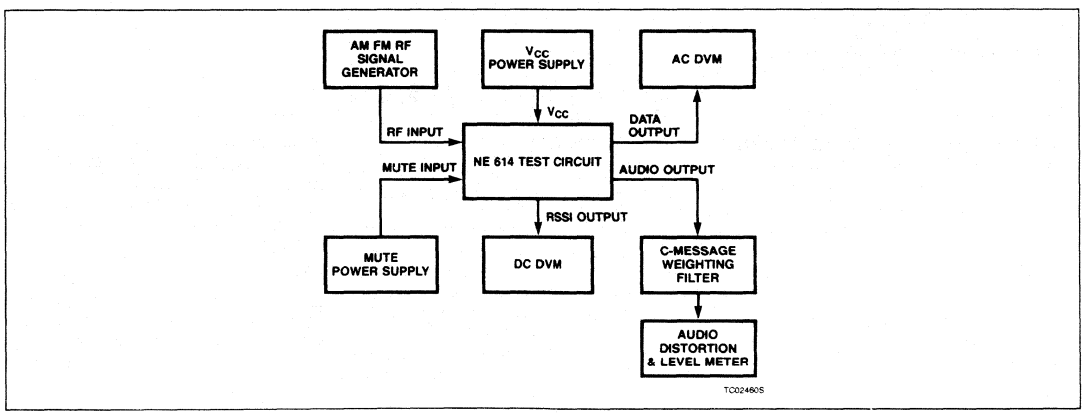
AC ELECTRICAL CHARACTERISTICS T_A = 25°C; V_{CC} = +6V, unless otherwise specified. RF frequency = 455kHz; RF level = −47dBm; FM modulation = 1kHz with +8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

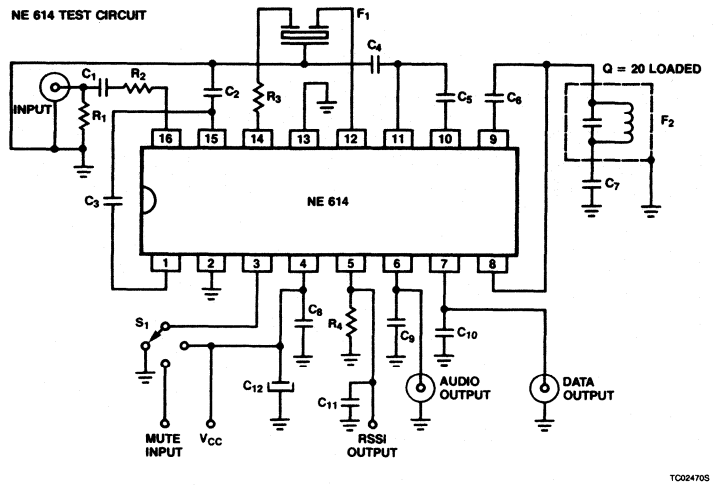
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input limiting − 3dB	Test at pin 16		−90	−80	dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level − 97dBm	8	12		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation		75		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance		50			kΩ
	Muted audio output impedance			50		kΩ

TYPICAL APPLICATION



TEST SETUP





NOTES:
C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8μF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film

Figure 1. NE614 Test Circuit and Parts List

DESCRIPTION OF OPERATION

The NE614 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low power systems objectives. Internal temperature compensated bias regulation completes the circuitry.

Figure 2 shows the equivalent circuits of the NE614.

Limiting Amplifiers

The NE614 has two independent limiting IF amplifiers. The first has a typical gain of 30dB. The second typically has 60dB gain. Both have 1.5k nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1k output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wide-band noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed-loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

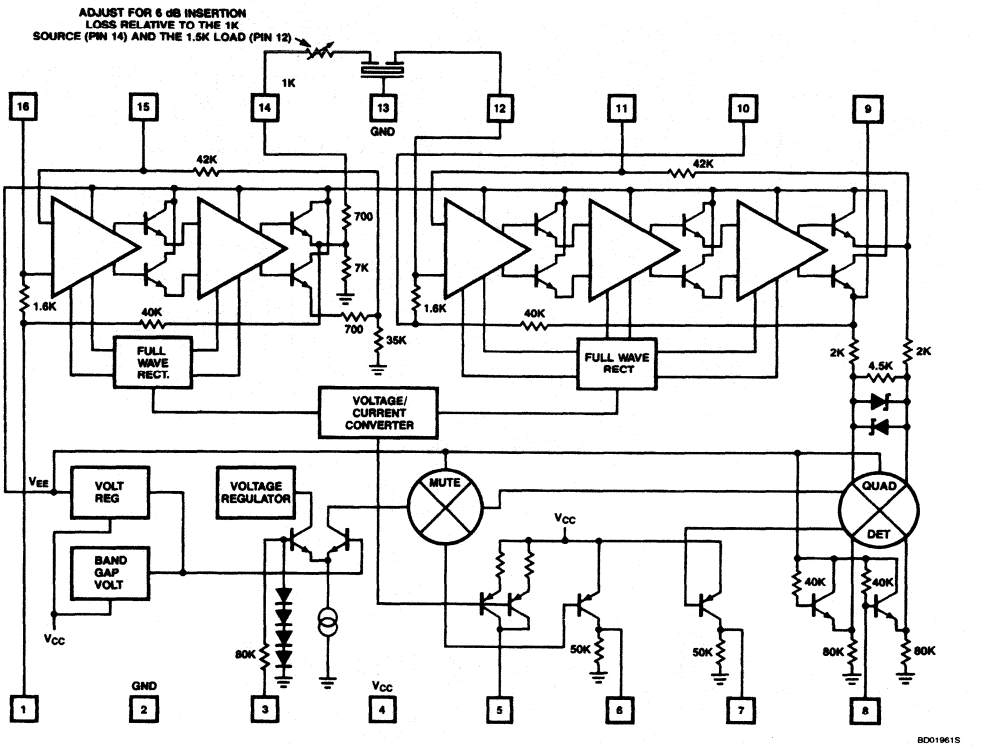


Figure 2. Equivalent Circuit

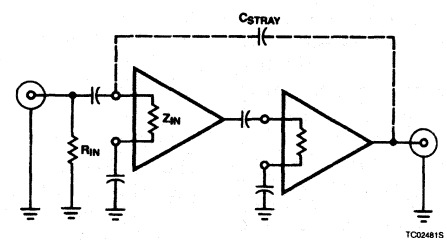
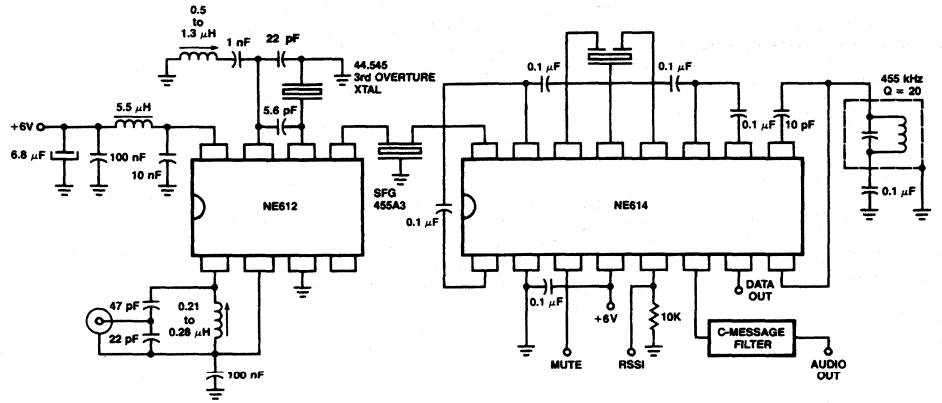


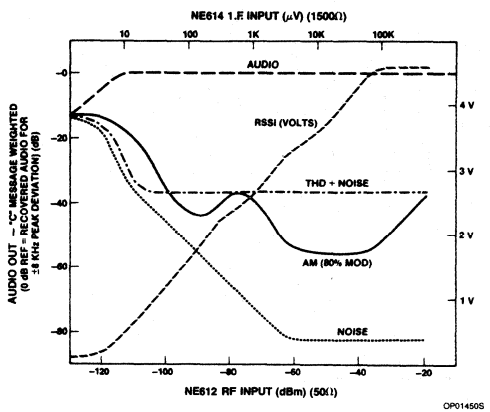
Figure 3. Considerations for Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5k. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.



a. NE614 Application Circuit



b. Typical Application Circuit Performance

Figure 4

Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used. Figure 4a indicates a 455kHz circuit configuration which should serve as a reasonable starting point for many applications. This circuit is configured for 46/49MHz cordless telephone.

Quadrature Detector

The detector of the NE614 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4b indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and and capacitively to Pin 9. Because of the DC bias of the NE614, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

Table 1. System Parameters as Applied to Figure 4a

$\Delta\omega$	=	2π*8kHz
ω_0	=	2π*455kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20

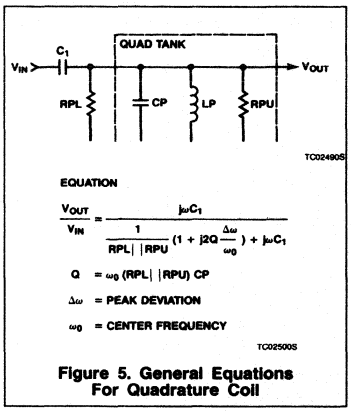


Figure 5. General Equations For Quadrature Coil

The quadrature coil or crystal/ceramic discriminator affects three system parameters: Bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network. Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A typical loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically 90mV_{RMS} with −35dB distortion.

While the NE614 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low-pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

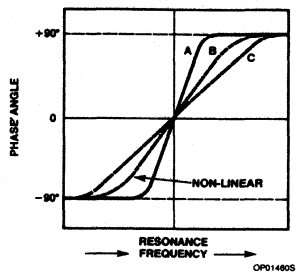


Figure 6. Quadrature

Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50μA. The signal strength indicator's transfer function is approximately 10μA per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

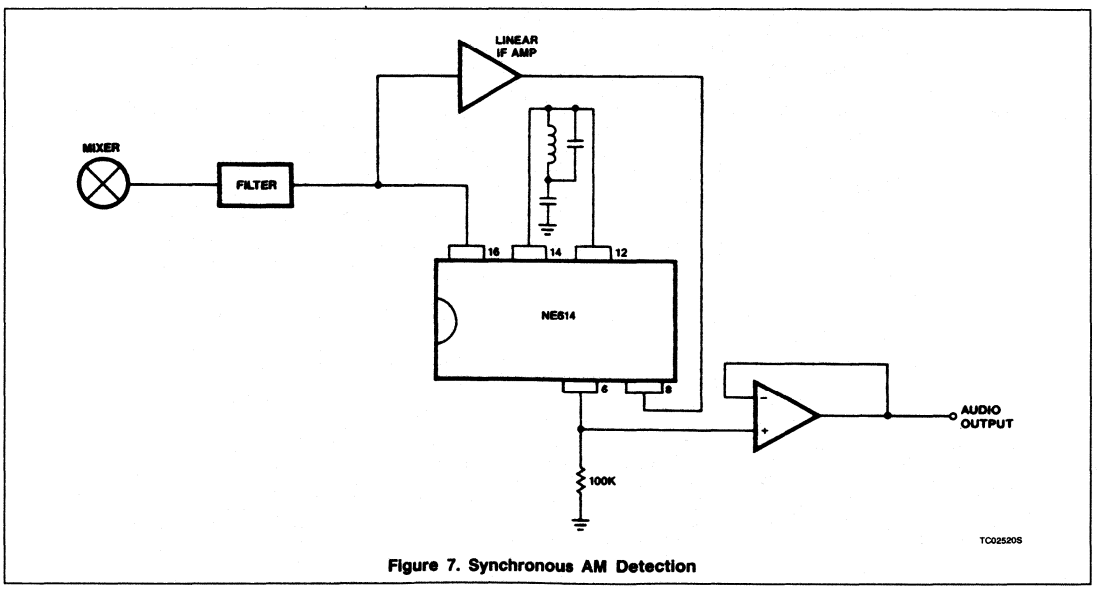


Figure 7. Synchronous AM Detection

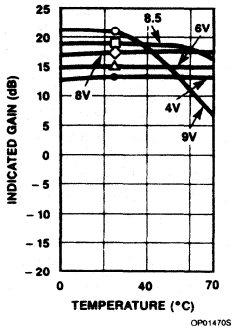


Figure 8. NE614 Indicated Gain vs Temperature and Voltage

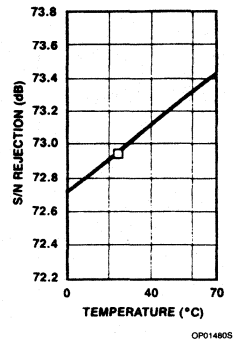


Figure 9. NE614 Signal-To-Noise Ratio vs Temperature

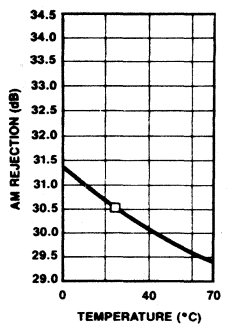


Figure 10. NE614 AM Rejection vs Temperature

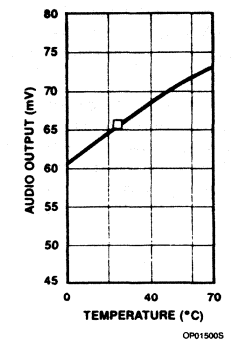


Figure 11. NE614 Audio Output vs Temperature

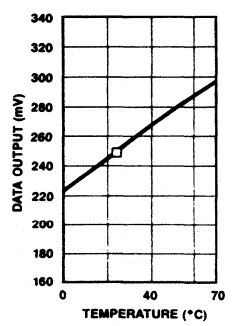


Figure 12. NE614 Data Output vs Temperature

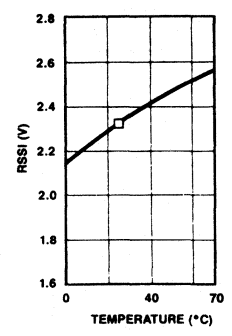


Figure 13. RSSI vs Temperature

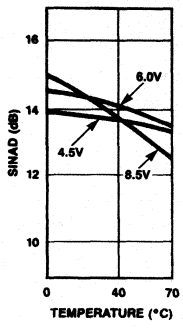


Figure 14. NE614 SINAD vs Temperature and V_{CC}

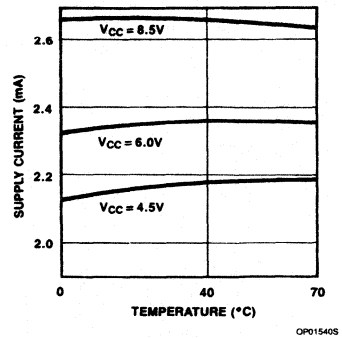


Figure 15. NE614 Supply Current vs Temperature

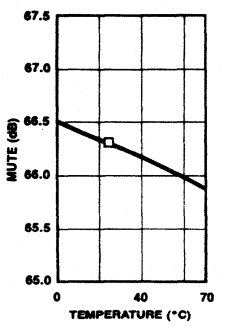


Figure 16. NE614 Muting vs Temperature

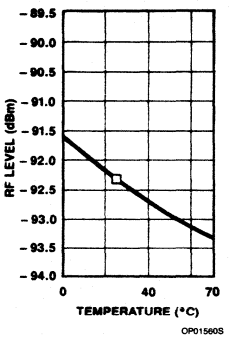


Figure 17. NE614 Limiting RF Level vs Temperature

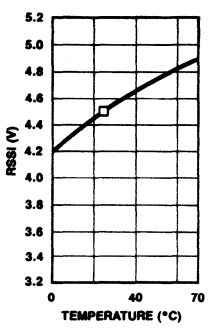


Figure 18. NE614 Large Signal Uncompensated RSSI Voltage vs Temperature

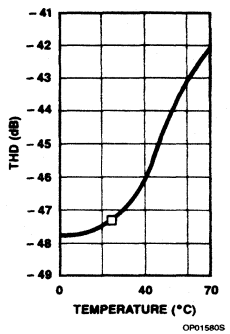


Figure 19. NE614 Total Harmonic Distortion vs Temperature

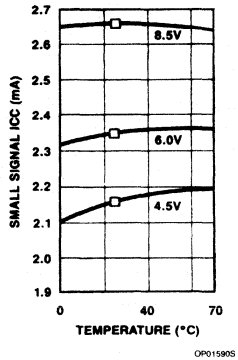


Figure 20. NE614 Supply Current vs Temperature and Voltage

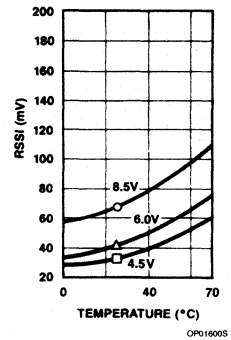


Figure 21. Small-Signal RSSI vs Temperature and Voltage

NE/SA5230
Low Voltage Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

FEATURES

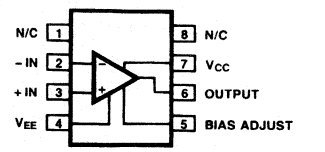
- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION

N, FE and D Packages



TOP VIEW

CD11071S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5230D
8-Pin Ceramic DIP	0 to +70°C	NE5230FE
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO	−40°C to +85°C	SA5230D
8-Pin Ceramic DIP	−40°C to +85°C	SA5230FE
8-Pin Plastic DIP	−40°C to +85°C	SA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE} – 0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	–65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Can exceed the supply voltages when $V_S \leqslant \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
   Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC} + 0.25	V
Common-mode voltage (negative)	V_{EE} – 0.25	V
Temperature		
NE grade	0 to 70	°C
SA grade	–40 to 85	°C

DC AND AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		$T_A = 25°C$		Any		0.4	3	mV
					Any		3	4	mV
V_{OS}	Drift				Any		2	5	μV/°C
I_{OS}	Offset current		$T_A = 25°C$		High		3	50	nA
			$T_A = 25°C$		Low		3	30	nA
					High			100	nA
					Low			60	nA
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	nA/°C
I_B	Bias current		$T_A = 25°C$		High		40	150	nA
			$T_A = 25°C$		Low		20	60	nA
					High			200	nA
					Low			150	nA
I_B	Drift				High		2	4	nA/°C
					Low		2	4	nA/°C
I_S	Supply current		$V_S = \pm 0.9V$	$T_A = 25°C$	Low		110	160	μA
				$T_A = 25°C$	High		600	750	μA
					Low			250	μA
					High			800	μA
			$V_S = \pm 7.5V$	$T_A = 25°C$	Low		320	550	μA
				$T_A = 25°C$	High		1.1	1.6	mA
					Low			600	μA
					High			1.7	mA
V_{CM}	Common-mode input range		$V_{OS} \leq 6mV$, $T_A = 25°C$		Any	$V^- - 0.25$		$V^+ + 0.25$	V
					Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		$V_S = \pm 7.5V$	$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$, $T_A = 25°C$	Any	85	95		dB
				$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$	Any	80			dB
PSRR	Power supply rejection ratio		$T_A = 25°C$		High	90	105		dB
			$T_A = 25°C$		Low	85	95		dB
					High	75			dB
					Low	80			dB
I_L	Load current	source	$V_S = \pm 7.5V$		Any	4	10		mA
		sink	$V_S = \pm 7.5V$		Any	5	15		mA
		source	$V_S = \pm 0.9V$		Any	1	5		mA
		sink	$V_S = \pm 0.9V$		Any	2	6		mA
		source	$V_S = \pm 0.9V$, $T_A = 25°C$		High	4	6		mA
		sink	$V_S = \pm 0.9V$, $T_A = 25°C$		High	5	7		mA
		source	$V_S = \pm 7.5V$, $T_A = 25°C$		High		16		mA
		sink	$V_S = \pm 7.5V$, $T_A = 25°C$		High		32		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	$V_S = \pm 7.5V$	$R_L = 10k\Omega$, $T_A = 25°C$	High	120	2000		V/mV
			$R_L = 10k\Omega$, $T_A = 25°C$	Low	60	750		V/mV
				High	100			V/mV
				Low	50			V/mV
V_{OUT}	Output voltage swing	$V_S = \pm 0.9V$	$T_A = 25°C$, +SW	Any	750	800		mV
			$T_A = 25°C$, -SW	Any	750	800		mV
			+SW	Any	700			mV
			-SW	Any	700			mV
		$V_S = \pm 7.5V$	$T_A = 25°C$, +SW	Any	7.30	7.35		V
			$T_A = 25°C$, -SW	Any	-7.32	-7.35		V
			+SW	Any	7.25	7.30		V
			-SW	Any	-7.30	-7.35		V
SR	Slew rate	$T_A = 25°C$		High		0.25		V/μs
		$T_A = 25°C$		Low		0.09		V/μs
BW	Inverting unity gain bandwidth	$C_L = 100pF$, $T_A = 25°C$		High		0.6		MHz
		$C_L = 100pF$, $T_A = 25°C$		Low		0.25		MHz
θ_M	Phase margin	$C_L = 100pF$, $T_A = 25°C$		Any		70		Deg.
t_S	Settling time	$C_L = 100pF$, 0.1%		High		2		μs
		$C_L = 100pF$, 0.1%		Low		5		μs
V_{INN}	Input noise	$R_S = 0\Omega$, f = 1kHz		High		30		$nV/\sqrt{Hz}$
		$R_S = 0\Omega$, f = 1kHz		Low		60		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion	$V_S = \pm 7.5V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.003		%
		$V_S = \pm 0.9V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.002		%

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, $V_{B1} = 0.8V$ at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

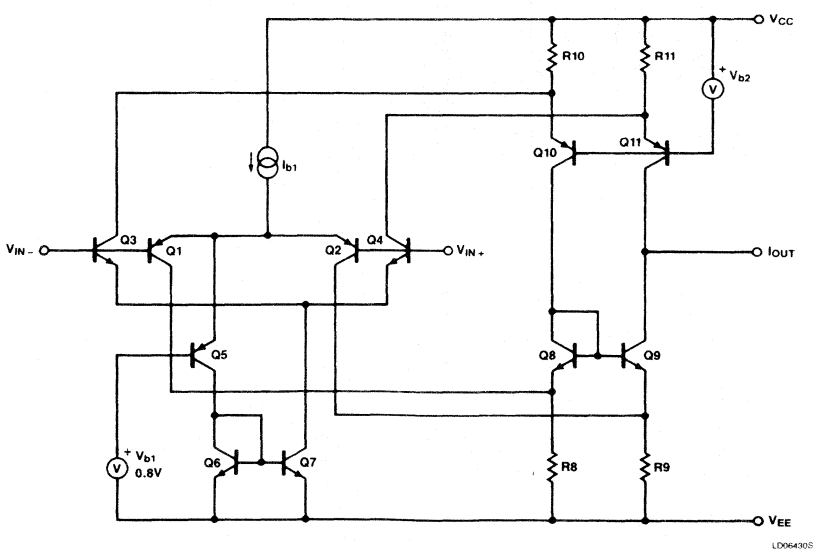


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Philips does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where $T_A \equiv$ Ambient Temperature
T_J = Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Package thermal resistance
= 270°C/W for SO-8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

θ_{JA} = 100°C/W for the plastic DIP;
θ_{JA} = 110°C/W for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data

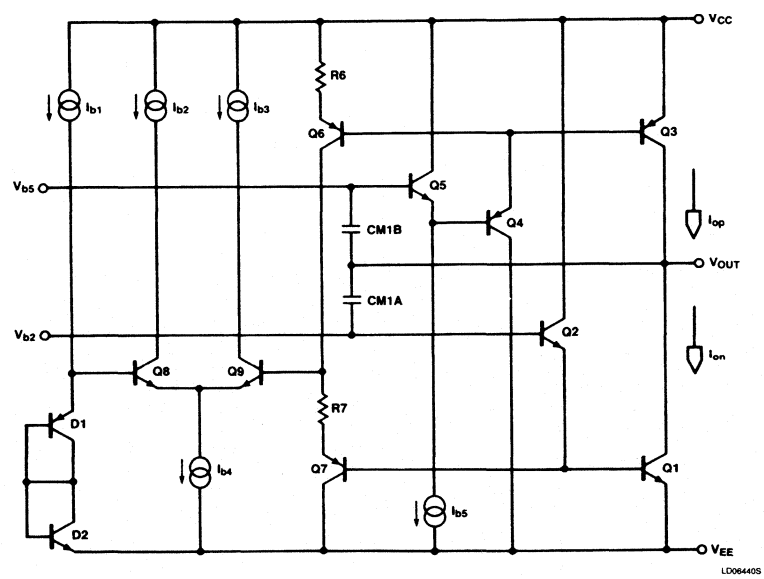


Figure 2. Output Stage

sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/μs at low bias and 0.25V/μs at high bias.

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

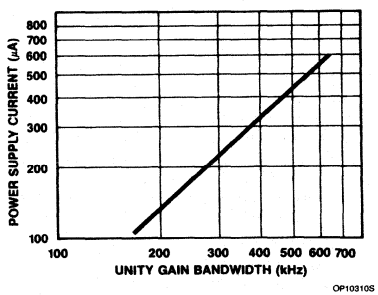
If extremely low signal distortion (< 0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

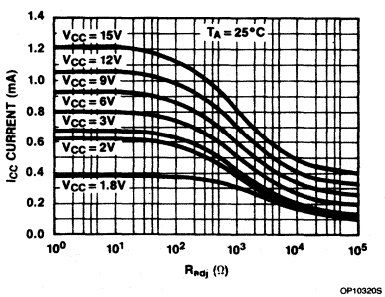
There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3

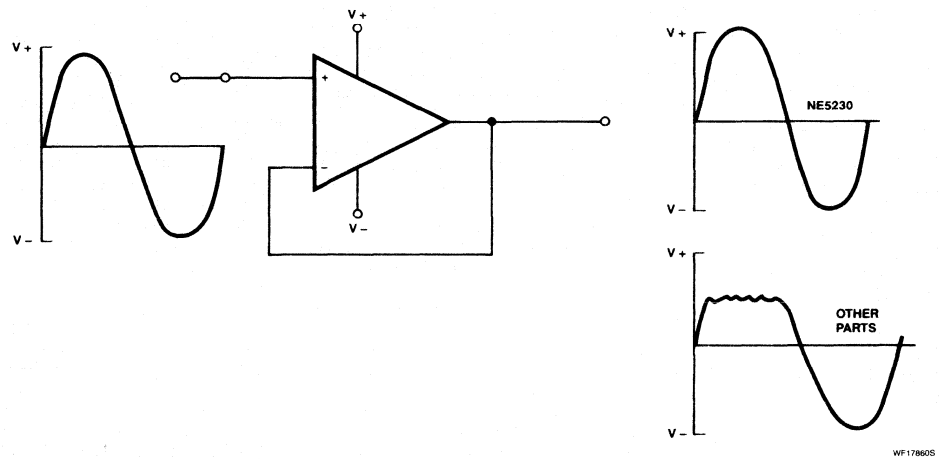


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability

the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN}/R_C \quad (2)$$

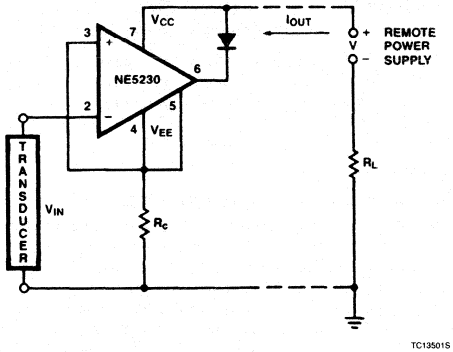
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

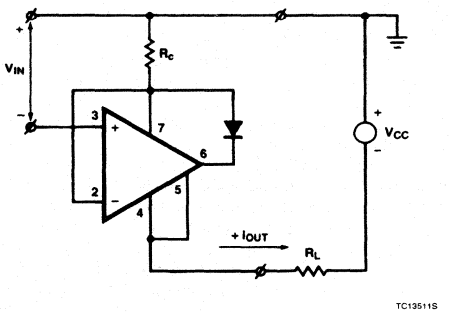
$$R_{L\ max} = [V_{remote\ supply}) - V_{CC\ min} - V_{IN\ max}]/I_L \quad (3)$$

Where $V_{CC\ min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration. The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used





NOTES:
1. $I_{OUT} = V_{IN/RC}$
2. $R_{L\ max} \simeq \frac{V_{REMOTE} - 1.8V - V_{IN\ max}}{I_{OUT}}$

For $R_C = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

a. The NE5230 as a Remote Transducer Transconductance Amp With 4 – 20mA Current Transmission Output Capability

b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

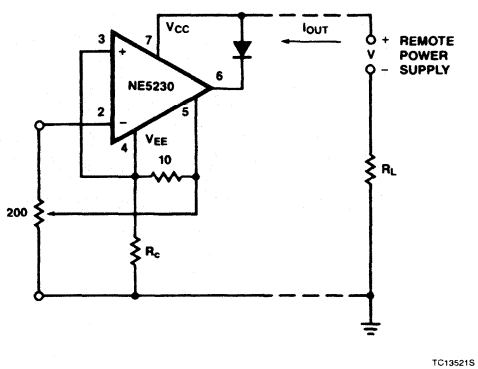
Figure 5

with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.



NOTES:
1. $I_{OUT} = V_{IN/RC}$
2. $R_L Max \simeq \frac{V_{REMOTE} - 1.8V - V_{IN} Max}{I_{OUT}}$

For $RC = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

Figure 6. NE5230 Remote Temperature Transducer Utilizing 4 – 20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

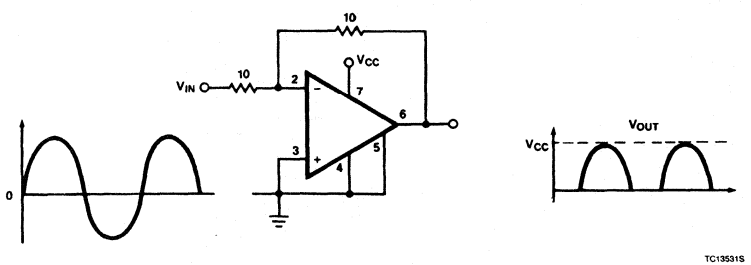
By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

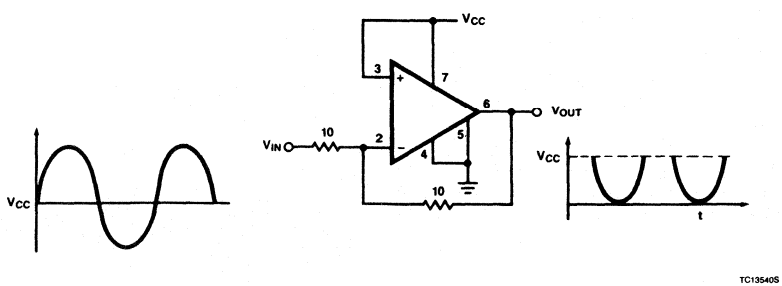
CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs



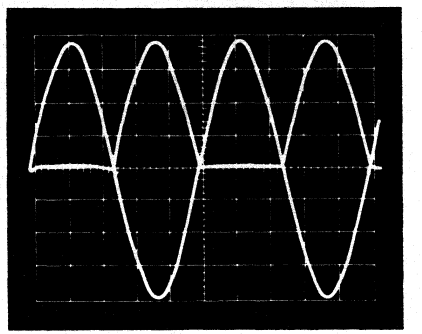
a. Rail-to-Ground Output Swing Referenced to Ground



b. Negative-Going Output Referenced to V_{CC}

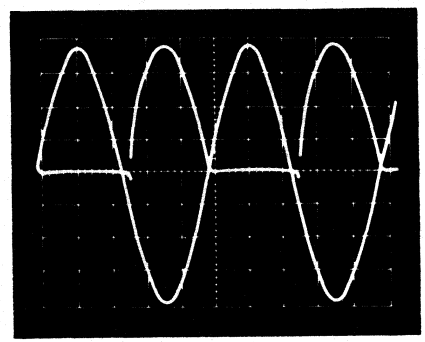
Figure 7. Half-Wave Rectifier With Positive-Going Output Swings

where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.



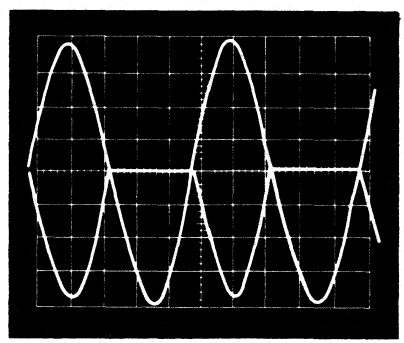
WF17870S

500mV/DIV 200μS/DIV
Biased to Ground



WF17880S

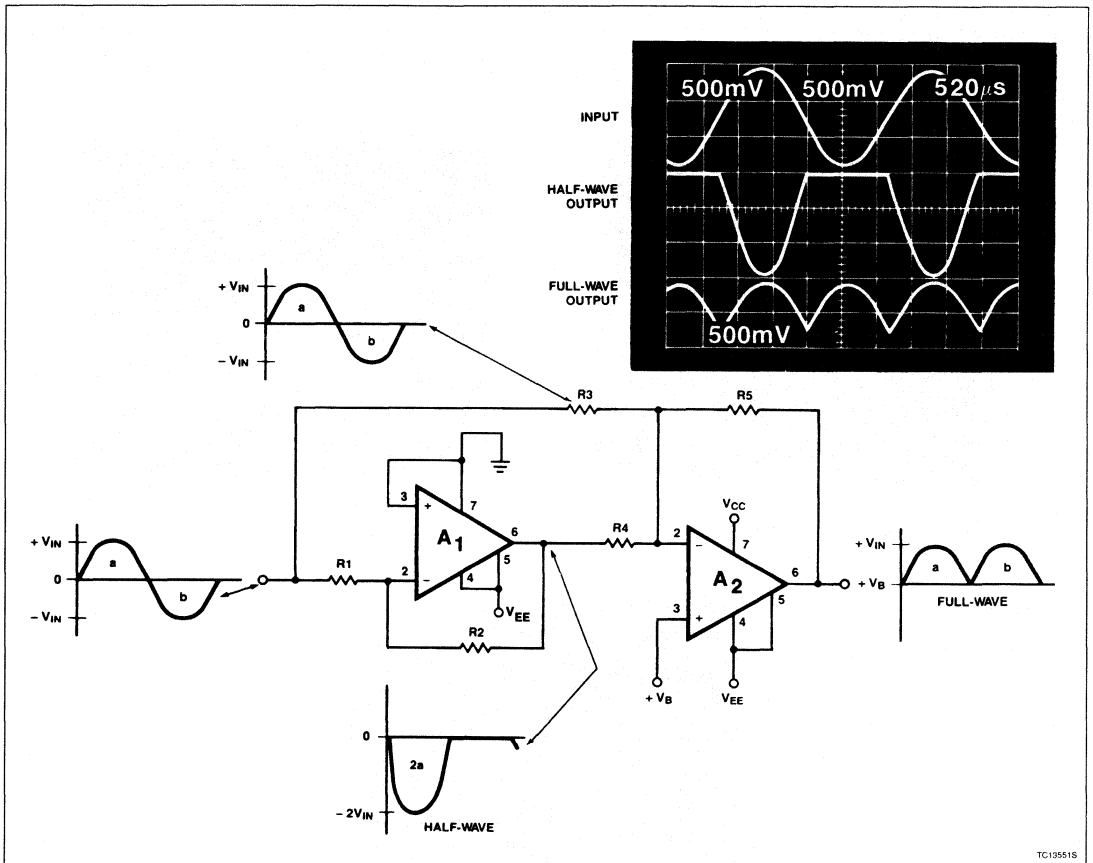
500mV/DIV 20μS/DIV
Biased to Ground



WF17890S

500mV/DIV 20μS/DIV
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply



NOTES:
R2 = 2 R1
R4 = R5 = R3
+ V_B will vary output reference.
For single supply operation V_{EE} can be grounded on A2.

Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave Rectifier will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers — Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook — A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

NE5900
Call Progress Decoder

Product Specification

Linear Products

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or reorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

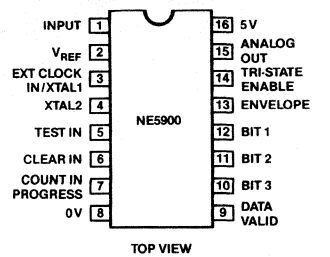
- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTTL, CMOS, NMOS**
- **Easy application**

APPLICATIONS

- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**
- **Pay telephones**

PIN CONFIGURATION

D[1] and N Packages

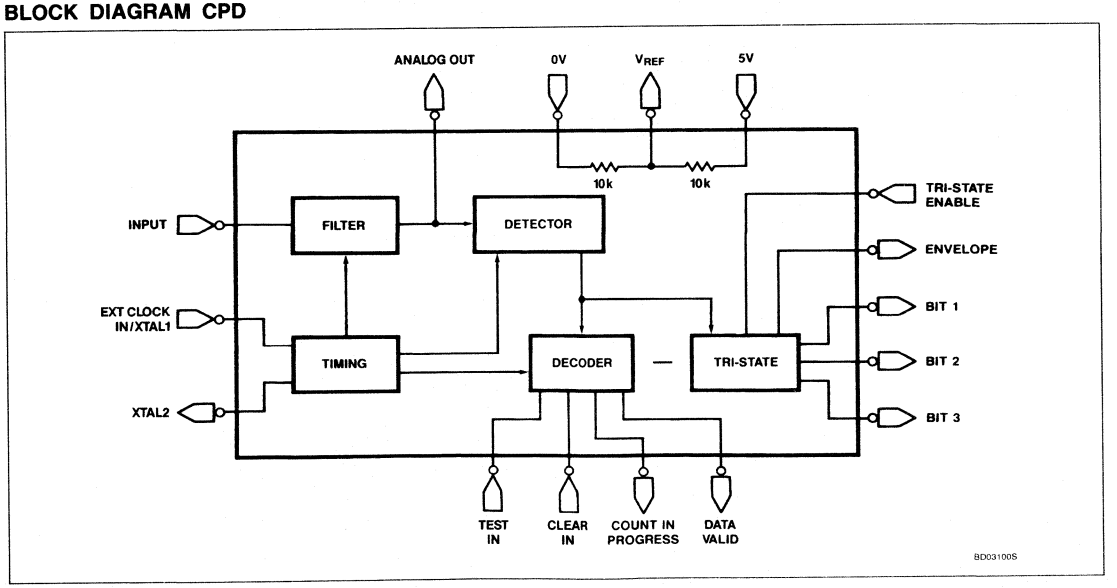


TOP VIEW

CD09970S

NOTE:
1. SOL — Released in large SO package only.

BLOCK DIAGRAM CPD



ORDERING INFORMATION

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5900D
16-Pin Plastic DIP	0 to +70°C	NE5900N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Power supply voltage	9	V
V_{IN}	Logic control input voltages	−0.3 to +16	V
V_{IN}	All other input voltages[1]	−0.3 to V_{CC} +0.3	V
V_{OUT}	Output voltages	−0.3 to V_{CC} +0.3	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_J	Junction temperature	+150	°C

NOTE:
1. Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS Unless otherwise stated, V_{DD} = +5.0V; Pin 3 f_{OSC} = 3.58MHz; Ambient Temperature = 0 to +70°C. Pin 5 = 0V, Pin 14 = V_{DD}.

SYMBOL	PARAMETER	TEST CONDITONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pins 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads.		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DC} = V_{REF} Output Pin 13 = V_{DD}		-39	-35	dB[1]
	Signal rejection	Pin 1 level, 300Hz frequency, V_{DC}=V_{REF} Output Pin 13 = 0V			-50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 input voltage	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 input voltage	Pins 6, 14	0		0.8	V
I_{HL}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	-1.0		1.0	μA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	-1.0		1.0	μA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} - 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} - 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13 Pin 14 = 0V	-3.0		3.0	μA
	Filter output gain	Input Pin 1, 460Hz - 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	-1.0		1.0	dBmo
	Input impedance[2]	Pin 1, frequency = 460Hz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz - 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTES:
1. 0dB = 0.775V_{RMS}.
2. By design; not tested.

The NE5900 uses the signal in the call progress tone passband and the cadence or interrupt rate of the signal to determine which call progress tone is present.

Figure 1 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from line transients. The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of −39dB typical (0dB = $0.775V_{RMS}$). The decoder will not respond to any signals below −50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3-second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 − 12, can be read.

The output code is as follows:

	PIN 12	PIN 11	PIN 10
DIAL TONE	0	0	0
RINGING SIGNAL	1	0	0
BUSY SIGNAL	0	1	0
REORDER TONE	0	0	1
OVERFLOW	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3-second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval. Note that the end of dial tone is interpreted as a valid ringing signal.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2μs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6). When dialing is complete, the device is cleared and ready to respond to the next call progress unit.

Enable is held at 5V to enable Pins 10, 11, 12, and 13. When enable is brought low, data valid is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications.

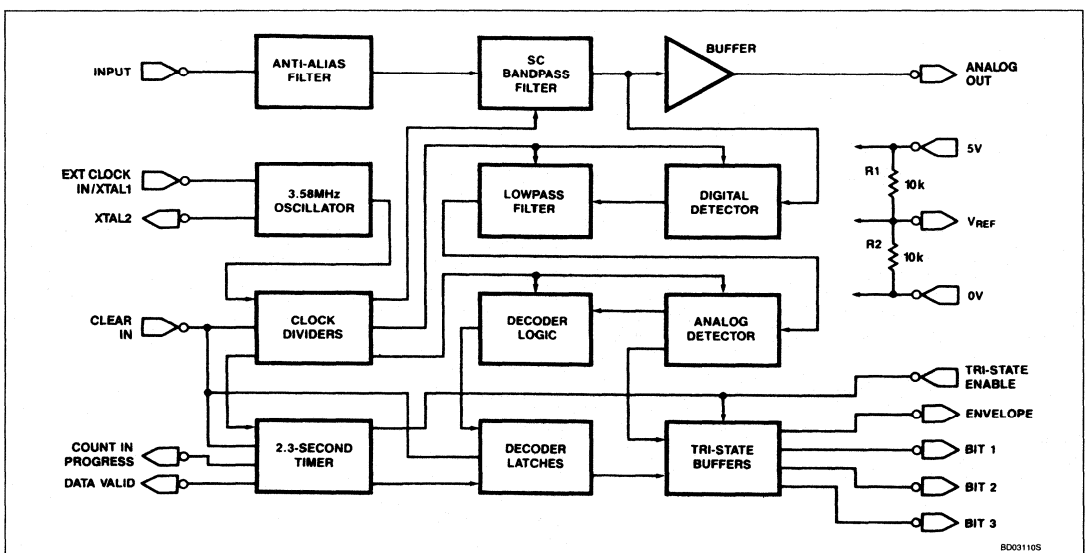


Figure 1. Detailed Block Diagram CPD

Figure 2 shows a typical application of the call progress decoder.

In this application only one external component is needed and no microprocessor activity other than clear is required.

Figure 3 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 4 gives a typical timing diagram for the application of Figures 2 and 3.

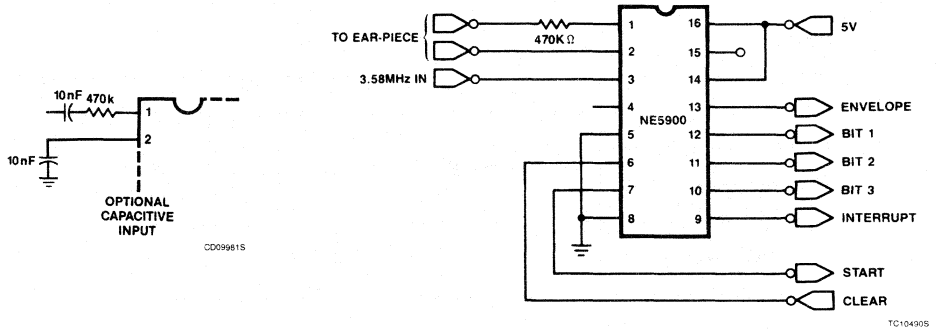


Figure 2. Typical Application

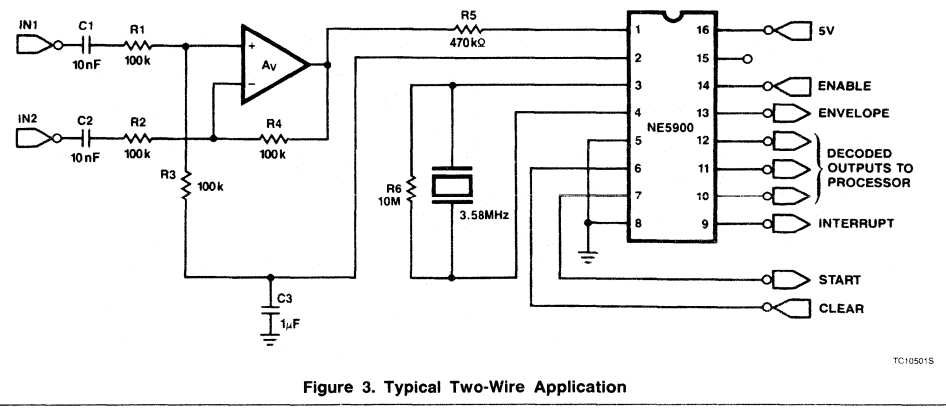


Figure 3. Typical Two-Wire Application

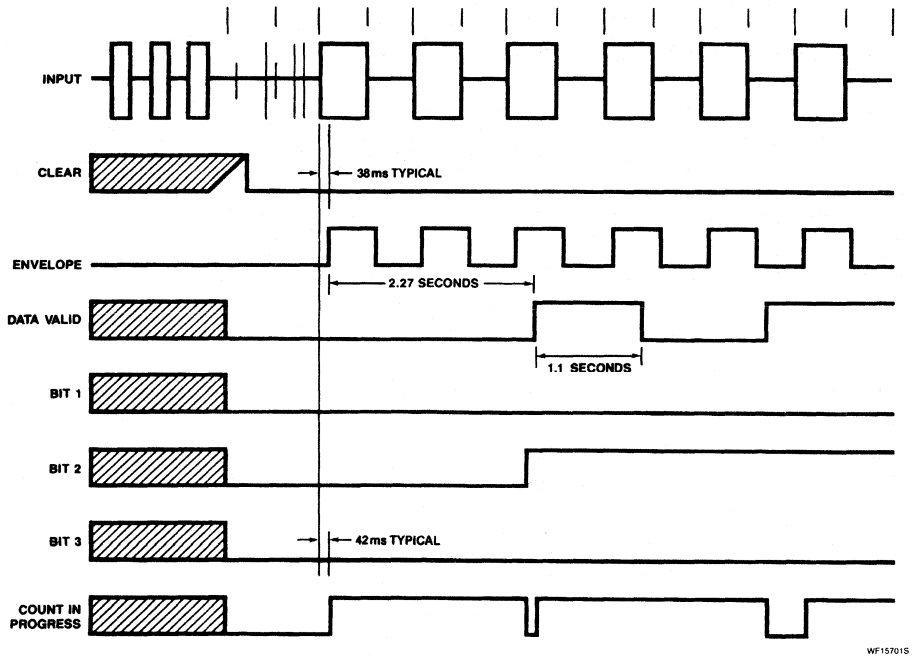
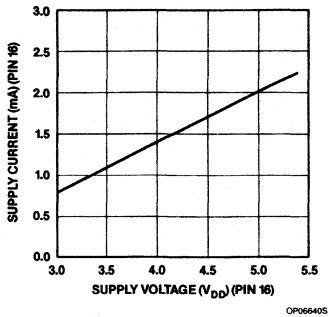

INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
WF15701S

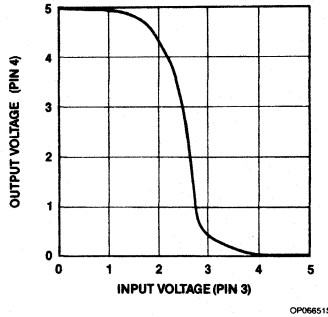
Figure 4

TYPICAL PERFORMANCE CHARACTERISTICS

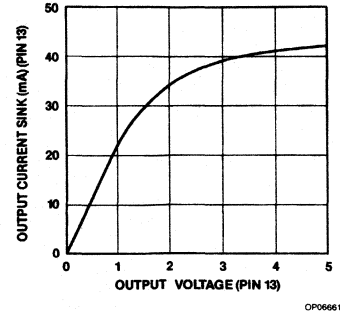
Power Supply Current vs V_{DD}



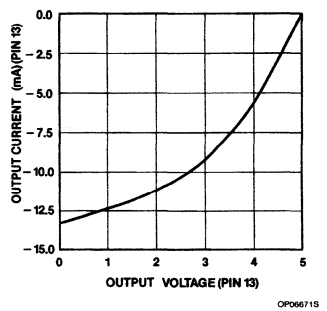
Voltage Transfer Curve



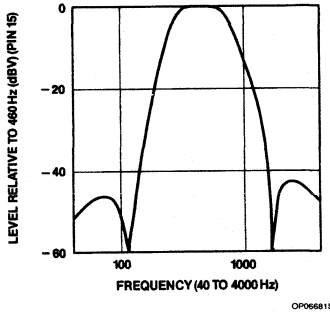
Output Voltage Current Curve Digital Output Low



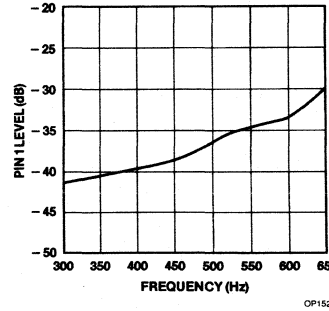
Output Voltage Current Curve Digital Output High



Filter Frequency Response



Typical Threshold



LOW COST SPEECH DEMONSTRATION BOARD

GENERAL DESCRIPTION

The low cost speech demonstration board is designed to add voice output to existing card based electronic equipment with the minimum of additional effort and components. The majority of components used are of the CMOS type with low power consumption making the board suitable for battery operation.

Applications include speech evaluation and speech demonstration.

FEATURES

- PCF8200 speech synthesizer
  - Male and female speech of very high quality
  - CMOS technology
  - Extended operating temperature range
  - Programmable speaking speed
- Low current consumption
  - All major components use CMOS technology (PCF8200, 80C39 and 27C64)
- Very large vocabulary up to 12 minutes
  - 4 EPROM sockets
  - EPROM selection for 27C16 to 27C256
  - Low data rates for synthesizer (average 1500 bits per second)
- Easy interfacing
  - 8-bit parallel data bus/key switch input
  - Volume control, speaker connection
  - Control signals (e.g. RESET, BUSY etc etc)
- Simple operating modes
  - ROM selection
  - Word sequence within a ROM
  - Repeat last utterence
  - Control software is readily customizeable
  - To implement parameter download from external source
- Single Eurocard size PC board
- Single + 5 V supply
- Low cost

APPLICATIONS

- OEM design-in
- May be simply used with many card systems for speech evaluation
- Speech demonstration
  - Particularly simple when used with the OM8201 (Speech Demonstration Box)

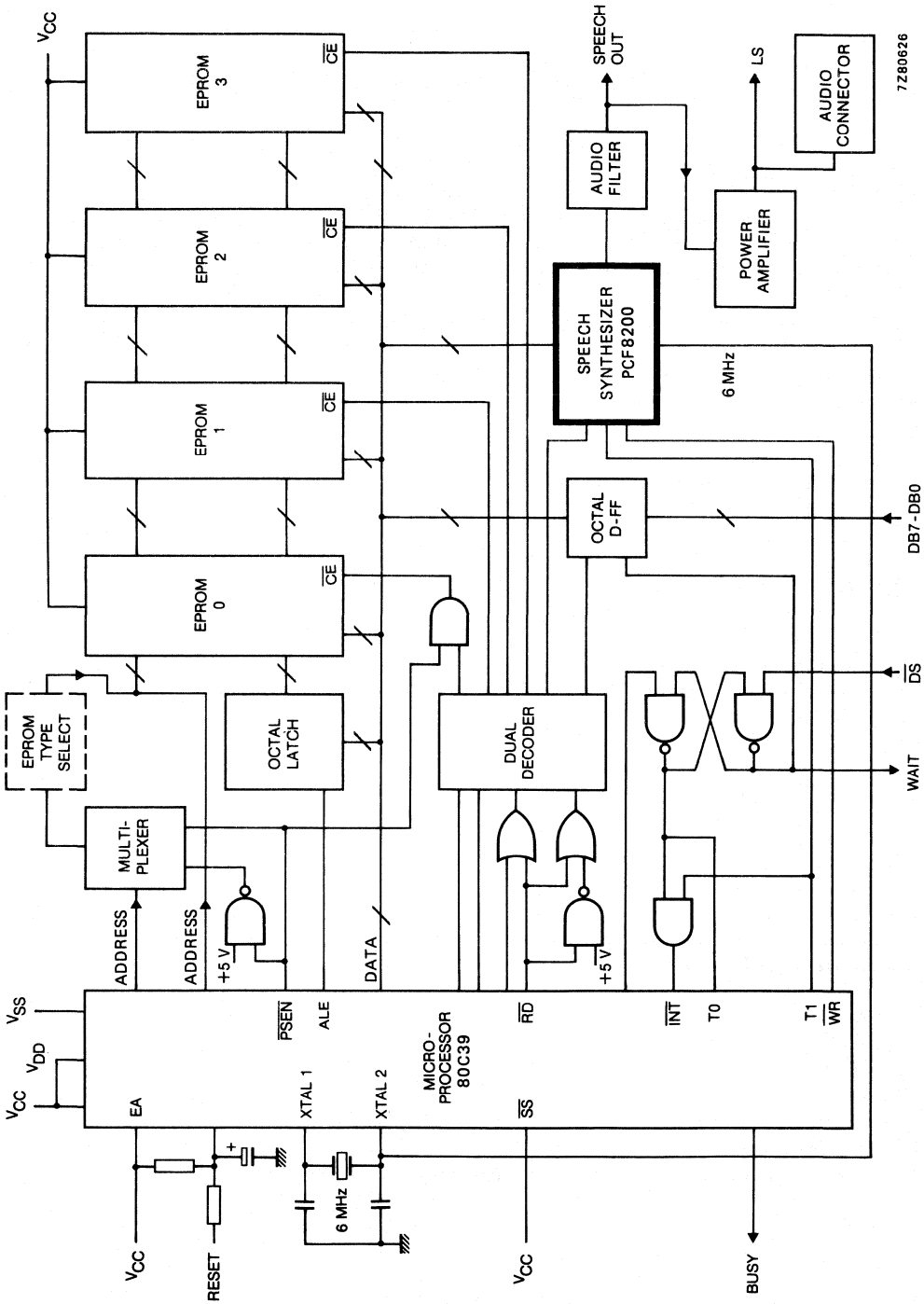


Fig. 1 Block diagram.

OPERATION

HARDWARE DESCRIPTION

The main controlling microprocessor is an 80C39 running at 6 MHz. This device supplies all of the main controlling signals for the board operation and the interfacing to any external system.
Four sockets are provided for EPROMS which contain speech coding. These may be 27C16 types, through to 27C256 types; the sockets will be a low insertion force type to allow for easy customizing.
The board will be supplied with one socket occupied by a 27C64 which will contain the control program and some speech examples. All four EPROM sockets must contain the same EPROM type.

The speech synthesizer PCF8200 converts the coding into a speech output. This synthesizer has been designed to simulate the human vocal tract using five formants for male and four formants for female speech. Periodic updating of the parameters for these formants can produce very high quality speech.

The output of the synthesizer can be fed into an audio amplifier, TDA7050, via a resistor-capacitor filter network which provides a frequency cut-off above 5 kHz of about 25 dB. The configuration of the audio amplifier used on this board gives an output of 140 mW peak power into a 25 Ω speaker from a 5 V supply.

Connections are made to the board via a standard DIN/IEC connector. This allows access to the 8-bit parallel data bus so that speech coding from an external source may be used, if implemented, and allows the selection of speech phrases by an external system, such as a microcomputer or even a bank of switches. The same connector also permits the addition of a volume control, loudspeaker, a high impedance audio output, and power supply. The control signals RESET, BUSY, WAIT and DS are also taken to the outside of the board. There is also a loudspeaker plug on the board.

All components are contained on a standard single Eurocard, and therefore suitable for rack mounted equipment.

SOFTWARE DESCRIPTION

All the software required to operate the board is contained in the only EPROM supplied. The software is written in modular from so that it is possible for a customer to alter or add to any particular function which suits his applications. An industrial standard microprocessor was chosen so that readily available development systems could be used to facilitate this modification.

There are four main modes of operation:

- ROM Selection
- Word Sequence
- Repeat Word
- Speaking Speed Selection

These modes are all controlled by software.

ROM Selection mode permits access to an individual EPROM and pronounces the first utterence from that EPROM.

Word Sequence gives the next word (activated by repeated access to the same EPROM) and if continually exercised will keep looping on the words in that EPROM.

The Repeat Word command allows indefinate repetition of the last utterance pronounced.

The Speaking Speed Selection allows the utterence to be pronounced at a different speed.

The software also controls the address sequencing within the utterance and ensures that the required data is supplied to the synthesizer.

There are also some examples of words/utterences encoded in the remainder of the supplied EPROM. These words are intended for demonstration purposes and will show the features of the synthesizer when selected. The main features being illustrated are:

- Male speech in several languages
- Female speech in several languages
- Programmable speaking speed

ORDERING INFORMATION

Product name: Low Cost Speech Demonstration Board

Type number: OM8200

Ordering code: 9337 541 30000

Orders should be placed with your local Philips/Signetics agency.

SPEECH DEMONSTRATION BOX

GENERAL DESCRIPTION

Speech demonstration box OM8201 is designed to be used in conjunction with the low cost speech demonstration board OM8200. The box contains all the necessary components to drive the board. The combination of these two components make an extremely attractive demonstration unit.

FEATURES

- Low cost
- Can use unmodified OM8200 board which allows access to all features of the OM8200
- Single + 9 V supply
  - Low power consumption therefore permits battery operation
  - External power supplies may also be used
  - Voltage is regulated and dropped to a standard + 5 V for the OM8200 board
- Simple mechanical construction
  - Allows easy access to the OM8200 for changing EPROMS
- Contains all peripherals needed to drive the OM8200

HARDWARE DESCRIPTION

The box contains a set of eight keypad switches which are connected to the data bus. Four switches can select which EPROM your speech data is derived from. Repeated pressing of an EPROM switch increments the expression number which will be uttered. To repeat the last expression, a separate switch must be activated.

It is possible in the PCF8200 to change the rate of speaking to 73%, 123% or 145% of the normal speed. A switch has been included on the box which will sequence through the speed options making the same utterance every time.

One of the two remaining switches is the master reset for the program and the other is for future enhancements of the box.

Included in the box are, the volume control for the amplifier, the loudspeaker, and a high impedance audio output.

The final piece of electronics is the power supply. This can be supplied from a + 9 V internal battery or from a + 9 V external supply. The + 9 V is regulated to a + 5 V supply which is then fed to other parts of the box and to the OM8200.

The box is of simple construction and allows easy access to the OM8200 for changing of EPROMS.

SOFTWARE DESCRIPTION

There is no software in the OM8201. The software of the OM8200 may be used in an unmodified form without any problems. However, if changes have been made to the control program of the OM8200 then different functions for the switches of the box can be achieved.

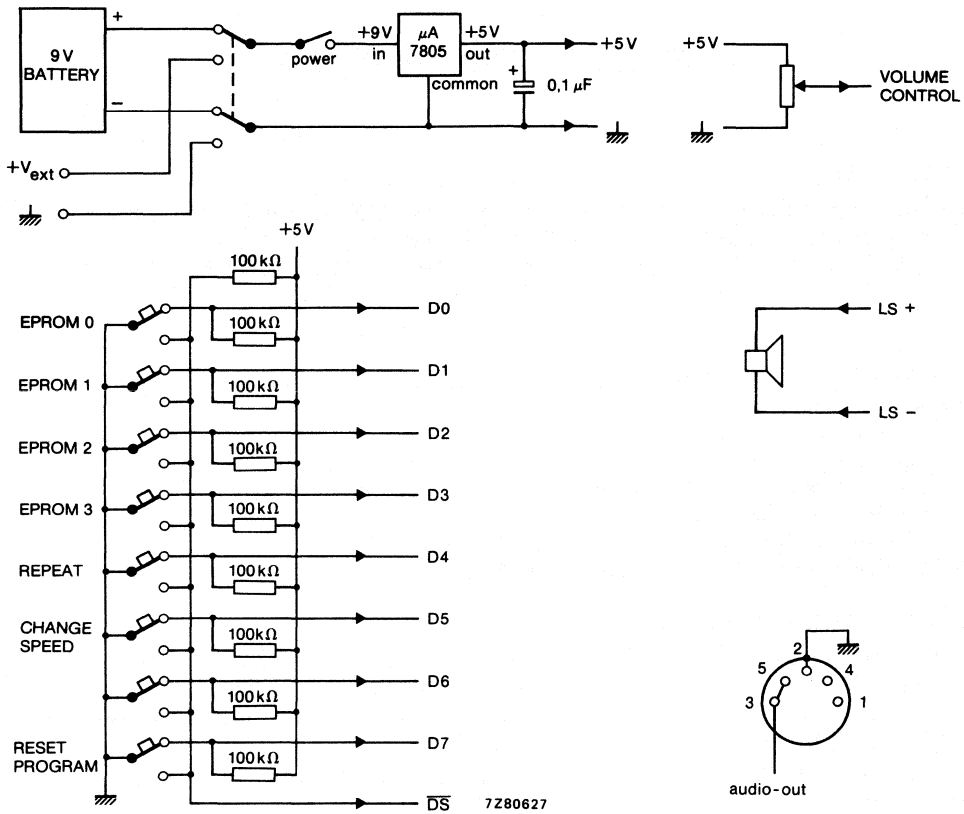


Fig. 1 Schematic diagram.

ORDERING INFORMATION

Product name: Speech Demonstration Box

Type number: OM8201

Ordering code: 9337 541 40000

N.B. OM8200 must be ordered as well if this box is to be used in demonstration mode. The order number for the OM8200 is 9337 541 30000.

Orders should be placed with your local Philips/Signetics agent.

SPEECH ANALYSIS/EDITING SYSTEM

GENERAL DESCRIPTION

The OM8210 is a speech analysing/editing system, and comprises of a speech adapter box and associated software. The system uses either the HP9816S or IBM-PC personal computer.
The OM8210 and the computer function together to produce speech coding for the PCF8200.
The system has many commands available, mostly single key operations, which gives it flexability.

FEATURES

- Input sampling of analogue speech signals
- Speech analysis
- Graphic parameter representation
- Parameter editing screen
- Conversion of parameters to PCF8200 synthesizer
- EPROM programming
- Parameter storage on floppy disc
- Speech output via PCF8200 voice synthesizer

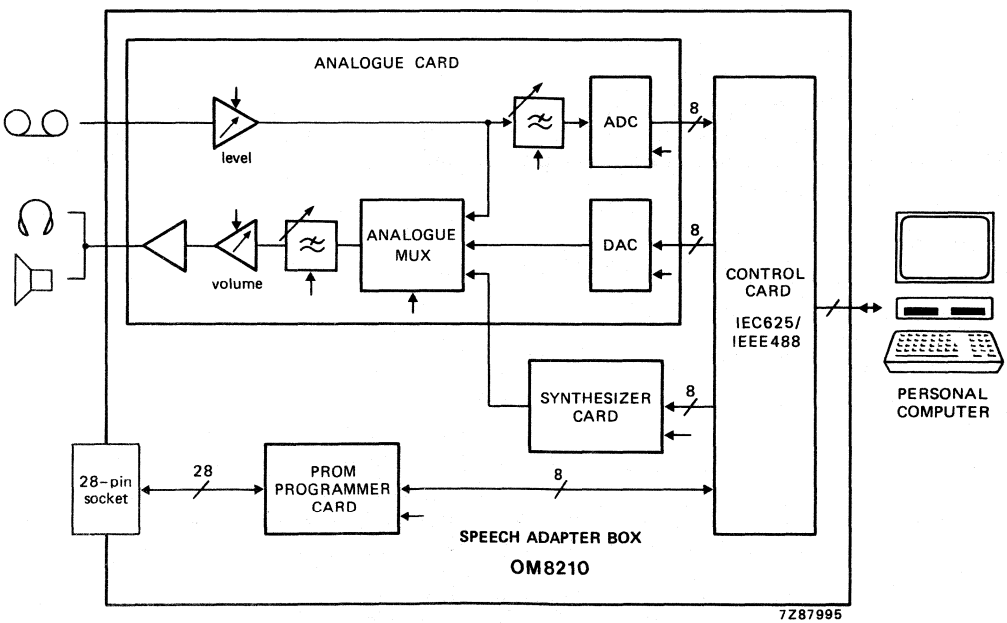


Fig. 1 Block diagram.

HARDWARE DESCRIPTION

The hardware for the OM8210 is contained in an attractive box with access to all the interconnections (IEC 625, interface loudspeaker, headphones, tape input, and EPROM socket), from the front panel. There are four single Eurocards and a power supply forming the speech adapter box.
These cards are:

- Analogue Card
- Synthesizer Card
- EPROM Card
- Control Card

Analogue Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analogue-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analogue converter (DAC) on the analogue card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analogue multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

Synthesizer Card

This card accommodates the PCF8200 voice synthesizer and a small amount of peripheral components and a socket for the MEA8000 voice synthesizer.

EPROM Programmer Card

This card allows four different types of EPROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

Control Card

This card performs three functions:

- IEC 625/IEEE 488 interface
- Control sequencer
- Clock generator

The IEC/IEEE interface is a simple talker/listener implementation with a HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEC/IEEE interface and the chip enable signals for the rest of the system (the ADC, the DAC, the synthesizer and control circuits).

The filter sampling frequency is generated with a software programmable PLL frequency synthesizer. The speech sampling frequency is derived from the filter sampling frequency by frequency division. Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available.

Each mode and each command in the mode is selected by single key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are:

Sample Mode	Samples and digitizes the recorded speech, the amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible.
Analysis Mode	Generates speech parameters from samples. The analysis selects the voiced/unvoiced sections, extracts the formants (5 for male and 4 for female), amplitude, and the pitch, and quantisizes the speech parameters.
Parameter Edit Mode	Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours, or amplitudes, concatenate sounds and optimize data rate by editing the frame duration.
Code Mode	Generates PCF8200 code and permits the arrangement of utterences in the optimum order of application. This mode also generates the address map at the head of the EPROM.
EPROM Mode	Used to program/read EPROMS with data for the code memory also possible is a new check, bit check and verification commands.
File Mode	Stores speech parameters or codes on disc, can also assemble code speech segment from an already existing library.
Media Mode	For diskette initialization and making back-up copies.
Option Mode	Allows the system configuration to be read or changed.

The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines. The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

Computer System

The following equipment is required to make a complete Hewlett Packard based editing system:
- HP9816S-630 (optimum computer type) or HP9817
- HP9121D (dual floppy disc)
- Additional memory card for the HP9816S (512 K bytes total required)

The following equipment is required to make a complete IBM based editing system:
- IBM-PC or PC-XT or Philips P3100
- Additional memory (512 K recommended)
- Display graphics card (Hercules monochrome)
- IEEE488 card (Tecmar Rev. D.)

ORDERING INFORMATION

Product name:	Speech Analysis/Editing System
Type number:	OM8210
Ordering code:	9337 561 50112

The computer system should be purchased from your local agents.
The OM8210 should be ordered through your local Philips/Signetics agent.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD3310 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed mode dialling; start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  - manual dialling — minimum duration for bursts and pauses
  - redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents at V_{DD} = 3,0 V			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 1,2	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3310P: 20-lead DIL; plastic (SOT146).
PCD3310T: 28-lead mini-pack; plastic (SO28; SOT136A).

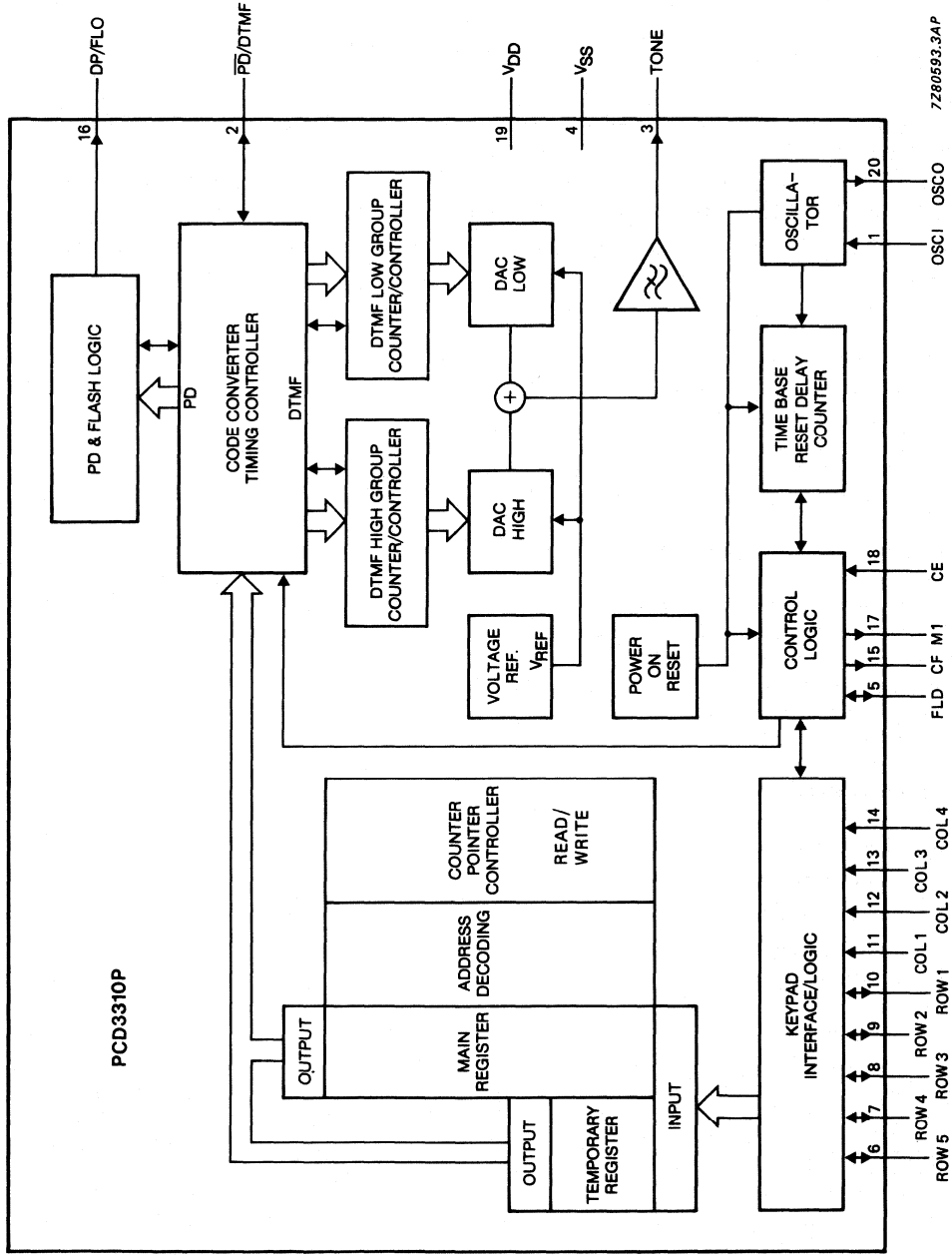


Fig. 1 Block diagram; PCD3310P.

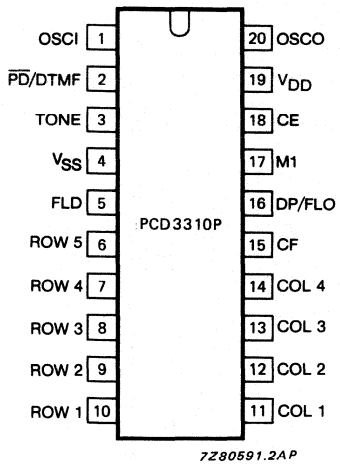
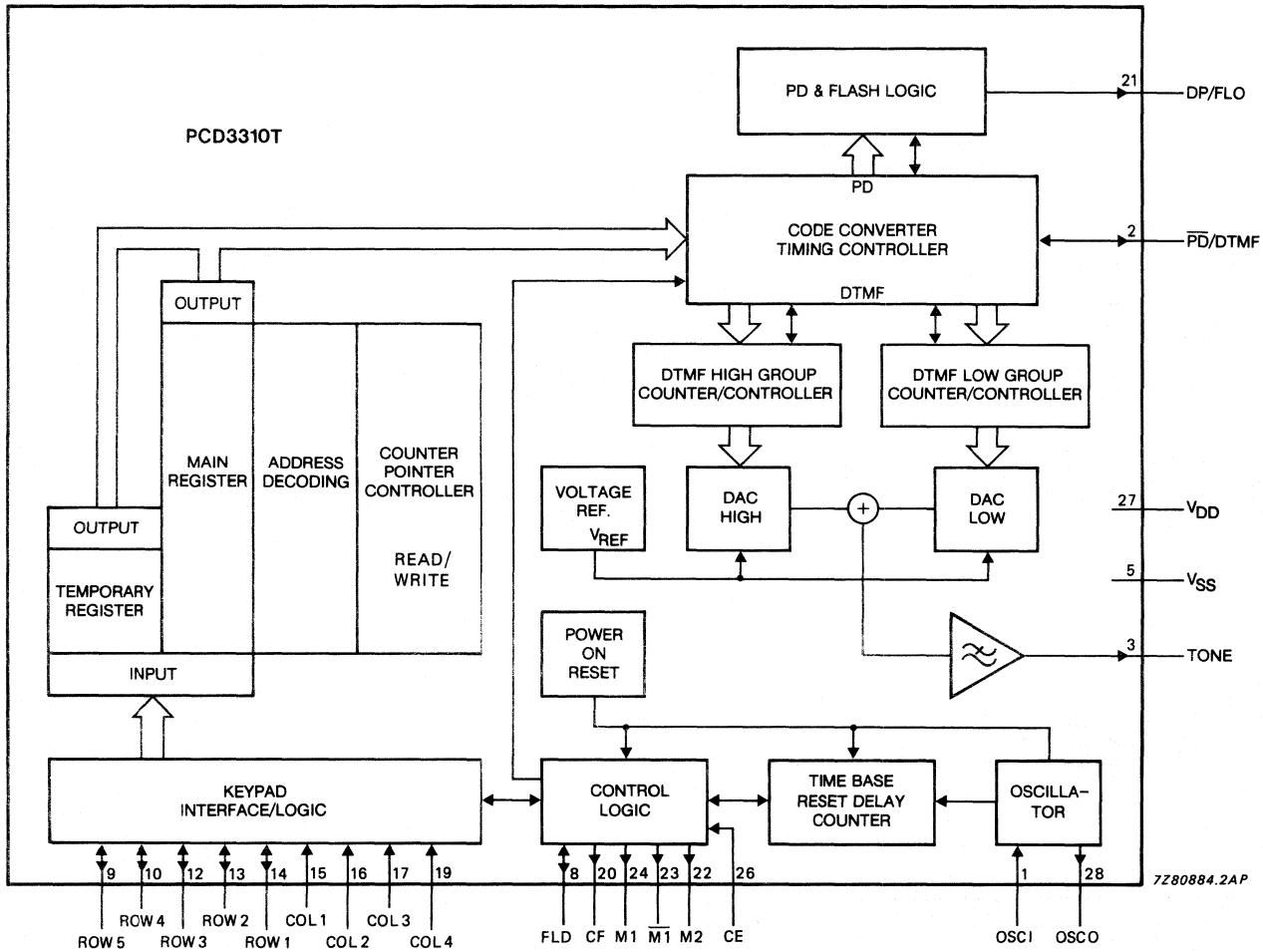


Fig. 2 Pinning diagram; PCD3310P.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	FLD	flash duration control input/output
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	COL 4	
15	CF	330 Hz confidence tone output to provide audible feedback of key entries
16	DP/FLO	dialling pulse and flash output
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA



Note: Pins 4, 6, 7, 11, 18 and 25 are not connected.

Fig. 3 Block diagram; PCD3310AT.

DEVELOPMENT DATA

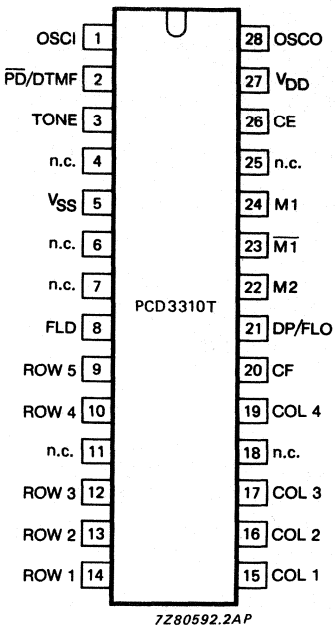


Fig. 4 Pinning diagram for PCD3310T.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	n.c.	not connected
5	V_{SS}	negative supply
6	n.c.	not connected
7	n.c.	not connected
8	FLD	flash duration control input/output
9	ROW 5	scanning row keyboard input/outputs
10	ROW 4	
11	n.c.	not connected
12	ROW 3	scanning row keyboard input/outputs
13	ROW 2	
14	ROW 1	
15	COL 1	sense column keyboard inputs with internal pull-ups
16	COL 2	
17	COL 3	
18	n.c.	not connected
19	COL 4	sense column keyboard input with internal pull-up
20	CF	330 Hz confidence tone output to provide audible feedback of key entries
21	DP/FLO	dialling pulse and flash output
22	M2	strobe; active HIGH during transmission
23	$\overline{M1}$	inverted mute output
24	M1	muting output
25	n.c.	not connected
26	CE	chip enable input
27	V_{DD}	positive supply
28	OSCO	oscillator output

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on-reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD3310 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary Write Address Counter (TWAC) which point to the last entered digit (see Fig. 7). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 11a, Fig. 11b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric (A, B, C, D, *, #) or the ">" key is activated. Then the circuit changes over to DTMF dialling and remains there until FL is activated or, after a static standby condition, CE is re-activated.

A connection between $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the PCD3310 are directly connected to the keyboard as shown in Fig. 5.

All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 11. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

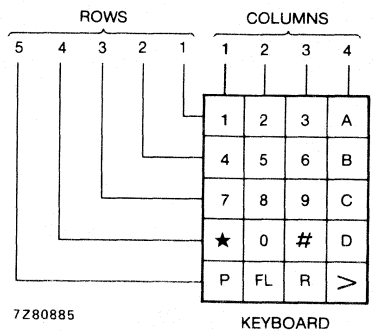


Fig. 5 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric pushbuttons (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, FL and R.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In mixed mode all key entries are valid and executed accordingly.

FUNCTIONAL DESCRIPTION (continued)

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling mode. Pressing the FL pushbutton will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig. 6).

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

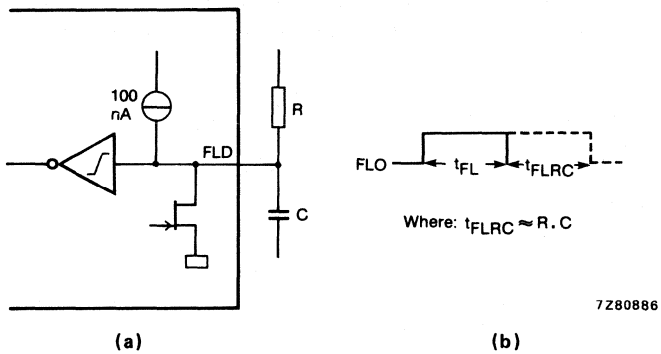


Fig. 6 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+ 0,13	+ 0,90
row 2	770	770,46	+ 0,06	+ 0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+ 0,24	+ 2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+ 0,42	+ 5,66
col 3	1477	1482,21	+ 0,35	+ 5,21
col 4	1633	1638,24	+ 0,32	+ 5,25

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling.

Confidence tone output (CF)

When any of the keys are activated a square-wave is generated and appears at this output to serve as an acoustic feedback for the user.

DEVELOPMENT DATA

DIALLING PROCEDURES (see also Figs 8, 9 and 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 7). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated write address counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 11. Each entry is tested for validity before being deposited in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD3310 is in the conversation mode.

If "R" is the first keyboard entry the circuit starts redialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the redialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for redialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, redialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

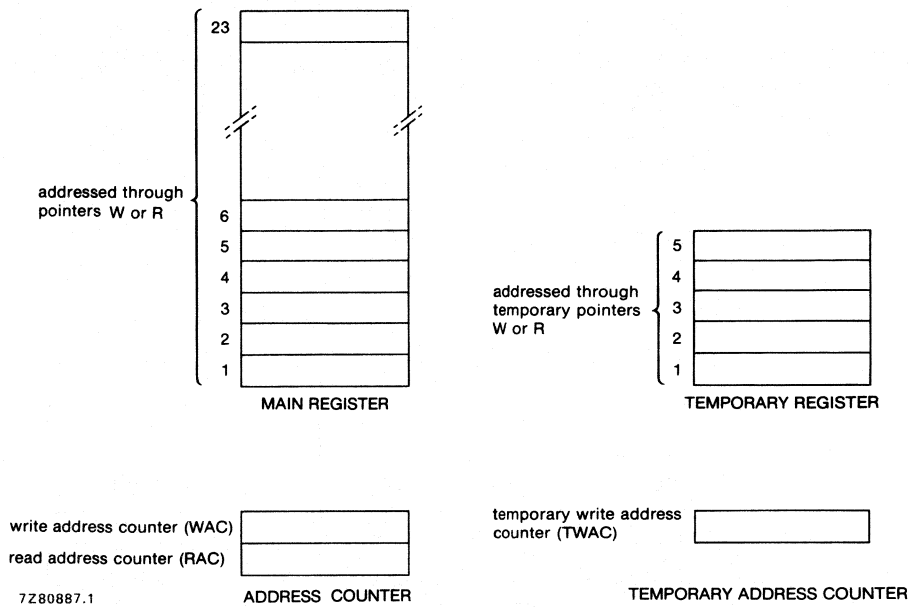
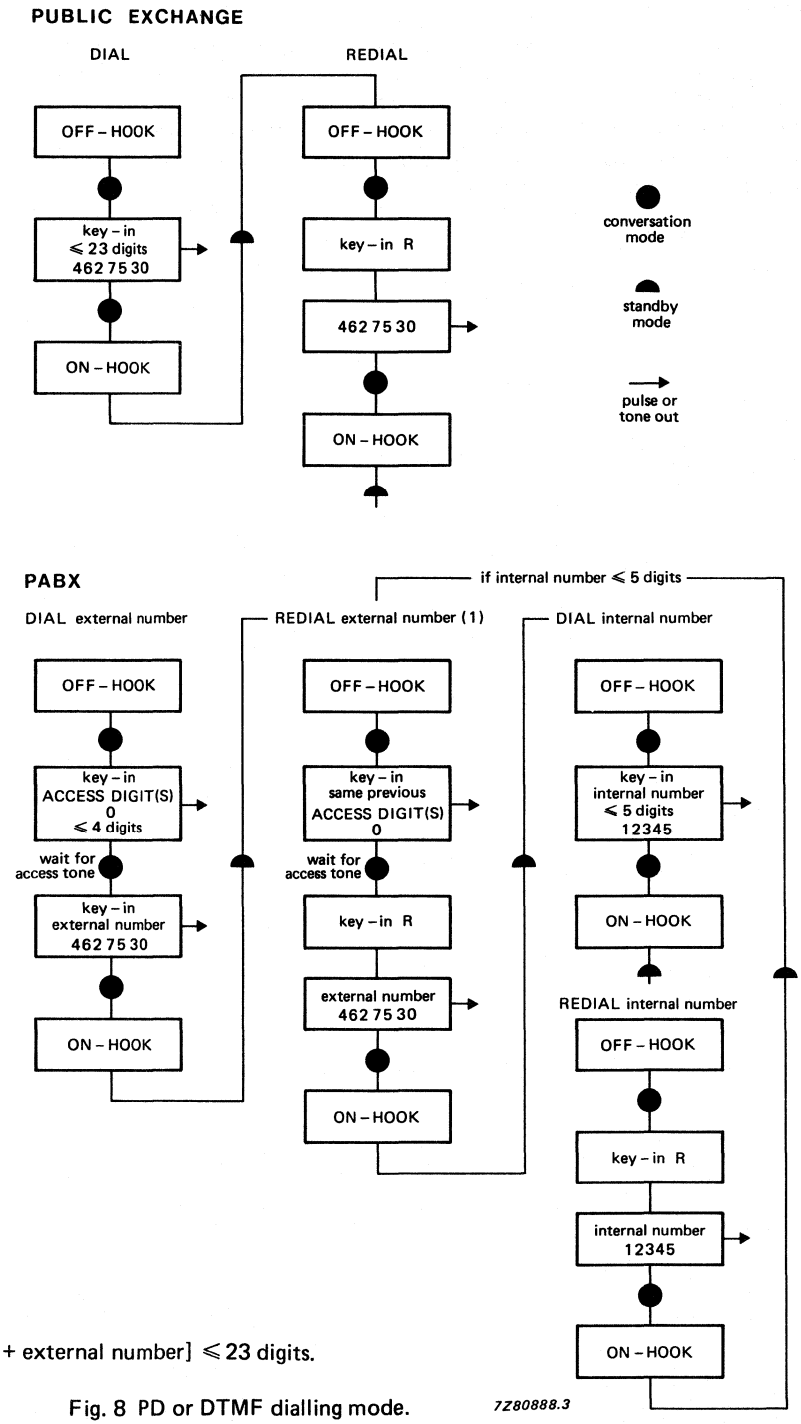


Fig. 7 Memory map.

DIALLING PROCEDURES (continued)



(1) If [access digit(s) + external number] ⩽ 23 digits.

Fig. 8 PD or DTMF dialling mode.

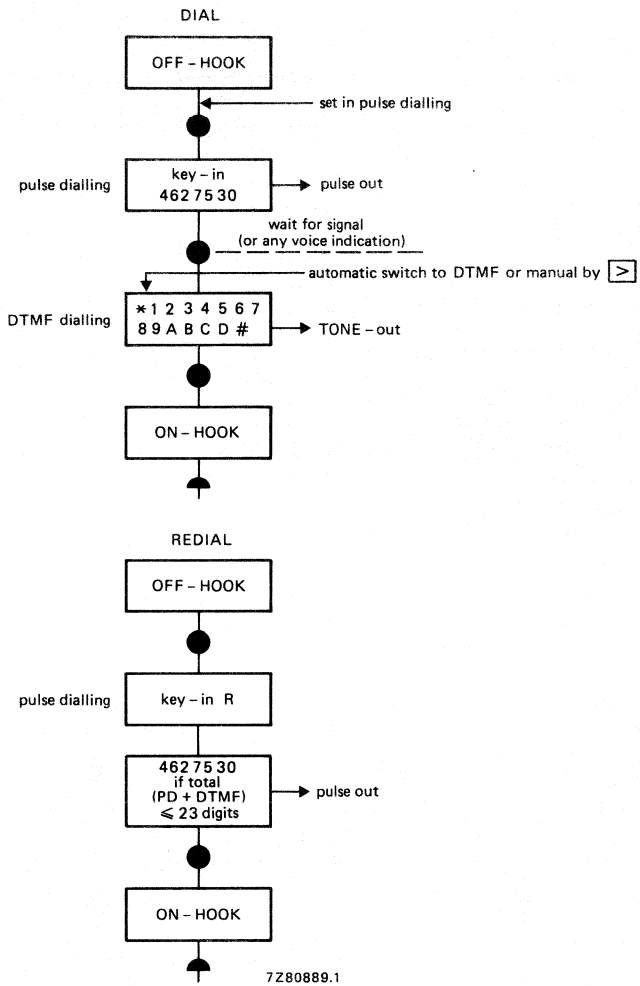


Fig. 9 PD/DTMF mixed mode dialling.

DIALLING PROCEDURES (continued)

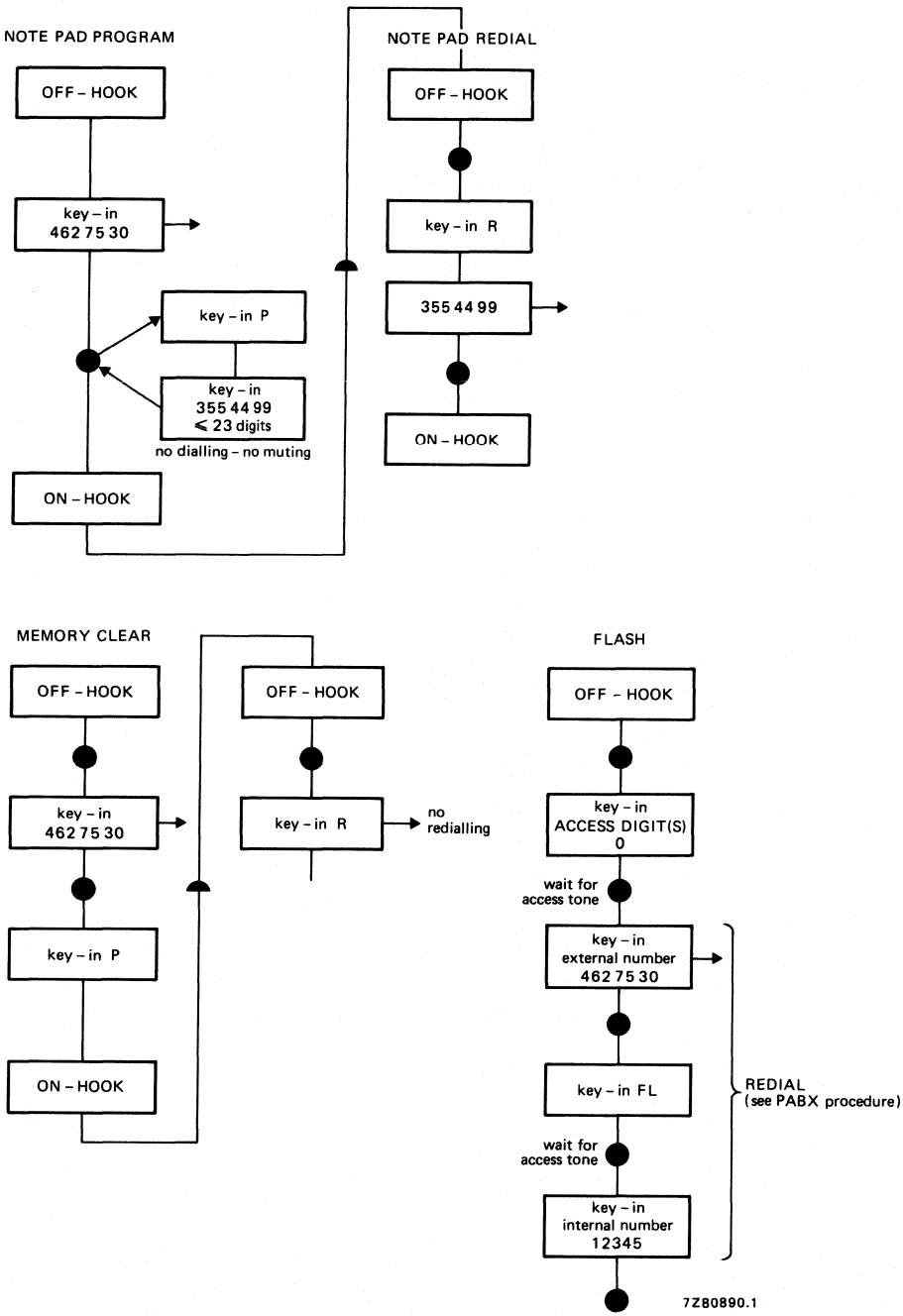


Fig. 10 Notepad, memory clear, flash; independent of dialling mode.

DEVELOPMENT DATA

TIMING

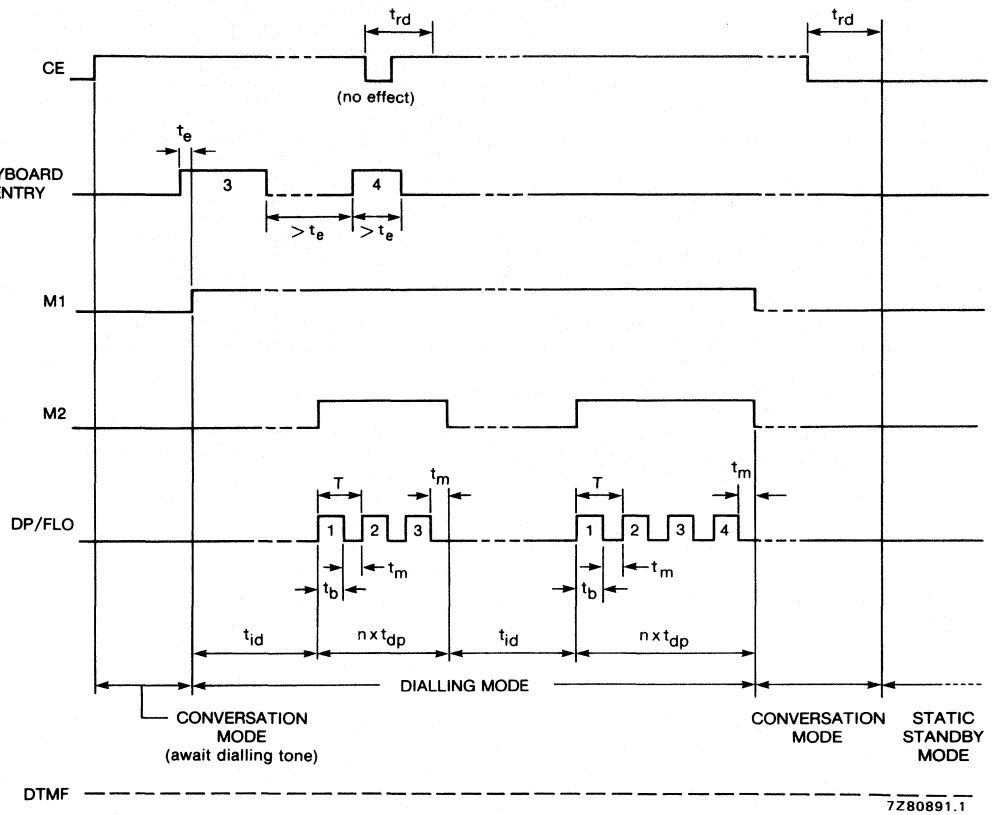


Fig. 11a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

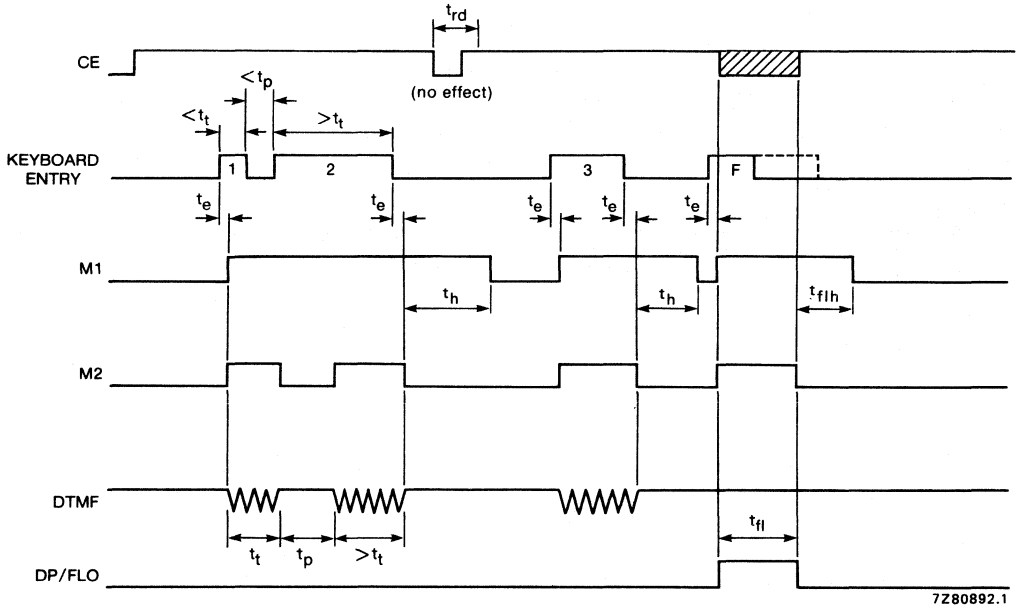


Fig. 11b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

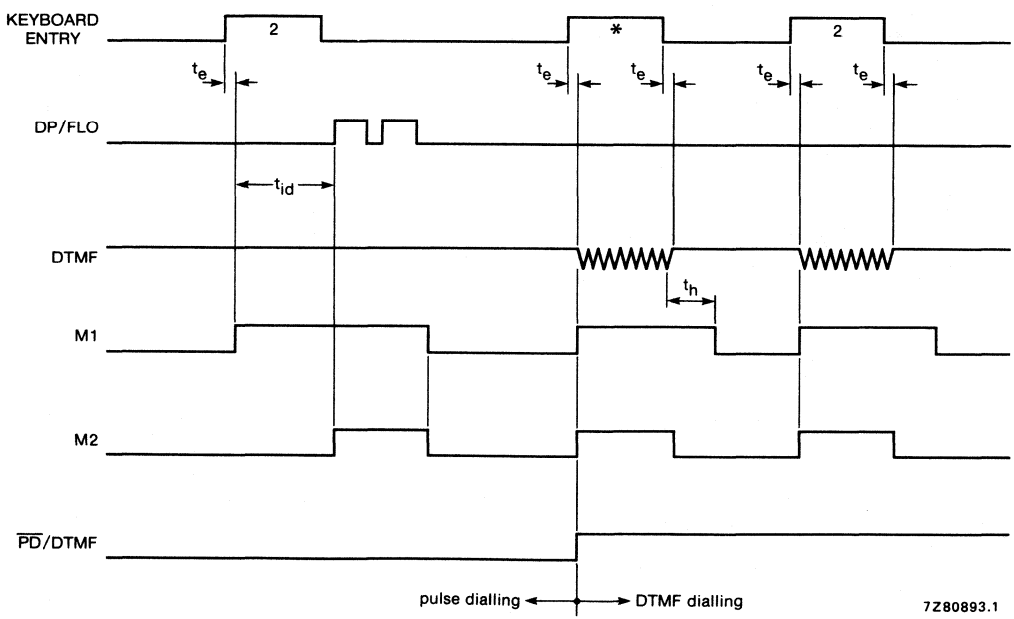


Fig. 11c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; mixed mode ($\overline{PD}$/DTMF open-circuit).

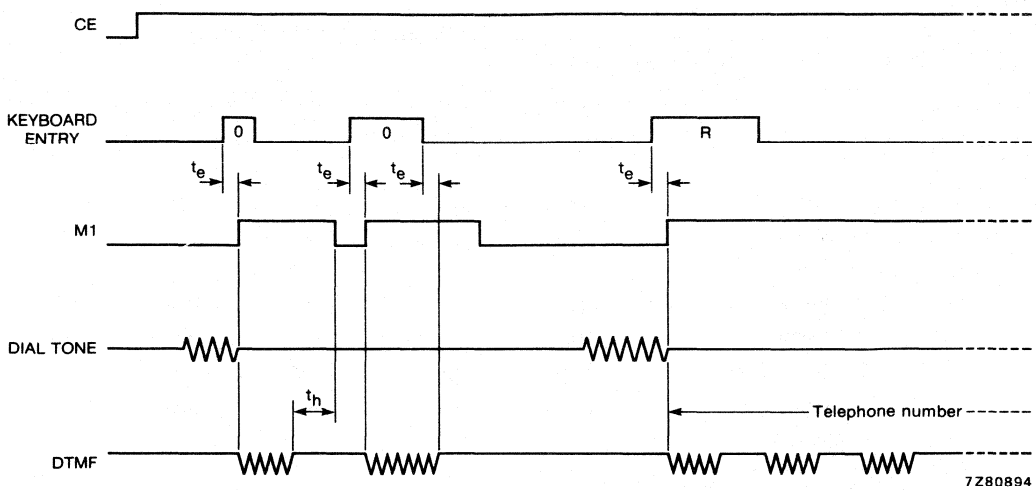


Fig. 12 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8 V
Supply current	I_{DD}	max.	50 mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10 mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8 V
Total power dissipation	P_{tot}	max.	300 mW
Power dissipation per output	P_O	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.;
T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	0,6	1,2	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON current	I_{ON}	–	–	45	μA
Keyboard OFF current	I_{OFF}	7,5	–	–	μA
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF, FLD	I_{OL}	0,7	–	–	mA
$\overline{PD}$/DTMF (note 2)	I_{OL}	–	1	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF	$-I_{OH}$	0,6	–	–	mA
$\overline{PD}$/DTMF (note 2)	$-I_{OH}$	–	1	–	mA
FLD (note 3)	$-I_{OH}$	–	100	–	nA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	–	160	–	ms
Confidence tone frequency	f_{ct}	–	330	–	Hz

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	$\frac{1}{2}V_{DD}$	−	V
Output impedance	$\lvert Z_O \rvert$	−	0,1	0,5	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 4)	THD	−	−25	−	dB
Transmission and pause time					
Manual dialling	t_t, t_p	68	−	−	ms
Redialling	t_t, t_p	68	70	72	ms
Flash pulse duration	t_{FL}	98	100	102	ms
Flash hold-over time	t_{flh}	31	33	34	ms
Hold-over time (muting on M1)	t_h	78	80	81	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	828	840	844	ms
Break time (note 5)	t_b	65	67	68	ms
Make time (note 5)	t_m	31	33	34	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; $V_{OH} = V_{SS}$.
4. Related to the level of the LOW group frequency component (CEPT CS 203).
5. Mark-to-space ratio 2 : 1.

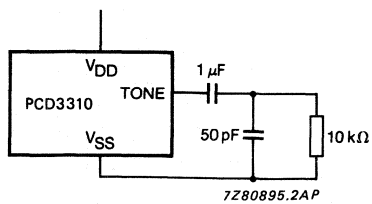
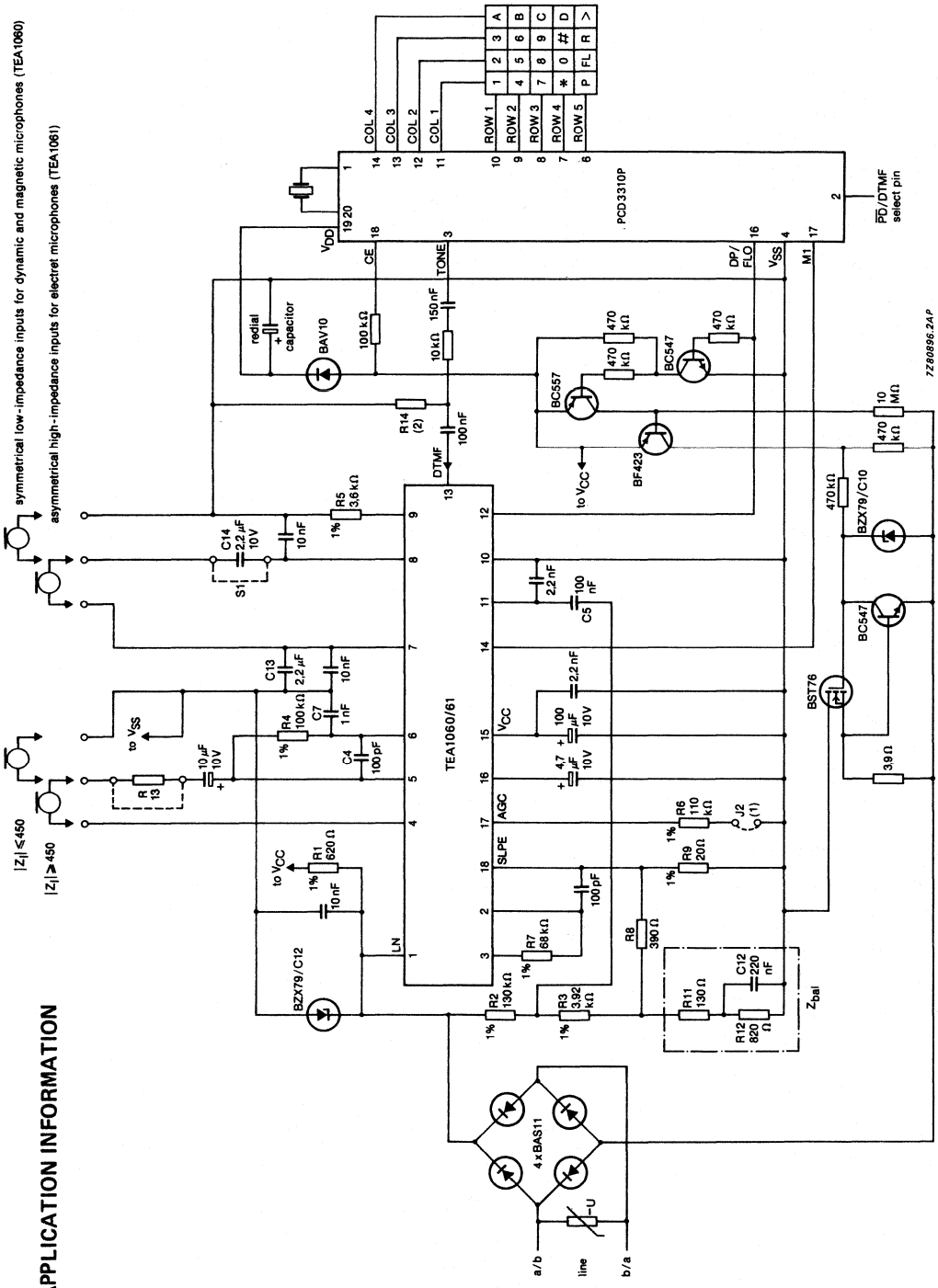


Fig. 13 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060.

Fig. 14 Application diagram of the full electronic basic telephone set.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD3310A is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed mode dialling; start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  - manual dialling — minimum duration for bursts and pauses
  - redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents at V_{DD} = 3,0 V			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3310AP: 20-lead DIL; plastic (SOT146).
PCD3310AT: 28-lead mini-pack; plastic (SO28; SOT136A).

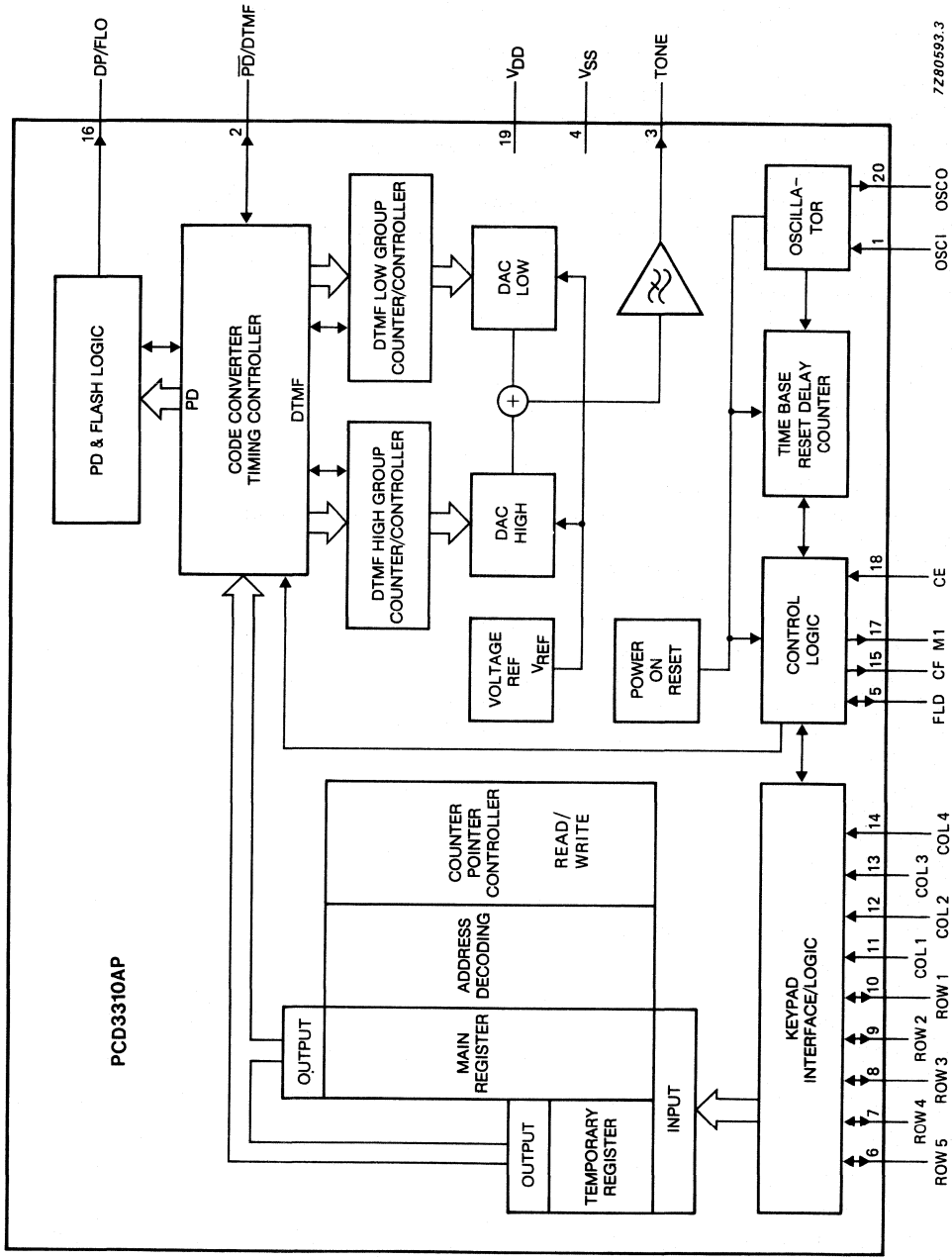


Fig. 1 Block diagram; PCD3310AP.

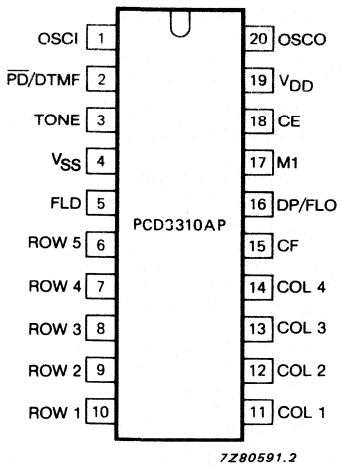


Fig. 2 Pinning diagram; PCD3310AP.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	FLD	flash duration control input/output
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	COL 4	
15	CF	330 Hz confidence tone output to provide audible feedback of key entries
16	DP/FLO	dialling pulse and flash output
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA

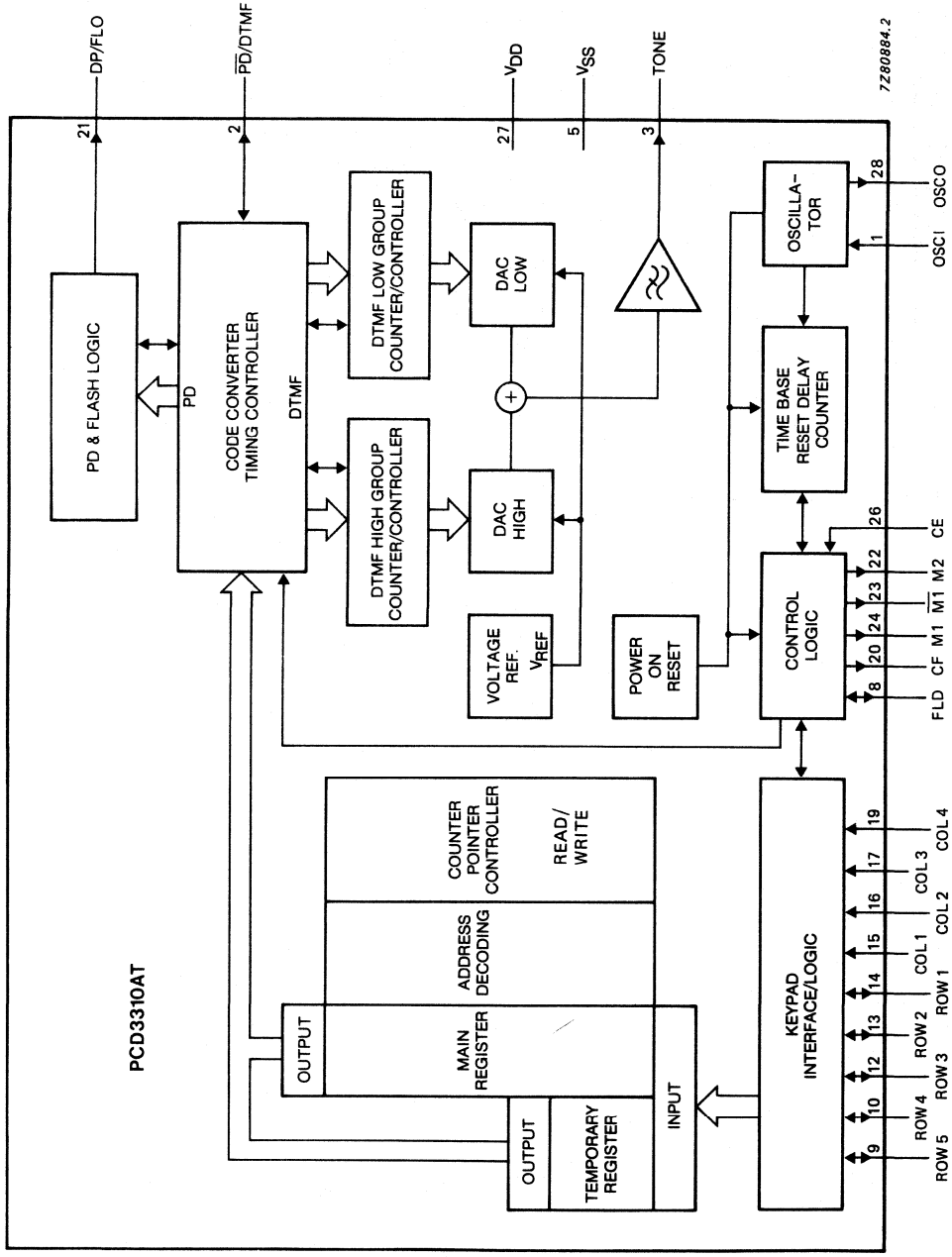


Fig. 3 Block diagram; PCD3310AT.

Note: Pins 4, 6, 7, 11, 18 and 25 are not connected.

DEVELOPMENT DATA

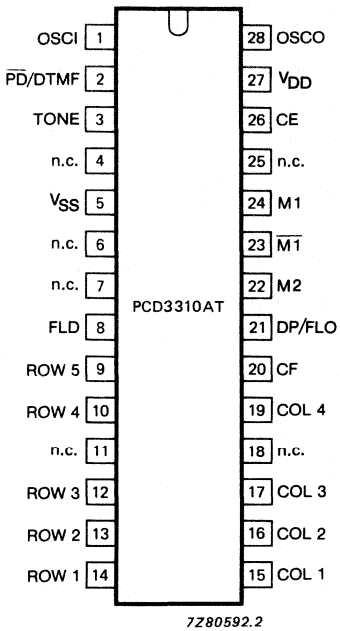


Fig. 4 Pinning diagram for PCD3310AT.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	n.c.	not connected
5	V_{SS}	negative supply
6	n.c.	not connected
7	n.c.	not connected
8	FLD	flash duration control input/output
9	ROW 5	scanning row keyboard input/outputs
10	ROW 4	
11	n.c.	not connected
12	ROW 3	scanning row keyboard input/outputs
13	ROW 2	
14	ROW 1	
15	COL 1	sense column keyboard inputs with internal pull-ups
16	COL 2	
17	COL 3	
18	n.c.	not connected
19	COL 4	sense column keyboard input with internal pull-up
20	CF	330 Hz confidence tone output to provide audible feedback of key entries
21	DP/FLO	dialling pulse and flash output
22	M2	strobe; active HIGH during transmission
23	$\overline{M1}$	inverted mute output
24	M1	muting output
25	n.c.	not connected
26	CE	chip enable input
27	V_{DD}	positive supply
28	OSCO	oscillator output

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on-reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD3310A for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary Write Address Counter (TWAC) which point to the last entered digit (see Fig. 7). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 11a, Fig. 11b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric (A, B, C, D, *, #) or the ">" key is activated. Then the circuit changes over to DTMF dialling and remains there until FL is activated or, after a static standby condition, CE is re-activated.

A connection between $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the PCD3310A are directly connected to the keyboard as shown in Fig. 5.

All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 11. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

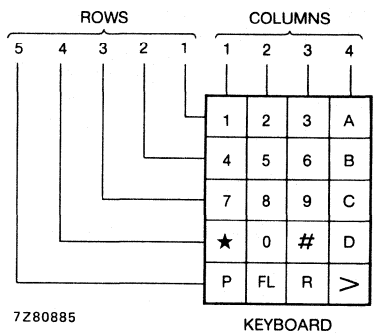


Fig. 5 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric pushbuttons (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, FL and R.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In mixed mode all key entries are valid and executed accordingly.

FUNCTIONAL DESCRIPTION (continued)

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling mode. Pressing the FL pushbutton will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig. 6).

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

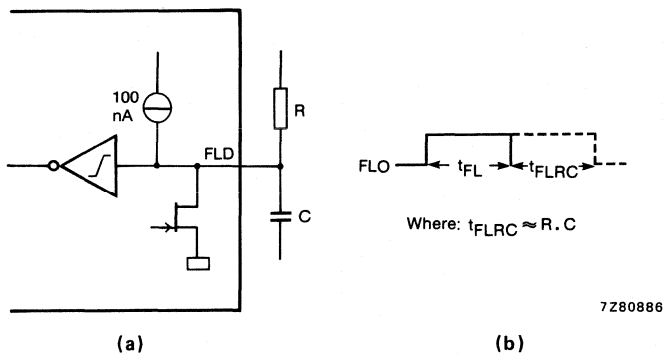


Fig. 6 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+ 0,13	+ 0,90
row 2	770	770,46	+ 0,06	+ 0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+ 0,24	+ 2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+ 0,42	+ 5,66
col 3	1477	1482,21	+ 0,35	+ 5,21
col 4	1633	1638,24	+ 0,32	+ 5,25

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310AP it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling.

Confidence tone output (CF)

When any of the keys are activated a square-wave is generated and appears at this output to serve as an acoustic feedback for the user.

DIALLING PROCEDURES (see also Figs 8, 9 and 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 7). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated write address counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 11. Each entry is tested for validity before being deposited in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD3310A is in the conversation mode.

If "R" is the first keyboard entry the circuit starts redialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the redialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for redialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, redialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

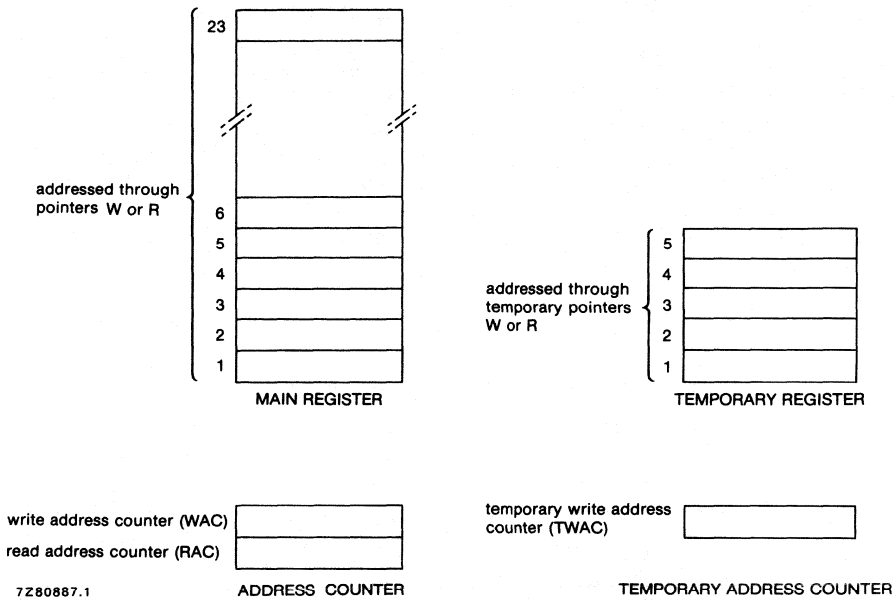
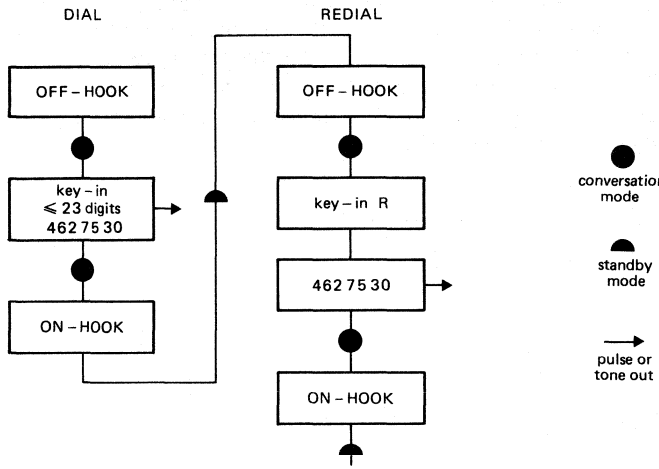


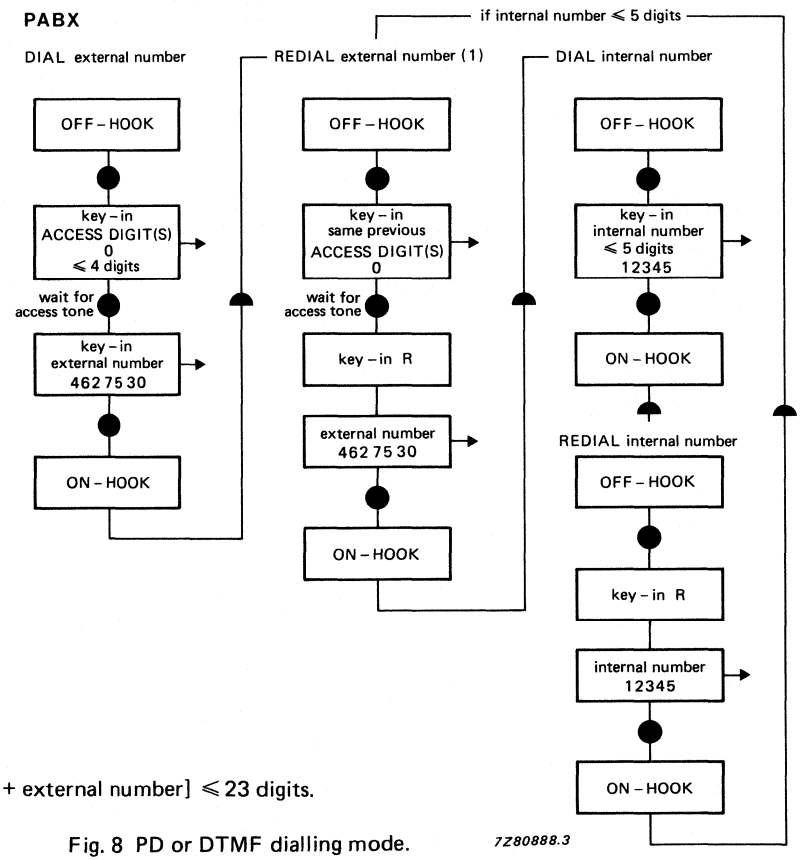
Fig. 7 Memory map.

DIALLING PROCEDURES (continued)

PUBLIC EXCHANGE



PABX



(1) If [access digit(s) + external number] ⩽ 23 digits.

Fig. 8 PD or DTMF dialling mode.

7Z80888.3

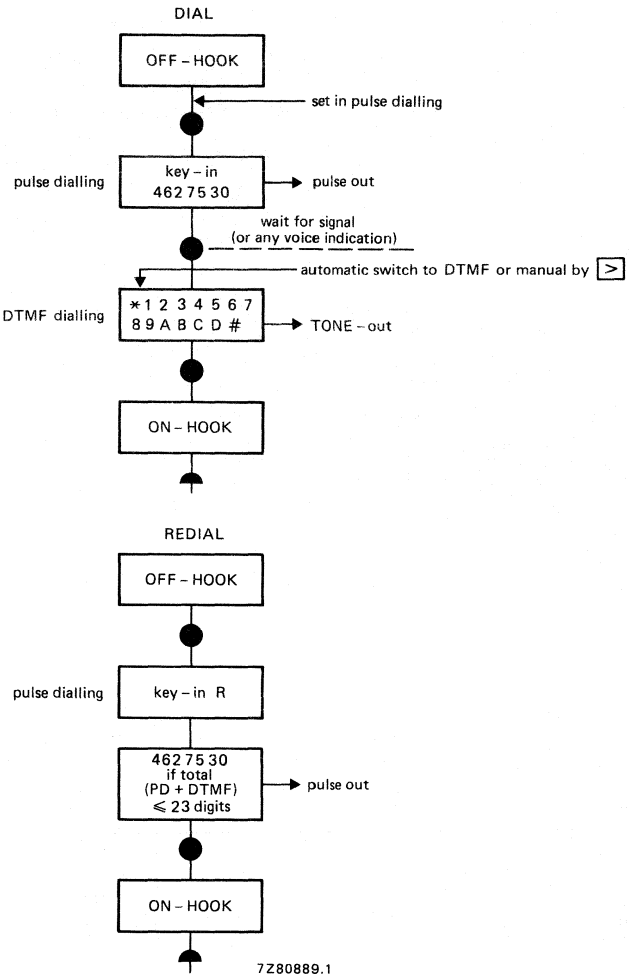


Fig. 9 PD/DTMF mixed mode dialling.

DIALLING PROCEDURES (continued)

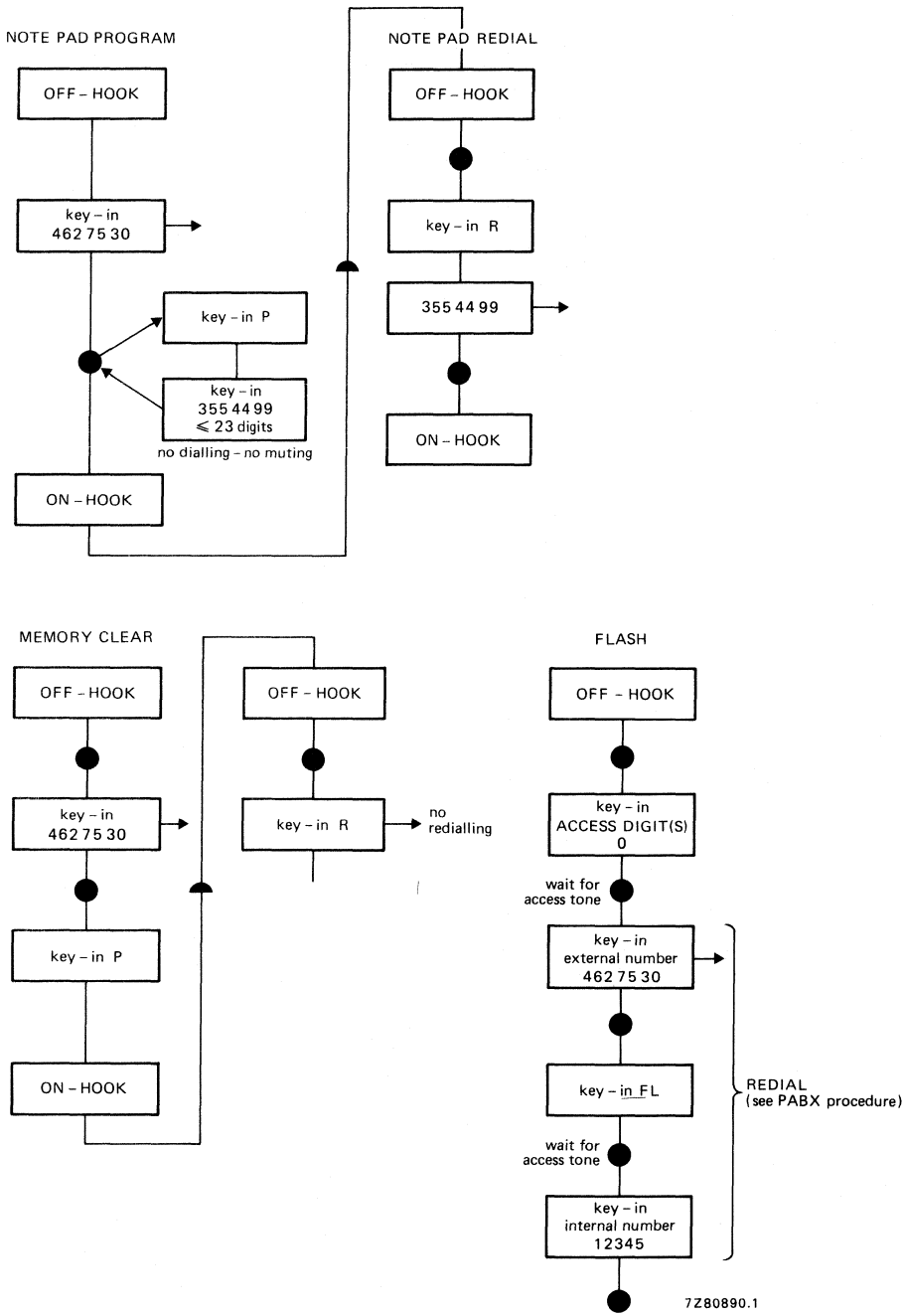


Fig. 10 Notepad, memory clear, flash; independent of dialling mode.

DEVELOPMENT DATA

TIMING

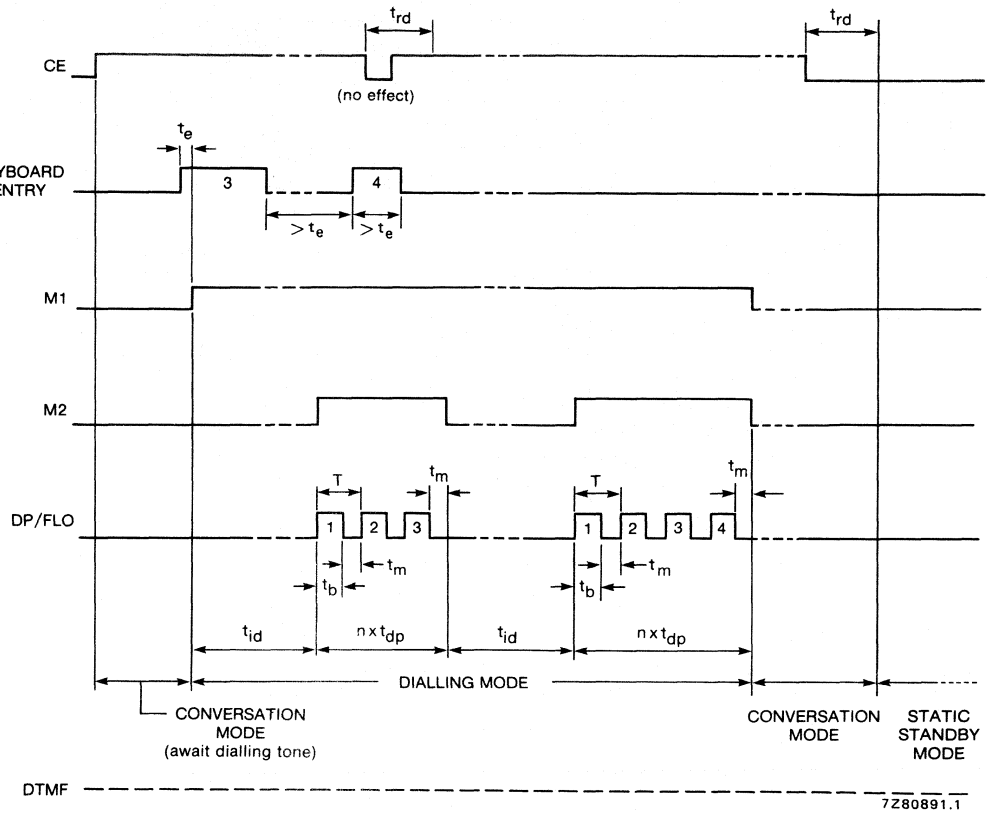


Fig. 11a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

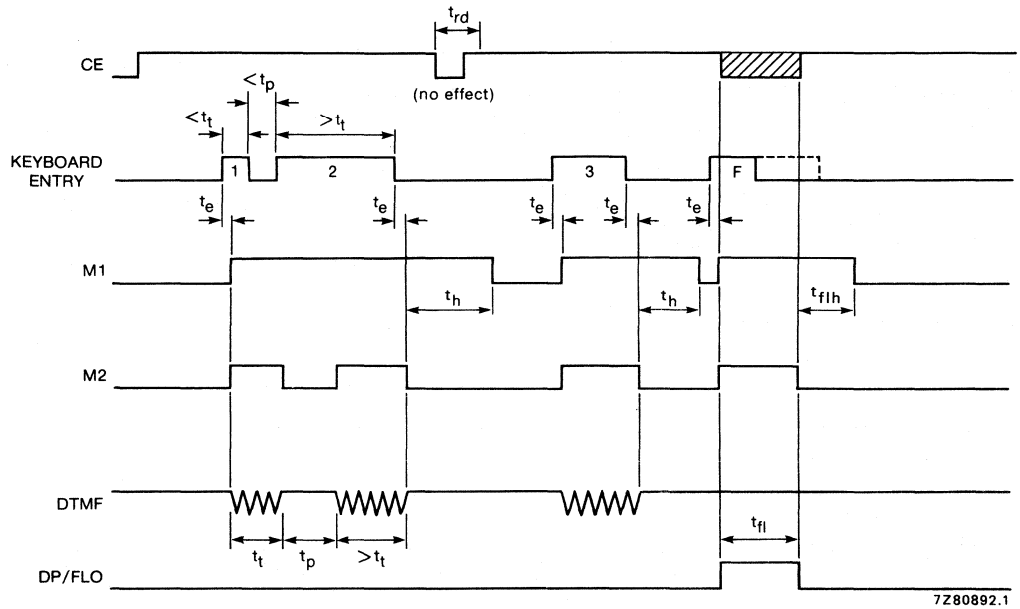


Fig. 11b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

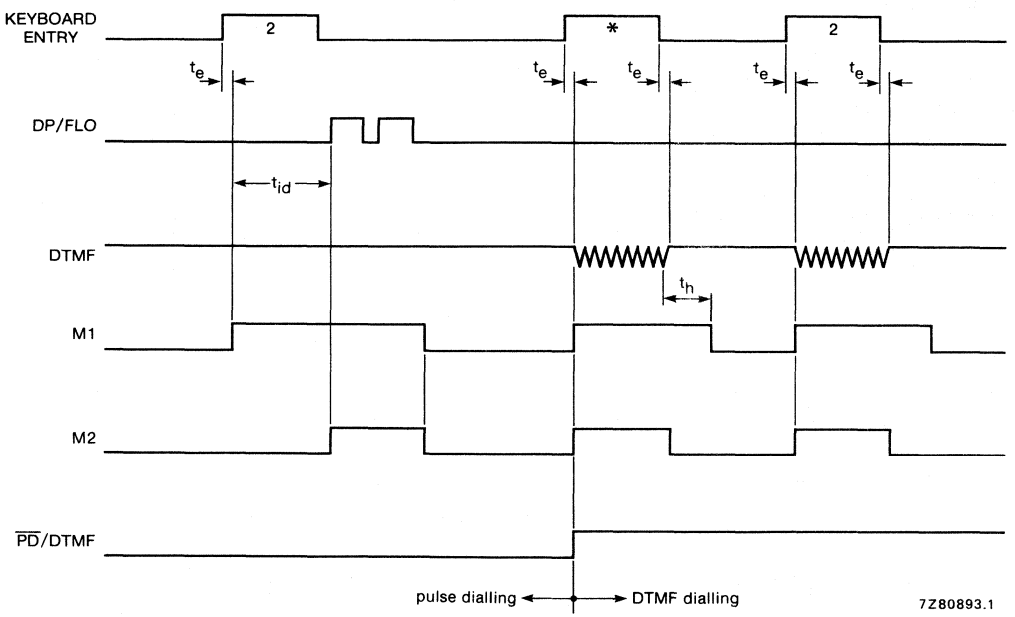


Fig. 11c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; mixed mode ($\overline{PD}$/DTMF open-circuit).

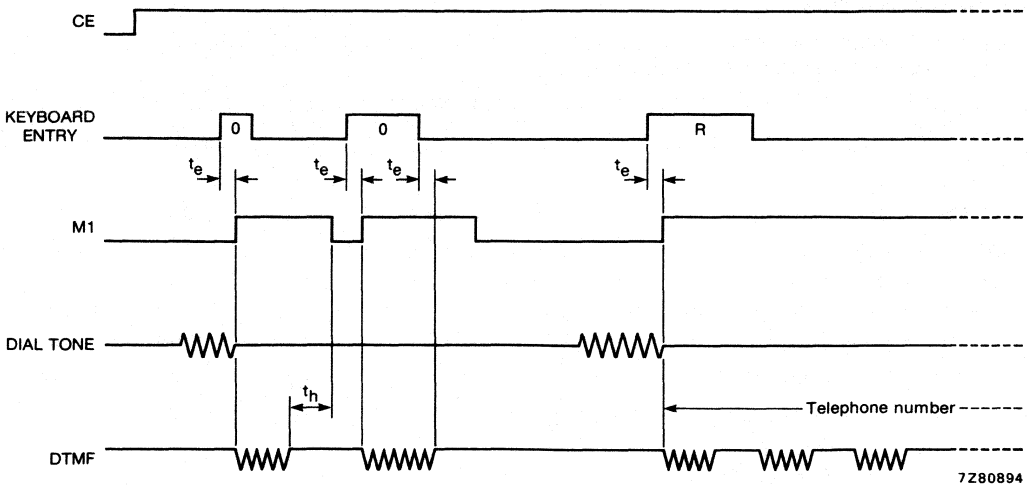


Fig. 12 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	0,6	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON current	I_{ON}	–	–	45	μA
Keyboard OFF current	I_{OFF}	7,5	–	–	μA
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF, FLD	I_{OL}	0,7	–	–	mA
$\overline{PD}$/DTMF (note 2)	I_{OL}	–	1	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF	$-I_{OH}$	0,6	–	–	mA
$\overline{PD}$/DTMF (note 2)	$-I_{OH}$	–	1	–	mA
FLD (note 3)	$-I_{OH}$	–	100	–	nA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	–	160	–	ms
Confidence tone frequency	f_{ct}	–	330	–	Hz

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	—	+ 0,6	%
DC voltage level	V_{DC}	—	$\frac{1}{2}V_{DD}$	—	V
Output impedance	$\lvert Z_O \rvert$	—	0,1	0,5	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 4)	THD	—	−25	—	dB
Transmission and pause time					
Manual dialling	t_t, t_p	68	—	—	ms
Redialling	t_t, t_p	68	70	72	ms
Flash pulse duration	t_{FL}	98	100	102	ms
Flash hold-over time	t_{flh}	31	33	34	ms
Hold-over time (muting on M1)	t_h	78	80	81	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	828	840	844	ms
Break time (note 5)	t_b	—	60	—	ms
Make time (note 5)	t_m	—	40	—	ms

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; $V_{OH} = V_{SS}$.
4. Related to the level of the LOW group frequency component (CEPT CS 203).
5. Mark-to-space ratio 3 : 2.

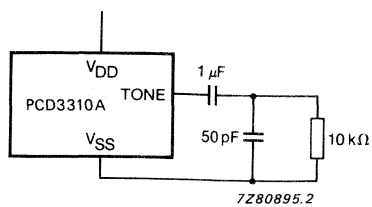
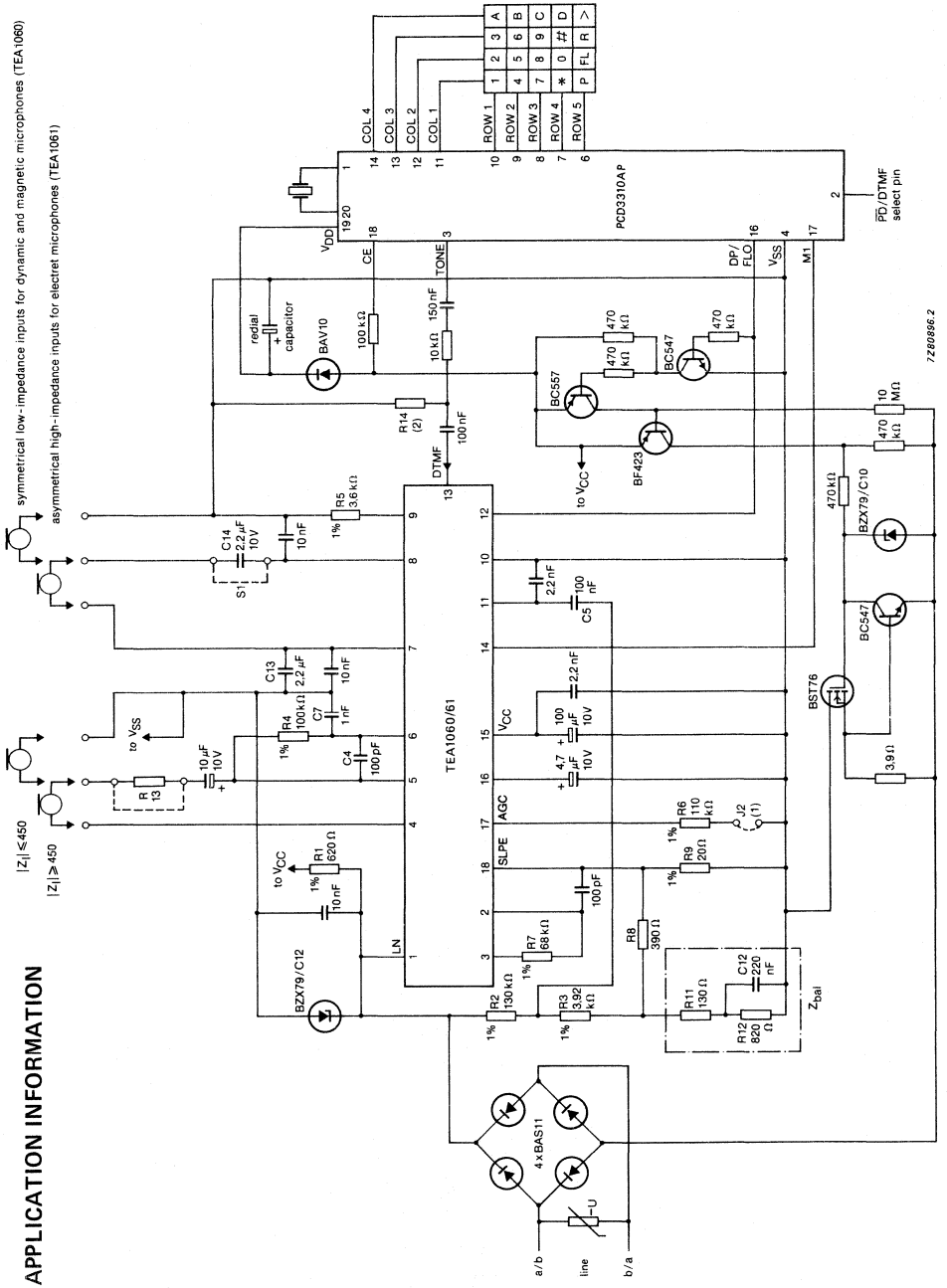


Fig. 13 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.

Fig. 14 Application diagram of the full electronic basic telephone set.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD3310C is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed mode dialling; start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  manual dialling — minimum duration for bursts and pauses
  redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents at V_{DD} = 3,0 V			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 1,2	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3310CP: 20-lead DIL; plastic (SOT146).
PCD3310CT: 28-lead mini-pack; plastic (SO28; SOT136A).

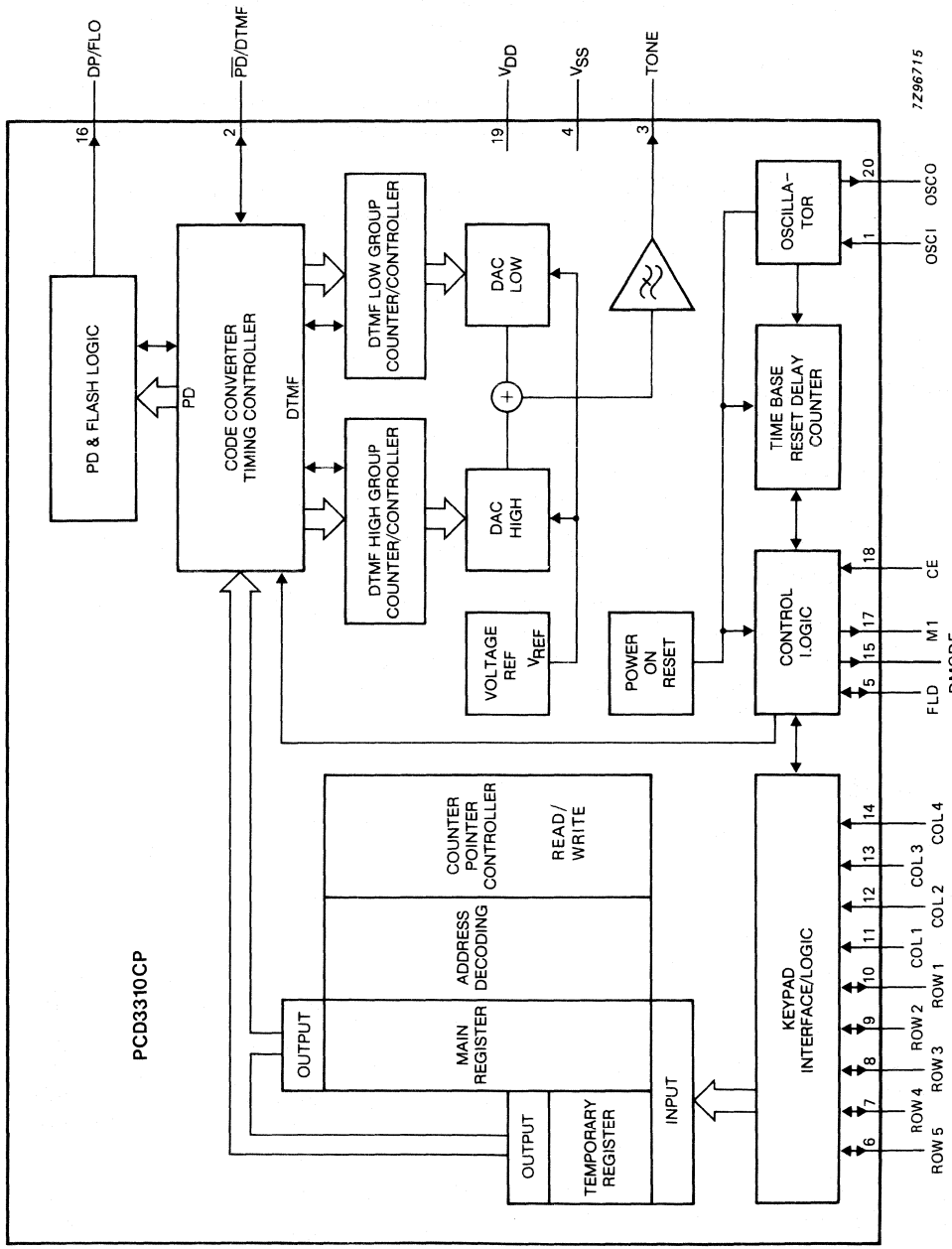


Fig. 1 Block diagram; PCD3310CP.

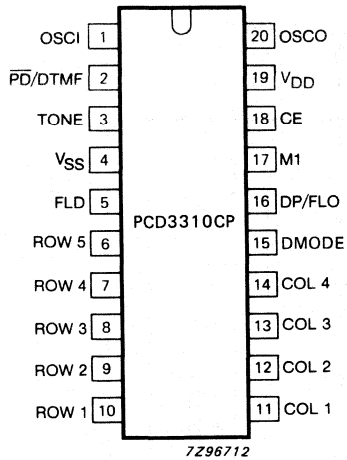


Fig. 2 Pinning diagram; PCD3310CP.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	FLD	flash duration control input/output
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	COL 4	
15	DMODE	dialling mode output
16	DP/FLO	dialling pulse and flash output
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA

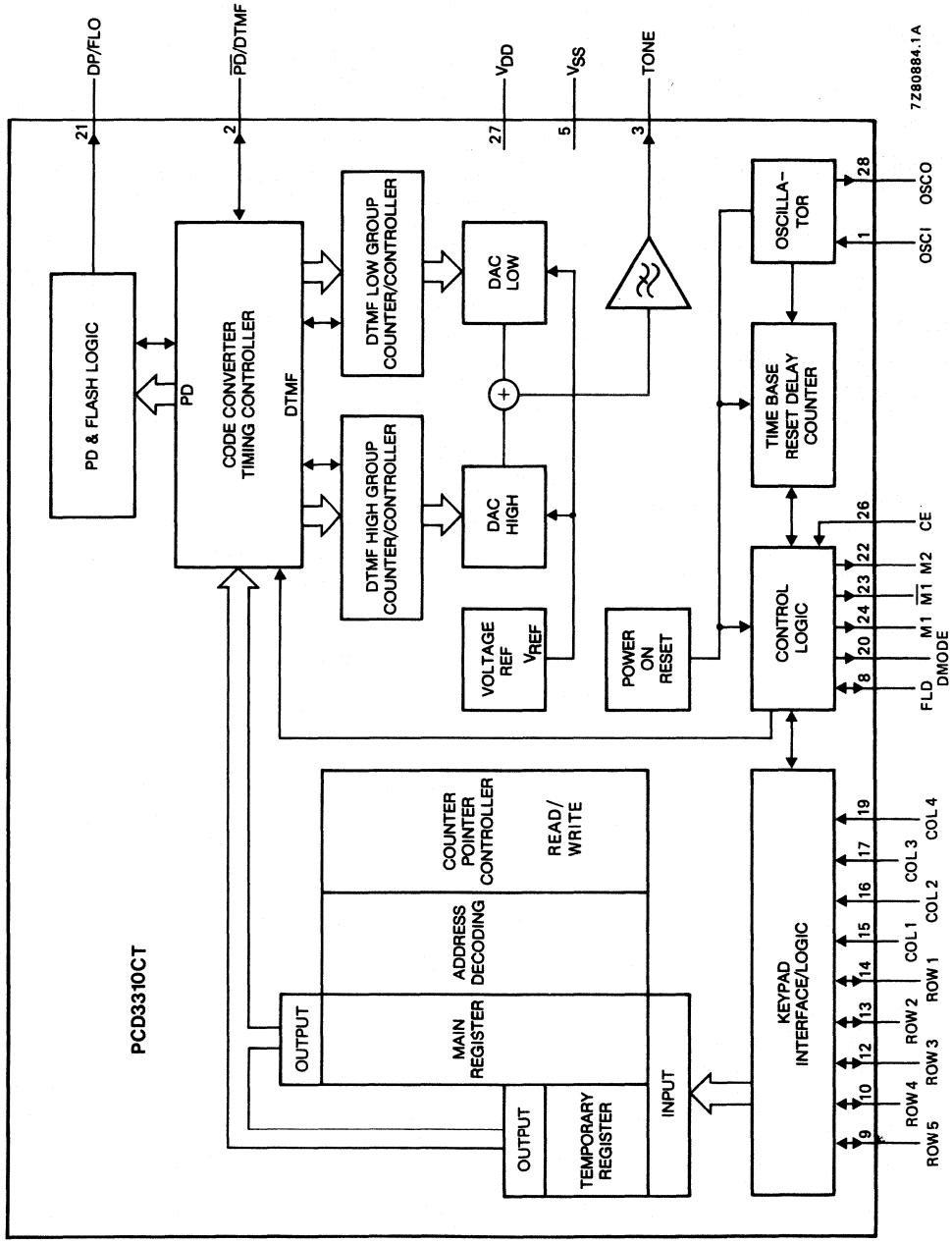


Fig. 3 Block diagram; PCD3310CT.

Note: Pins 4, 6, 7, 11, 18 and 25 are not connected.

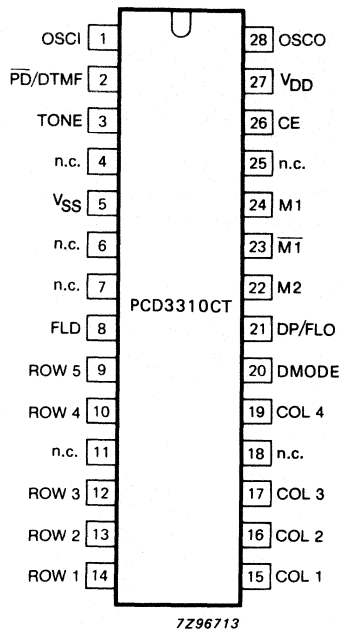


Fig. 4 Pinning diagram for PCD3310CT.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	n.c.	not connected
5	V_{SS}	negative supply
6	n.c.	not connected
7	n.c.	not connected
8	FLD	flash duration control input/output
9	ROW 5	scanning row keyboard input/outputs
10	ROW 4	
11	n.c.	not connected
12	ROW 3	scanning row keyboard input/outputs
13	ROW 2	
14	ROW 1	
15	COL 1	sense column keyboard inputs with internal pull-ups
16	COL 2	
17	COL 3	
18	n.c.	not connected
19	COL 4	sense column keyboard input with internal pull-up
20	DMODE	dialling mode output
21	DP/FLO	dialling pulse and flash output
22	M2	strobe; active HIGH during transmission
23	$\overline{M1}$	inverted mute output
24	M1	muting output
25	n.c.	not connected
26	CE	chip enable input
27	V_{DD}	positive supply
28	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on-reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD3310C for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary Write Address Counter (TWAC) which point to the last entered digit (see Fig. 7). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 11a, Fig. 11b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric (A, B, C, D, *, #) or the ">" key is activated. Then the circuit changes over to DTMF dialling and remains there until FL is activated or, after a static standby condition, CE is re-activated.

A connection between $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the PCD3310C are directly connected to the keyboard as shown in Fig. 5.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 11. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

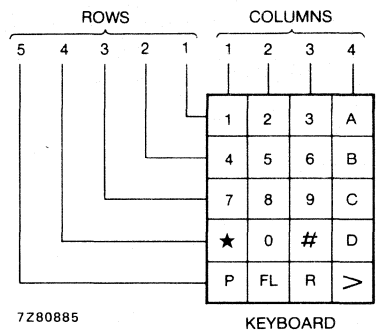


Fig. 5 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric pushbuttons (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, FL and R.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In mixed mode all key entries are valid and executed accordingly.

FUNCTIONAL DESCRIPTION (continued)

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling mode. Pressing the FL pushbutton will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig. 6).

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

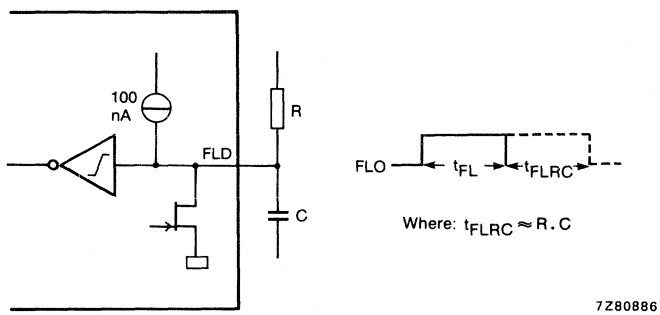


Fig. 6 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+ 0,13	+ 0,90
row 2	770	770,46	+ 0,06	+ 0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+ 0,24	+ 2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+ 0,42	+ 5,66
col 3	1477	1482,21	+ 0,35	+ 5,21
col 4	1633	1638,24	+ 0,32	+ 5,25

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310CP it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling.

Confidence tone output (CF)

When any of the keys are activated a square-wave is generated and appears at this output to serve as an acoustic feedback for the user.

Dialling mode output (DMODE)

The DMODE output represents the actual dialling status of the dialler. In pulse dialling mode the output is LOW and in DTMF mode the output is HIGH.

DIALLING PROCEDURES (see also Figs 8, 9 and 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 7). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated write address counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 11. Each entry is tested for validity before being deposited in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD3310C is in the conversation mode.

If "R" is the first keyboard entry the circuit starts redialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the redialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for redialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, redialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

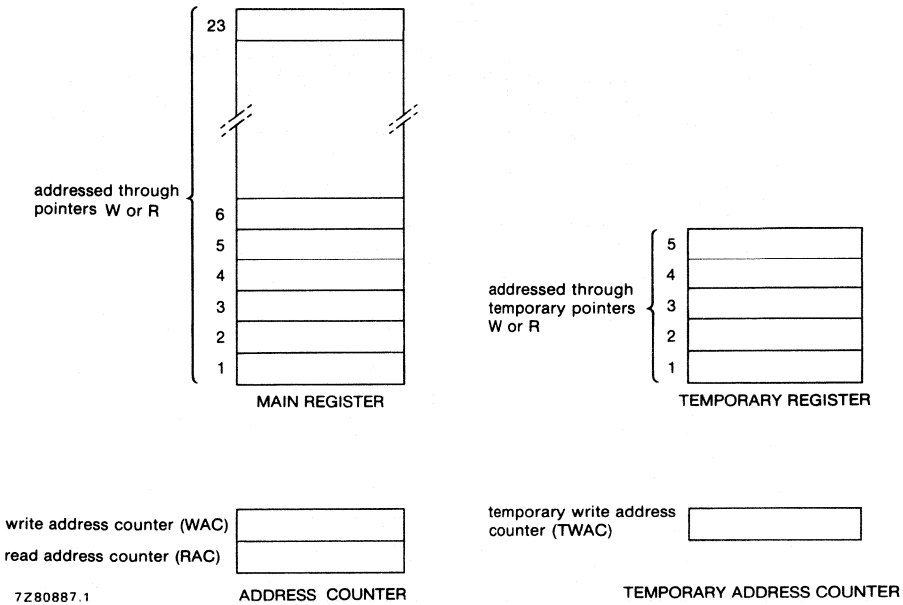
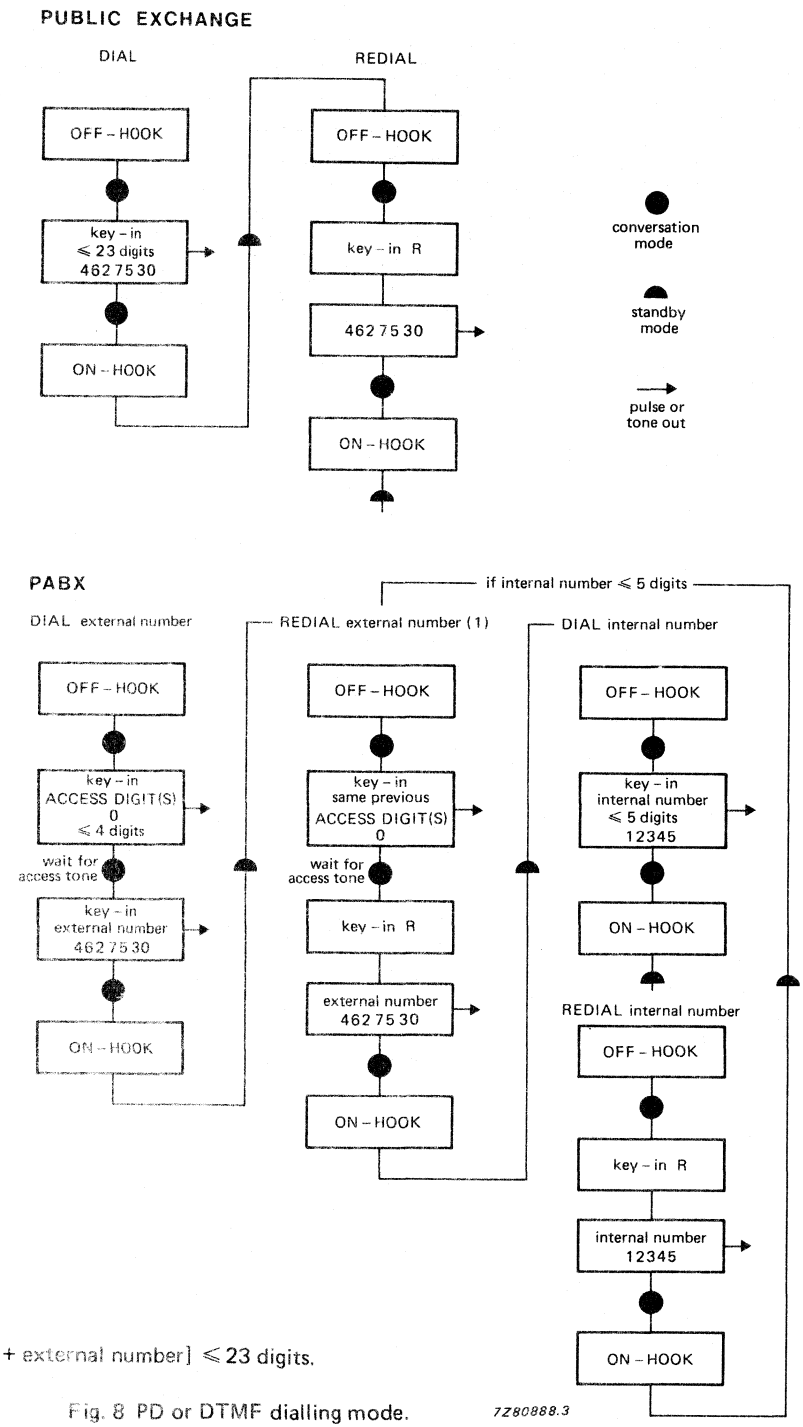


Fig. 7 Program memory map.

DIALLING PROCEDURES (continued)



(1) If [access digit(s) + external number] ≤ 23 digits.

Fig. 8 PD or DTMF dialling mode.

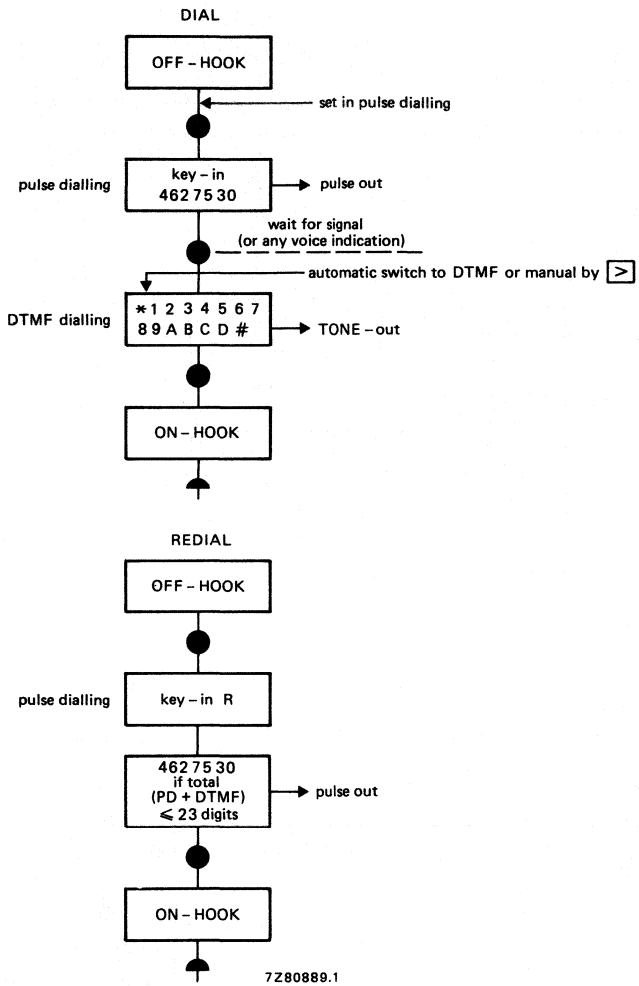


Fig. 9 PD/DTMF mixed mode dialling.

DIALLING PROCEDURES (continued)

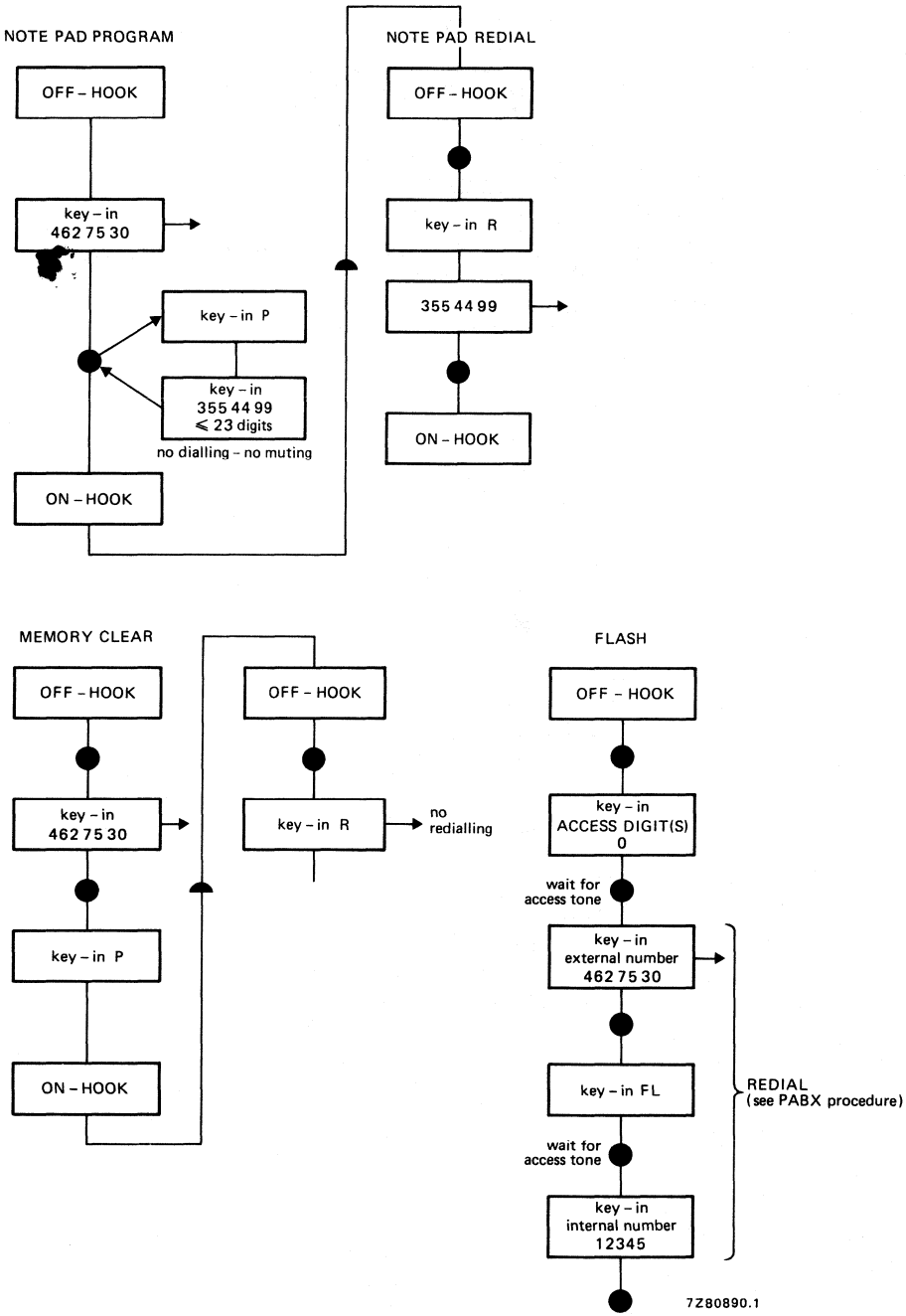


Fig. 10 Notepad, memory clear, flash; independent of dialling mode.

DEVELOPMENT DATA

TIMING

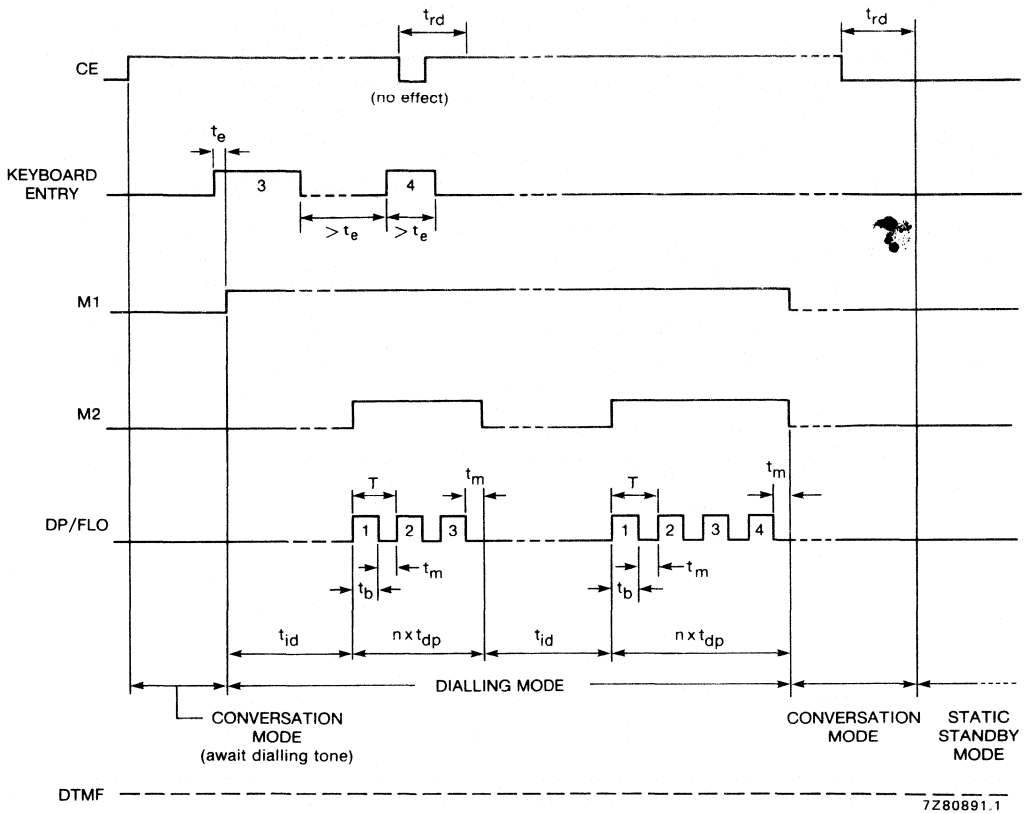


Fig. 11a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

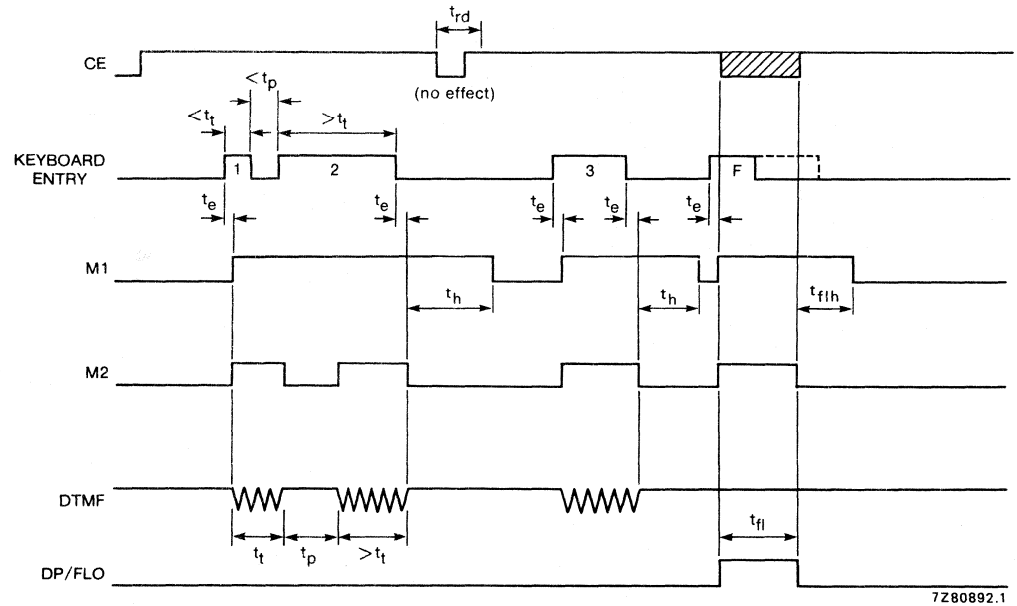


Fig. 11b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

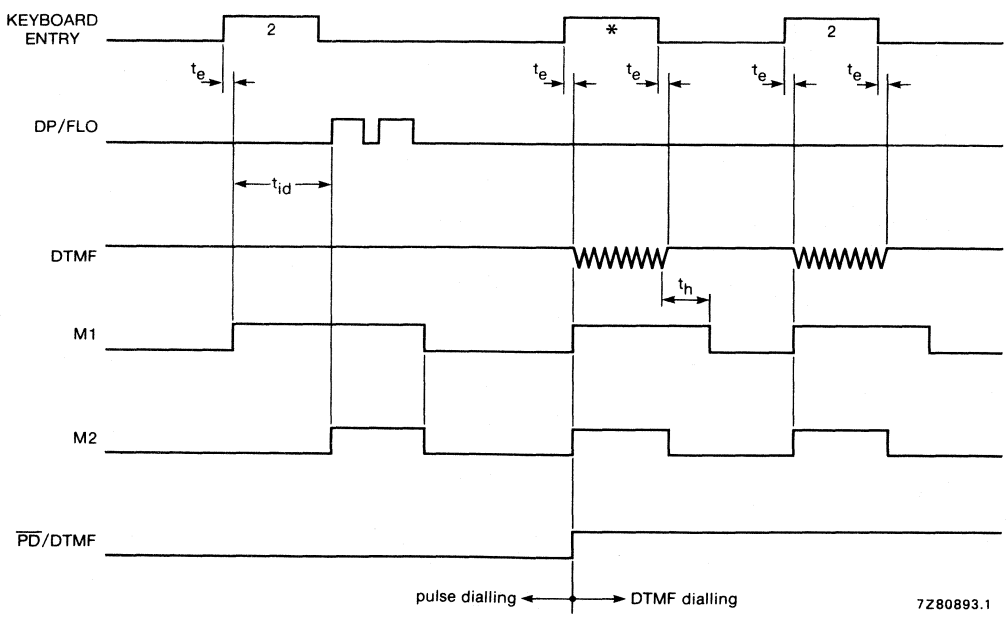


Fig. 11c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; mixed mode ($\overline{PD}$/DTMF open-circuit).

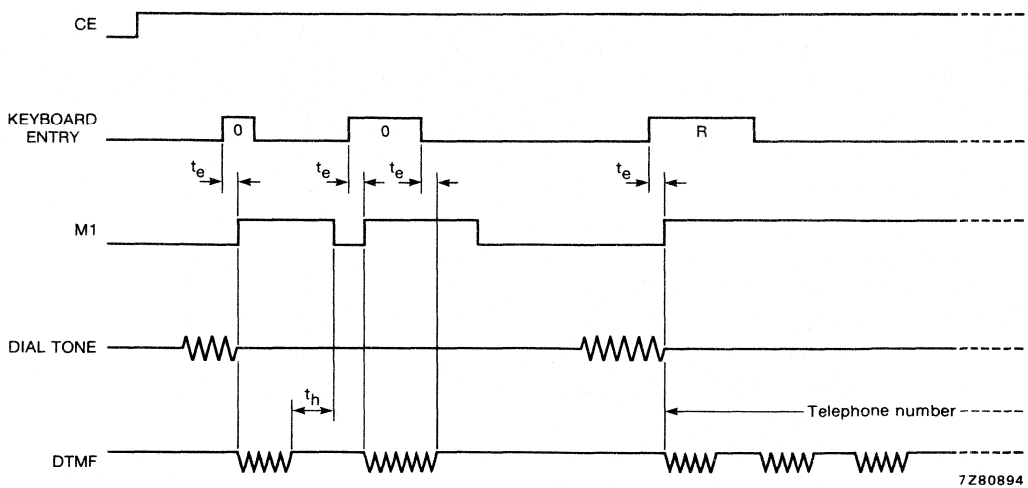


Fig. 12 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8 V
Supply current	I_{DD}	max.	50 mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10 mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8 V
Total power dissipation	P_{tot}	max.	300 mW
Power dissipation per output	P_O	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	0,6	1,2	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON current	I_{ON}	–	–	45	μA
Keyboard OFF current	I_{OFF}	7,5	–	–	μA
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF, FLD	I_{OL}	0,7	–	–	mA
$\overline{PD}$/DTMF (note 2)	I_{OL}	–	1	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, $\overline{M1}$, M2, DP/FLO, CF	$-I_{OH}$	0,6	–	–	mA
$\overline{PD}$/DTMF (note 2)	$-I_{OH}$	–	1	–	mA
FLD (note 3)	$-I_{OH}$	–	100	–	nA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	–	160	–	ms
Confidence tone frequency	f_{ct}	–	330	–	Hz

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
D.C. voltage level	V_{DC}	−	$\frac{1}{2}V_{DD}$	−	V
Output impedance	$\lvert Z_O \rvert$	−	0,1	0,5	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 4)	THD	−	−25	−	dB
Transmission and pause time					
Manual dialling	t_t, t_p	68	−	−	ms
Redialling	t_t, t_p	68	70	72	ms
Flash pulse duration	t_{FL}	98	100	102	ms
Flash hold-over time	t_{flh}	31	33	34	ms
Hold-over time (muting on M1)	t_h	78	80	81	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	828	840	844	ms
Break time (note 5)	t_b	65	67	68	ms
Make time (note 5)	t_m	31	33	34	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; $V_{OH} = V_{SS}$.
4. Related to the level of the LOW group frequency component (CEPT CS 203).
5. Mark-to-space ratio 2 : 1.

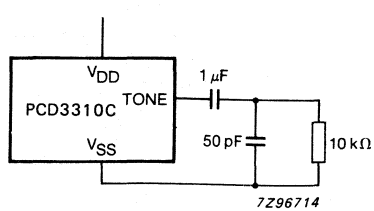
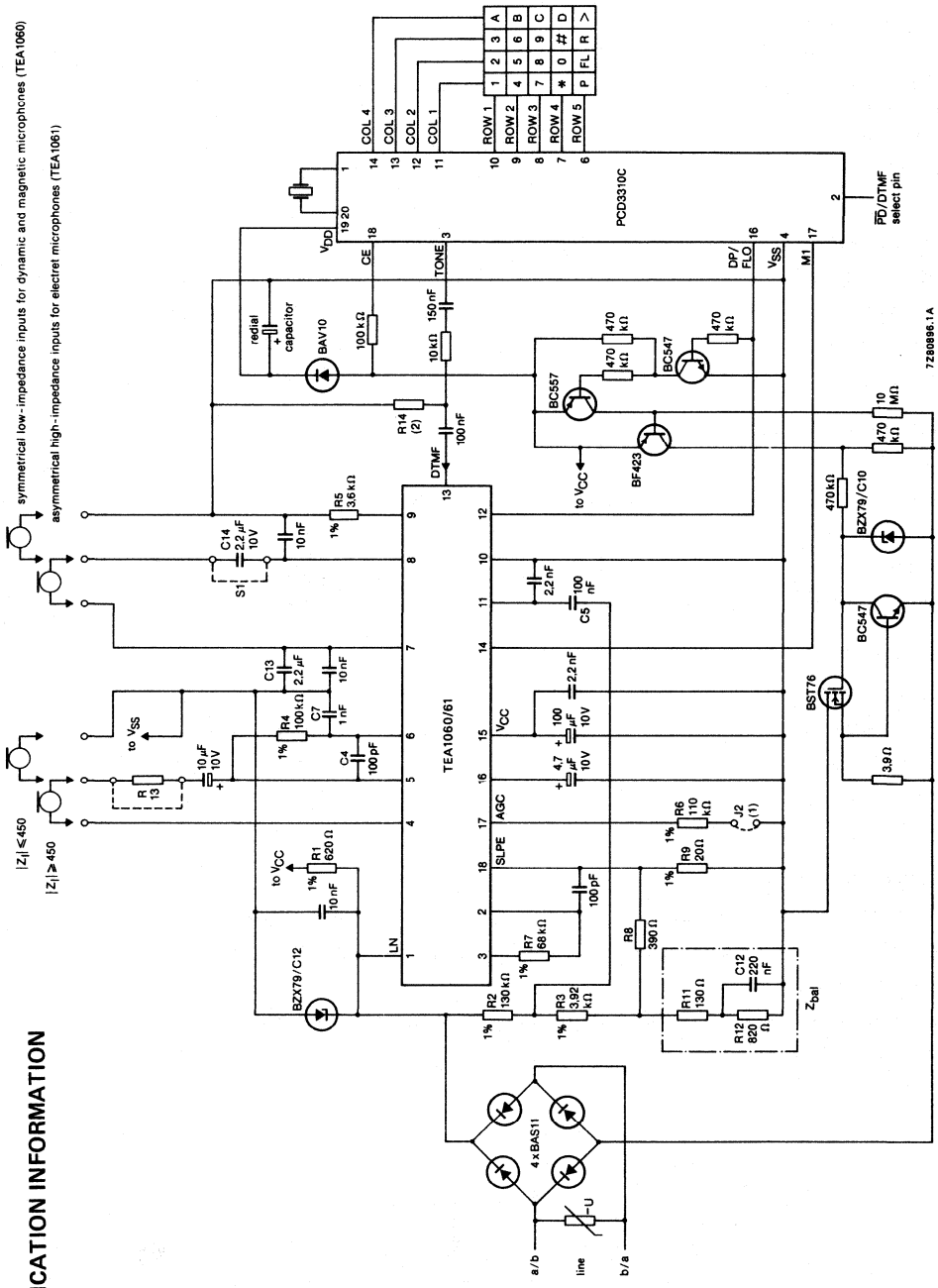


Fig. 13 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060.

Fig. 14 Application diagram of the full electronic basic telephone set.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT27).
PCD3311T: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312P: 8-lead DIL; plastic (SOT97).
PCD3312T: 8-lead mini-pack; plastic (SO8L; SOT176).

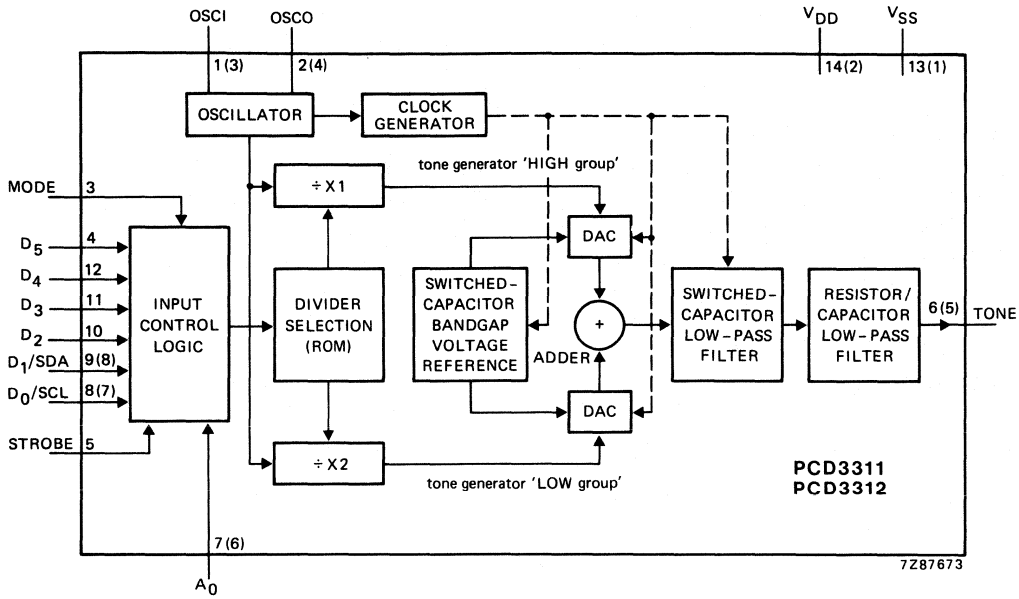


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

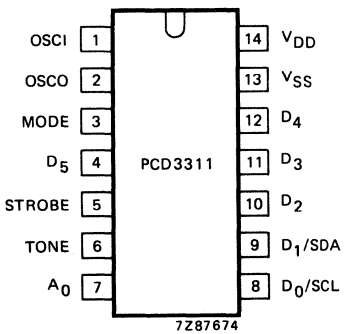


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

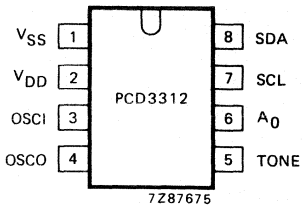


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

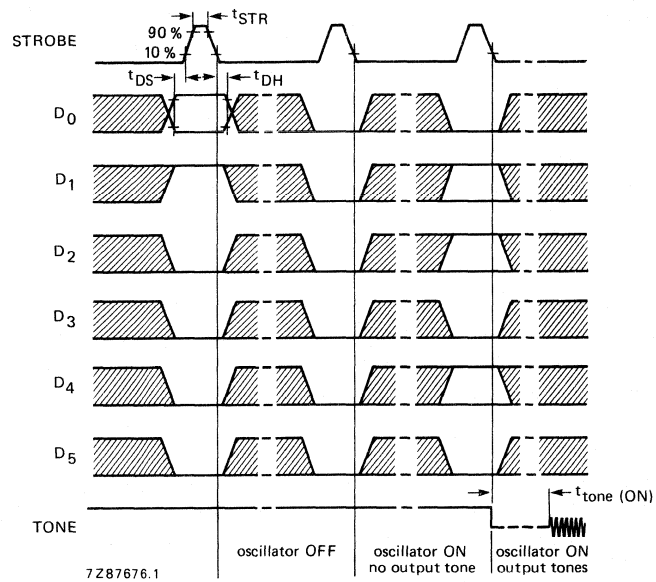


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I^2C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I^2C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

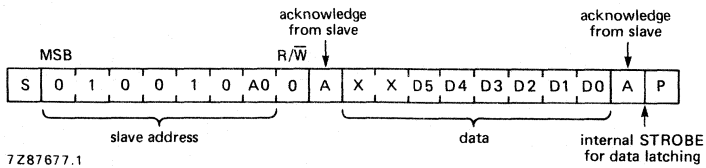


Fig. 5 I^2C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

DEVELOPMENT DATA

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

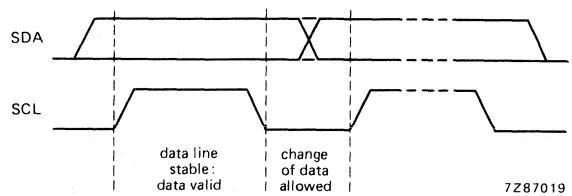


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

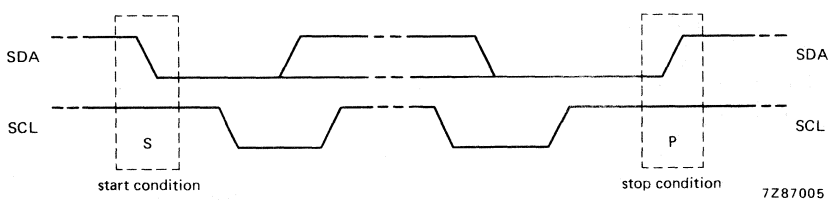


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

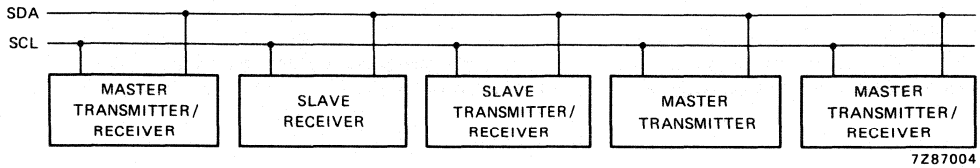


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

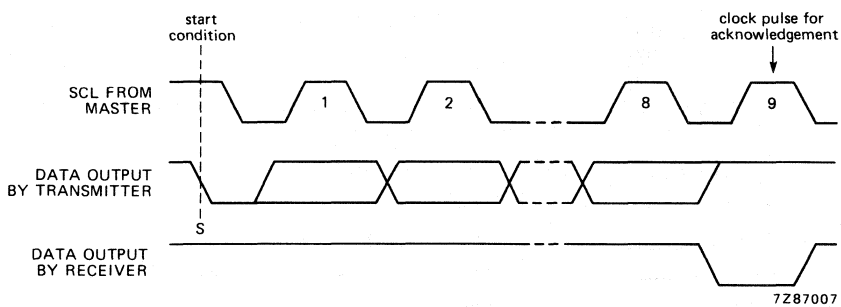


Fig. 9 Acknowledgement on the I^2C bus.

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

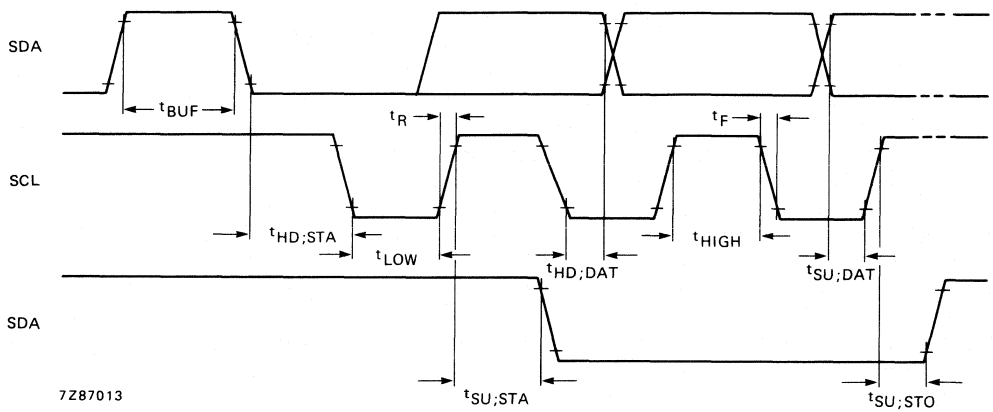


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

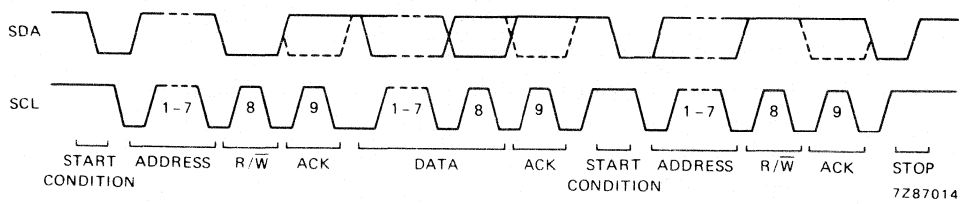


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

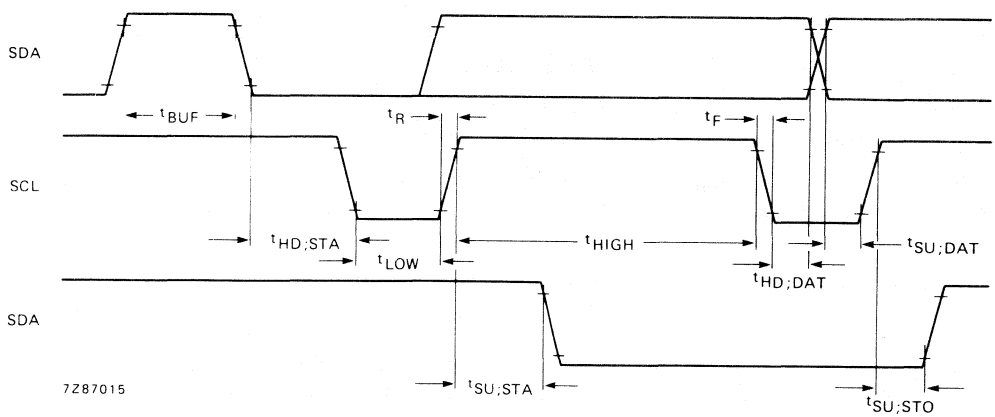


Fig. 12 Timing of the low-speed mode.

DEVELOPMENT DATA

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

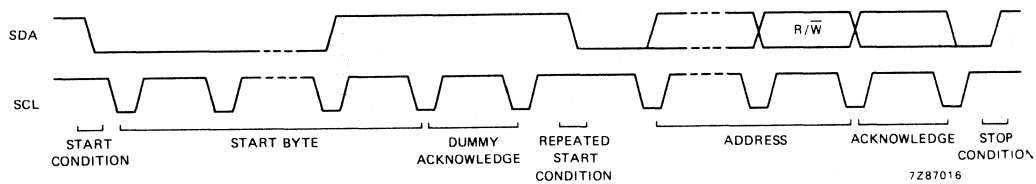


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	—	10	mA
D.C. output current (any output)	$\pm I_O$	—	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	—	50	mA
Power dissipation per output	P_O	—	50	mW
Total power dissipation per package	P_{tot}	—	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	—	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	—	50	100	μA
single output tone	I_{DD}	—	0,5	1,0	mA
dual output tone	I_{DD}	—	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	—	—	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	—	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	—	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	—	—	mA
Clock frequency (see Fig. 10)	f_{SCL}	—	—	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	—	—	7	pF
Allowable input spike pulse width	t_I	—	—	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

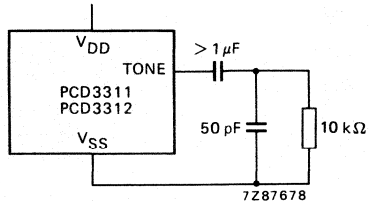


Fig. 14 TONE output test circuit.

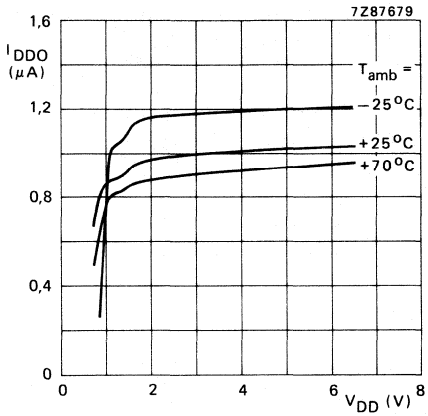


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

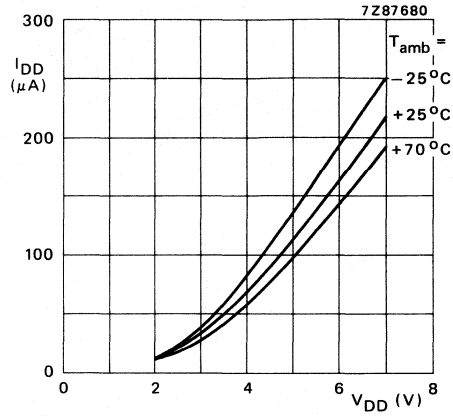


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

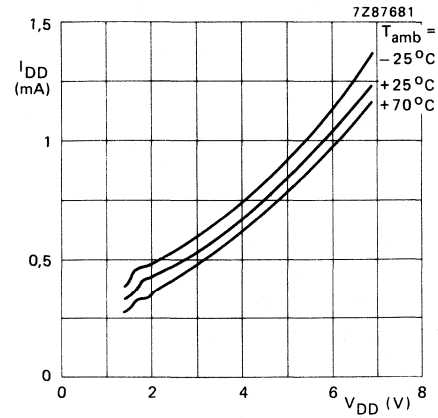


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

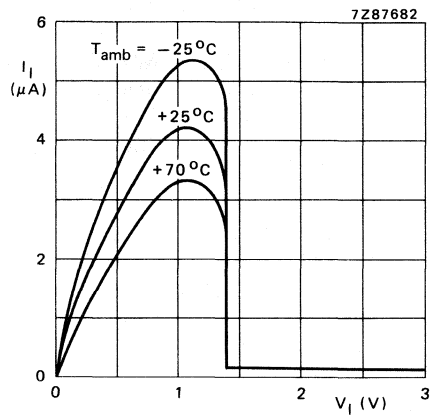


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

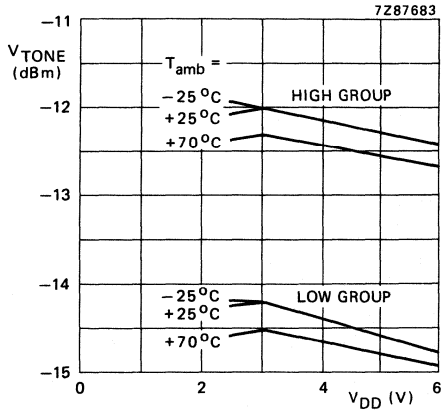


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

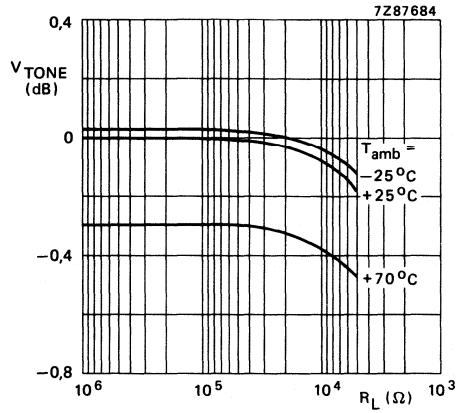


Fig. 20 Dual tone output voltage level as a function of output load resistance.

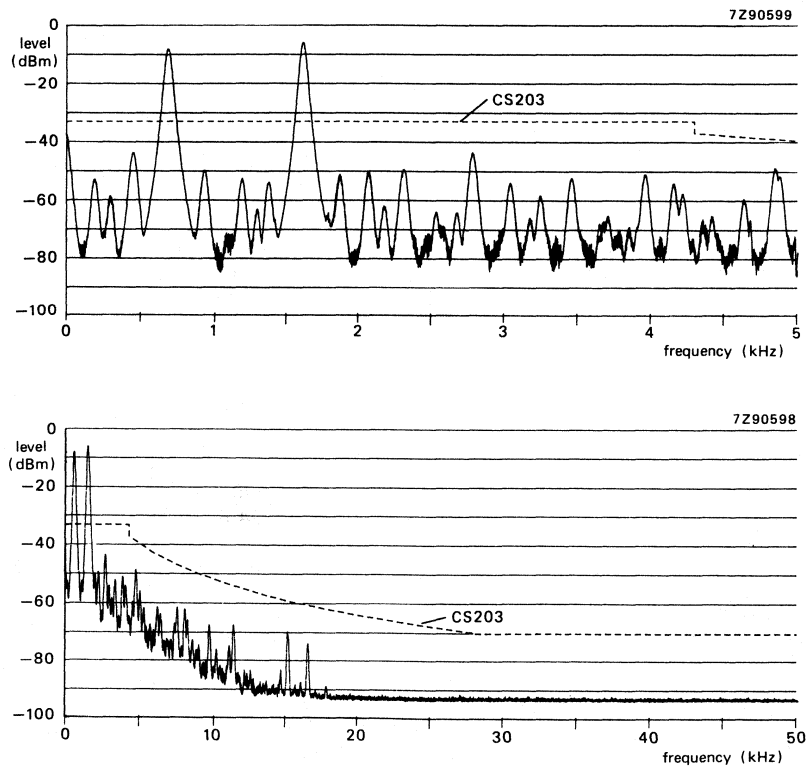


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

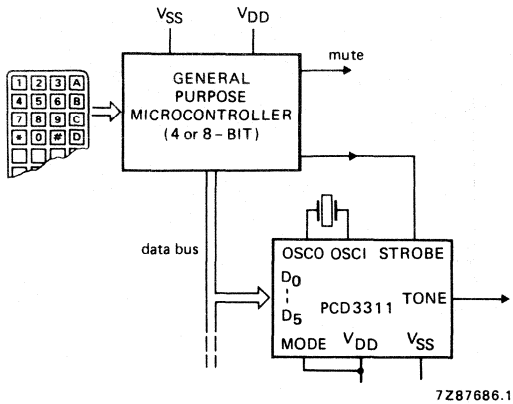


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

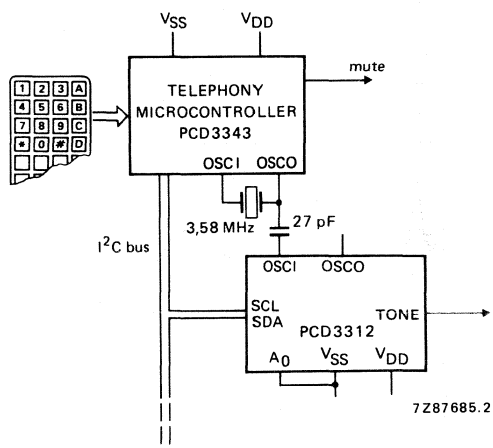
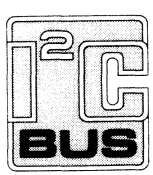


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

DTMF/SINGLE-TONE GENERATOR

GENERAL DESCRIPTION

The PCD3311A is a single-chip silicon gate CMOS integrated circuit. It is intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The device can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With its on-chip voltage reference the PCD3311A provides constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the device provides 32 single frequencies.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINE

PCD3311AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

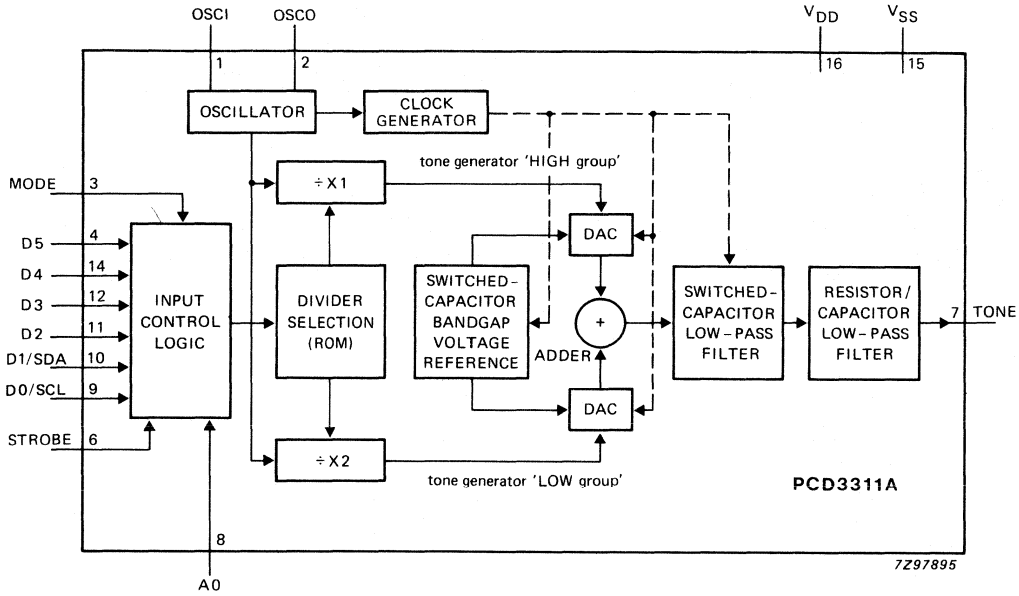


Fig. 1 Block diagram.

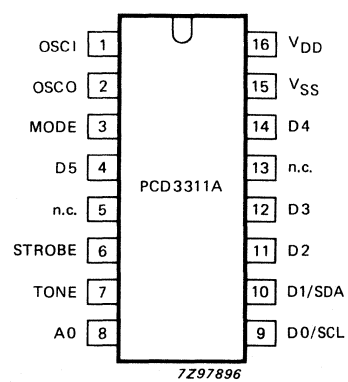


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D0/SCL	parallel data input* or serial clock line (I^2C bus)
10	D1/SDA	parallel data input* or serial data line (I^2C bus)
11	D2	parallel data inputs*
12	D3	
14	D4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5;13	n.c.	not connected

* MODE = HIGH.

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311A is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus.

Parallel mode can only be obtained by setting MODE input HIGH.

Data inputs (D0, D1, D2, D3, D4 and D5)

Inputs D0 and D1 have no internal pulll-down or pull-up resistors and must not be left open in any application. Inputs D2 to D5 have internal pull-down.

Tables 1, 2 and 3 show all input codes and their corresponding output frequencies.

Strobe input (STROBE)

This input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained by setting MODE input LOW.

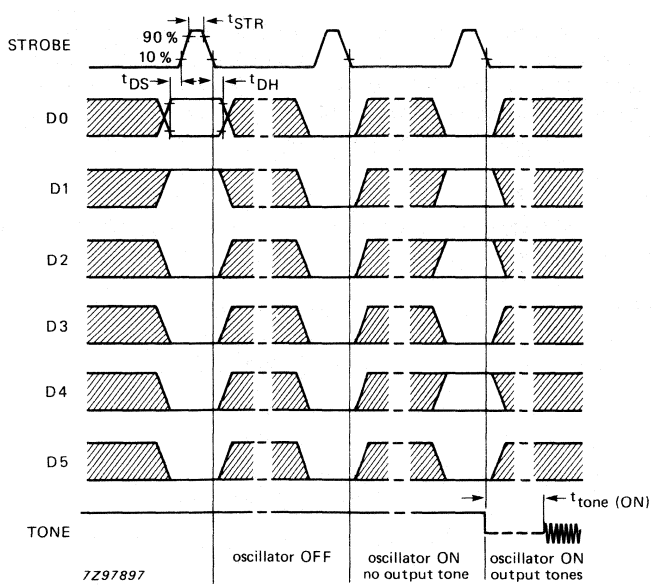


Fig. 3 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

FUNCTIONAL DESCRIPTION (continued)

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D0 and D1 respectively. For the PCD3311A the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I²C bus specification (see "CHARACTERISTICS OF THE I²C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A0)

A0 is the slave address input and it identifies the device when up to two PCD3311 devices are connected to the same I²C bus. However, A0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 4)

The PCD3311 is always a slave receiver in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode where the least significant bit is selectable by hardware on input A0, and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 1, 2 and 3). D6 and D7 are don't care (X) bits.

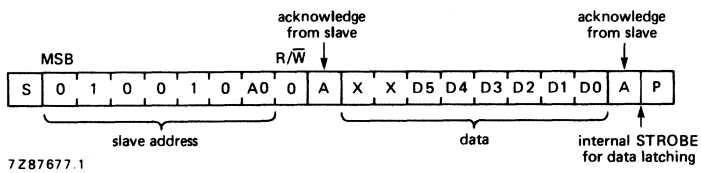


Fig. 4 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 2 shows the frequency tolerance of the output tones for DTMF signalling; Table 3 for the single tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 1 Input data for control (no output tone; TONE at V_{DD})

D5	D4	D3	D2	D1	D0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care.

Table 2 Input data for DTMF

D5	D4	D3	D2	D1	D0	HEX	symbol	standard frequency Hz	tone output freq. Hz*	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

DEVELOPMENT DATA

* Tone output frequency when using a 3,579 545 MHz crystal.

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for single frequencies

D5	D4	D3	D2	D1	D0	HEX	standard frequency (Hz)	tone output (Hz)*	frequency deviation	
									%	Hz
0	0	0	1	0	0	04	680	679,62	−0,06	−0,38
0	0	0	1	0	1	05	740	741,11	+0,15	+1,11
0	0	0	1	1	0	06	810	810,59	+0,07	+0,59
0	0	0	1	1	1	07	873	874,34	+0,15	+1,34
1	0	0	1	0	0	24	886	884,28	−0,20	−1,73
1	0	0	1	0	1	25	930	931,93	+0,21	+1,93
1	0	0	1	1	0	26	970	972,70	+0,28	+2,70
1	0	0	1	1	1	27	991	991,29	+0,03	+0,29
1	0	1	0	0	0	28	1055	1051,57	−0,33	−3,43
1	0	1	0	0	0	28	1060	1051,57	−0,80	−8,43
1	0	1	0	0	1	29	1124	1127,77	+0,34	+3,77
1	0	1	0	1	0	2A	1160	1161,44	+0,12	+1,44
1	0	1	0	1	1	2B	1197	1197,17	+0,01	+0,17
1	0	1	1	0	0	2C	1270	1275,68	+0,45	+5,68
1	0	1	1	0	0	2C	1275	1275,68	+0,05	+0,68
1	0	1	1	0	1	2D	1358	1353,33	−0,34	−4,68
1	0	1	1	1	0	2E	1400	1402,09	+0,15	+2,09
1	0	1	1	1	1	2F	1446	1441,04	−0,34	−4,96
1	1	0	0	0	0	30	1520	1525,81	+0,38	+5,81
1	1	0	0	0	0	30	1530	1525,81	−0,27	−4,19
1	1	0	0	0	1	31	1540	1540,92	+0,06	+0,92
1	1	0	0	1	0	32	1640	1638,24	−0,11	−1,76
1	1	0	0	1	1	33	1670	1673,47	+0,21	+3,47
1	1	0	1	0	0	34	1747	1748,68	+0,10	+1,68
1	1	0	1	0	1	35	1830	1830,97	+0,05	+0,97
1	1	0	1	1	0	36	1860	1852,77	−0,39	−7,23
1	1	0	1	1	1	37	1960	1970,03	+0,51	+10,03
1	1	0	1	1	1	37	1981	1970,03	−0,55	−10,97
1	1	1	0	0	0	38	2000	2021,20	+1,06	+21,20
1	1	1	0	0	1	39	2110	2103,14	−0,33	−6,86
1	1	1	0	1	0	3A	2200	2192,01	−0,36	−7,99
1	1	1	0	1	1	3B	2247	2255,54	+0,38	+8,54
1	1	1	1	0	0	3C	2280	2288,71	+0,38	+8,71
1	1	1	1	0	1	3D	2400	2394,34	−0,24	−5,66
1	1	1	1	1	0	3E	2600	2593,87	−0,24	−6,13
1	1	1	1	1	1	3F	2800	2779,15	−0,75	−20,85

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

* Tone output frequency when using a 3,579545 MHz crystal.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

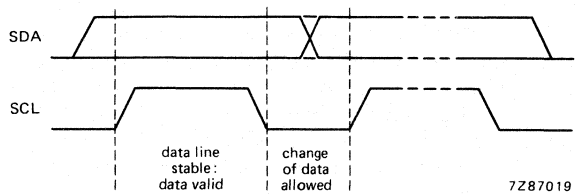


Fig. 5 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

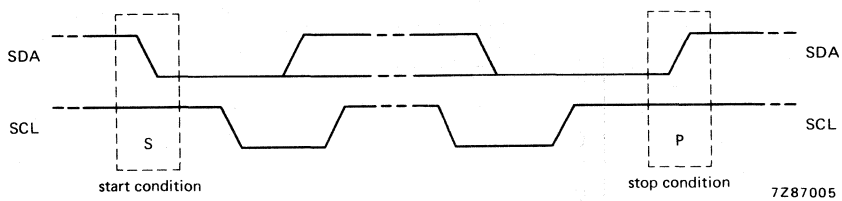


Fig. 6 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

CHARACTERISTICS OF THE I²C BUS (continued)

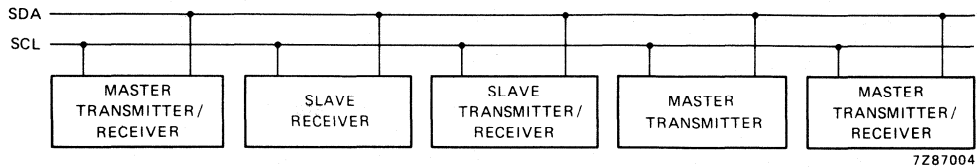


Fig. 7 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

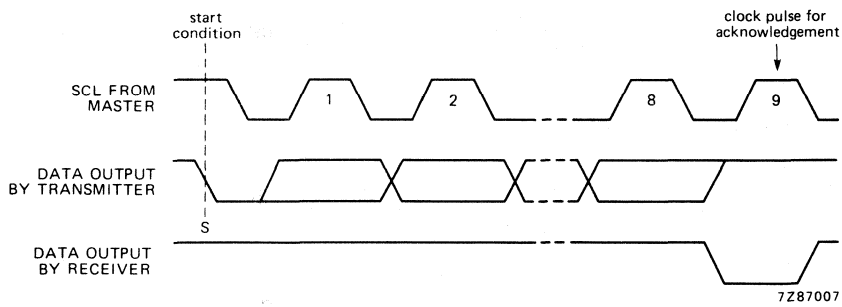


Fig. 8 Acknowledgement on the I²C bus.

DEVELOPMENT DATA

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 9.

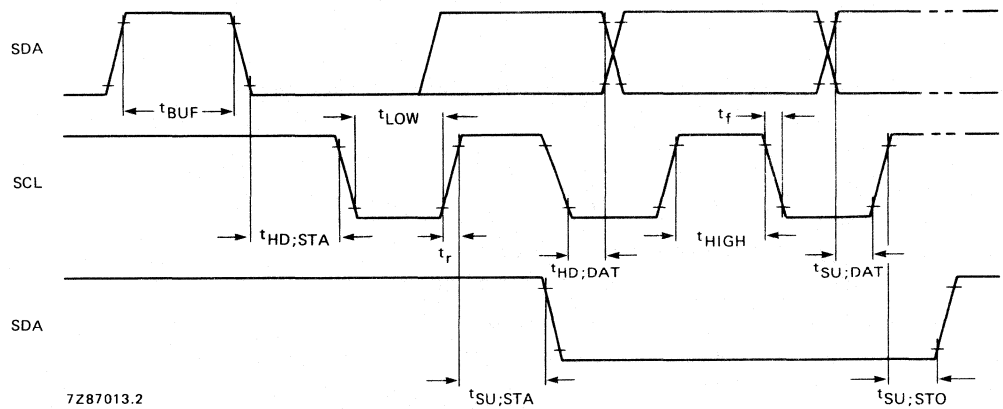


Fig. 9 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

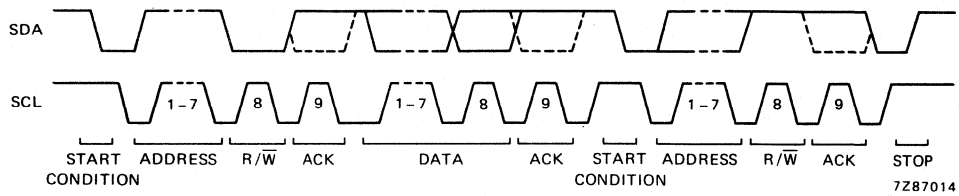


Fig. 10 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 11.

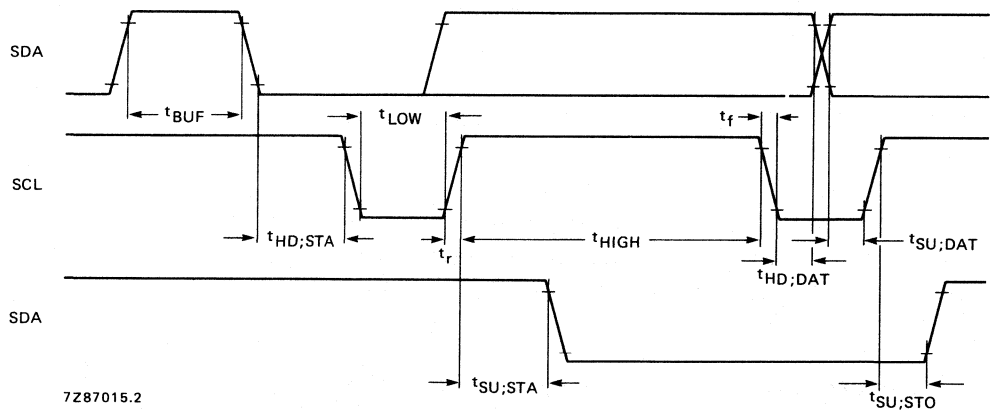


Fig. 11 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

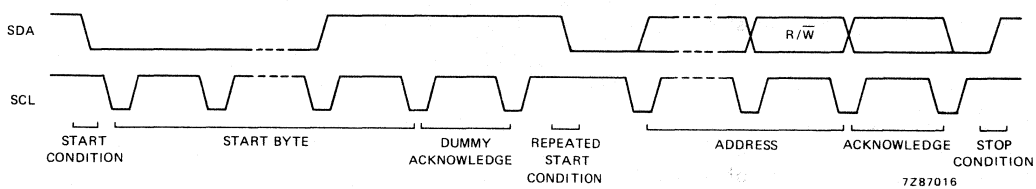


Fig. 12 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 100 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,9	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D0 to D5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D2 to D5; MODE; STROBE; A0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D0); SDA (D1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D0/SCL and D1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

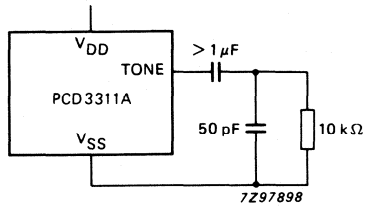


Fig. 13 TONE output test circuit.

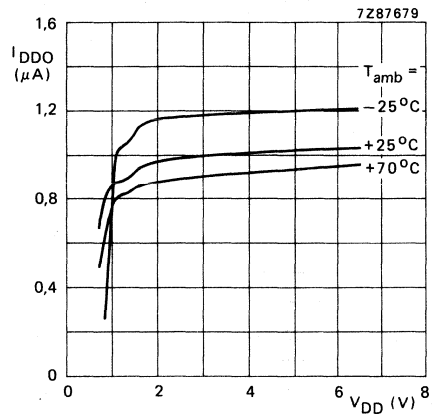


Fig. 14 Standby supply current as a function of supply voltage; oscillator OFF.

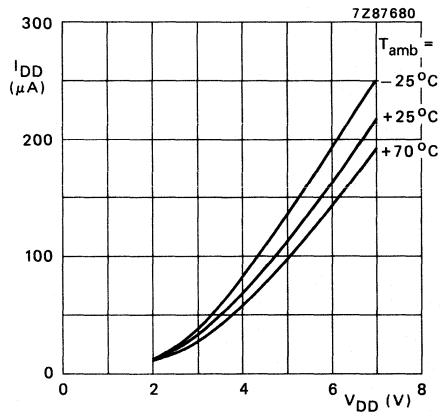


Fig. 15 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

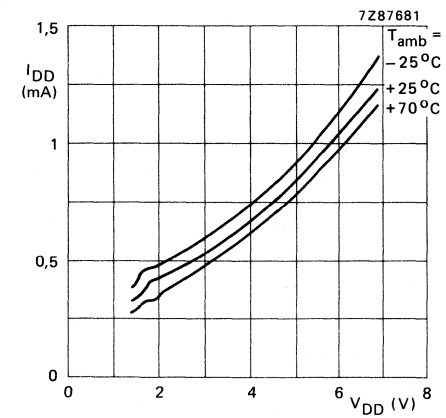


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

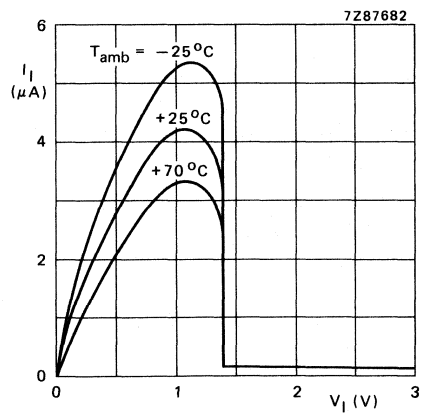


Fig. 17 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

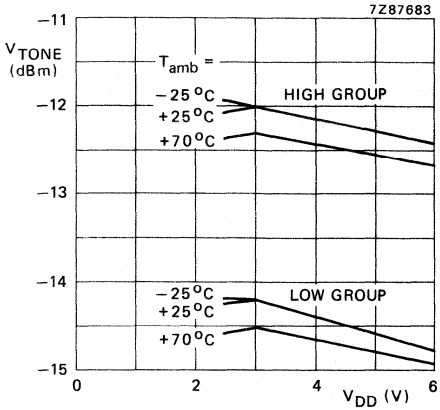


Fig. 18 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

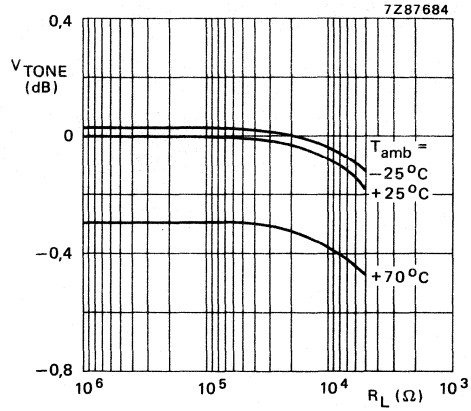


Fig. 19 Dual tone output voltage level as a function of output load resistance.

DEVELOPMENT DATA

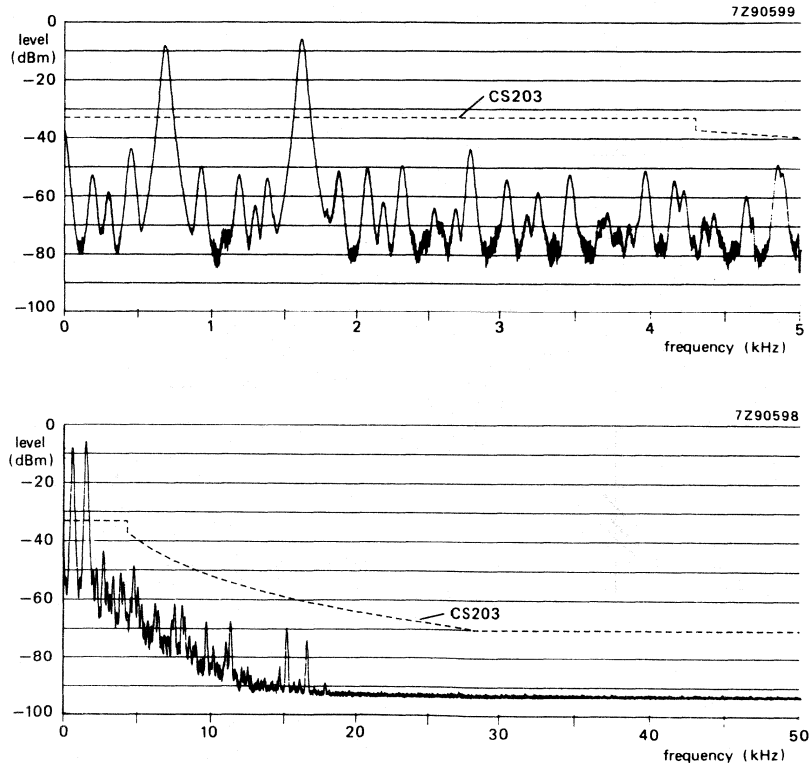


Fig. 20 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

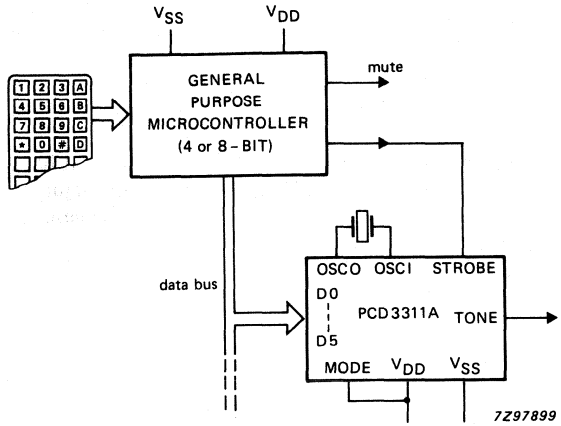


Fig. 21 PCD3311A driven by a microcontroller with parallel data-bus.

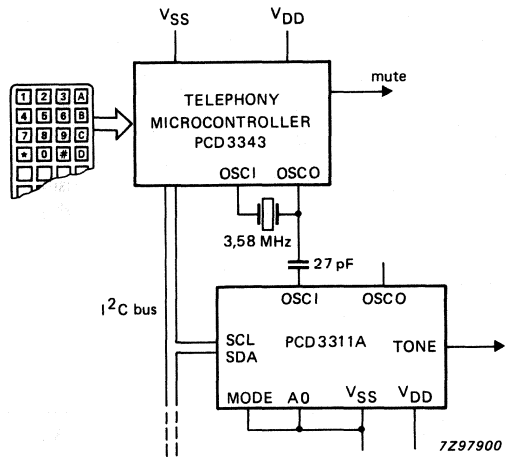


Fig. 22 PCD3311A driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus). The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes.

CMOS REDIAL AND REPERTORY DIALLER

GENERAL DESCRIPTION

The PCD3315/503 is a single chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD), and dual tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312. In addition to manual dialling it also features several automatic functions, e.g. redial, extended redial, notepad and repertory dial.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Ten repertory dial numbers
- Successsive dial and autodial procedures during a single call
- 18-digit capacity for each autodial memory
- Number of digits per call is infinite (FIFO register)
- Flash or register recall
- Uses standard 4 x 4 keyboard (single or double contact)
- Four extra function keys: program/autodial, flash, redial, access pause
- Keyboard expansion is possible to accomodate the 10 repertory dialling numbers
- Access pause generation and termination.
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Four diode or strap functions: mark-space ratio, FLASH time, access pause time and tone bursts time
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	min. 1	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DD}	typ. 270	μA
dialling mode	I_{DD}	typ. 500	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to +70	°C

PACKAGE OUTLINES

PCD3315P: 28-lead DIL; plastic (SOT117).
PCD3315T: 28-lead mini-pack; plastic (SO28; SOT136A).

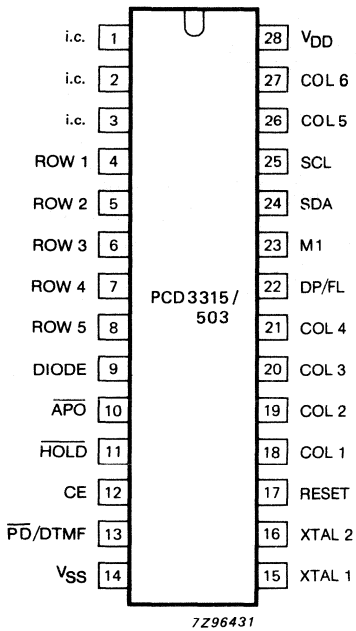


Fig. 1 Pinning diagram.

PINNING

1	i.c.	internally connected
2	i.c.	internally connected
3	i.c.	internally connected
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	DIODE	diode option output
10	$\overline{\text{APO}}$	access pause output
11	$\overline{\text{HOLD}}$	hold input
12	CE	chip enable input
13	$\overline{\text{PD}}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	crystal pins
16	XTAL 2	
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	DP/FL	dialling pulse and flash output
23	M1	muting output
24	SDA	serial data
25	SCL	serial clock
26	COL 5	sense column keyboard inputs
27	COL 6	
28	V_{DD}	positive supply

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The minimum supply voltage and supply current depend on the operating modes:

- Standby
- Conversation
- Dialling

(see operational description)

Oscillator (XTAL 1; XTAL 2)

The timebase for the PCD3315/503 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between XTAL 1 and XTAL 2. The oscillator will run when the CE = HIGH.
The output XTAL 2 can drive the oscillator input of the PCD3312 via a capacitor.

Keyboard inputs/outputs (COL 1 to 6; ROW 1 to 5)

The sense column COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 4 are directly connected to a 4 x 4 single contact keyboard matrix. An extra row (ROW 5) is added to address four additional function keys that are required for autodial functions.
Repertory dialler extension (ROW 1 to ROW 5/COL 5 and COL 6): 10 extra keys to access by single button repertory numbers (on-chip RAM). The keyboard organization is shown in Fig. 2. Keyboard entries are valid 20 ms (debounce time) after the leading edge and until 20 ms after the trailing edge of the keyboard entry.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling and are ignored.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid.

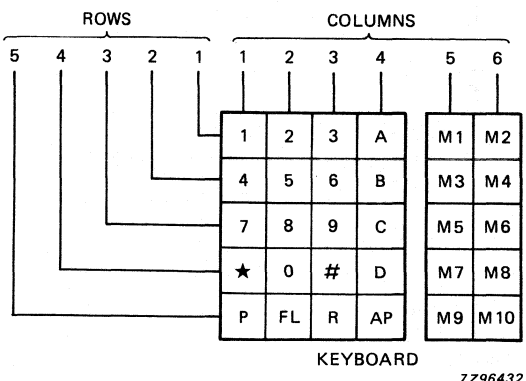


Fig. 2 Keyboard organization.

Diode option output (DIODE)

An extra row is added to the keyboard matrix to provide several selections:

- Access pause duration
- "Flash" time selection
- Mark/space ratio
- Tone burst time selection

Dialling pulse and flash output (DP/FL)

This output drives the line interrupter circuit. In pulse dialling mode it controls the timing for the line interrupter. This output also provides a "Flash" pulse which generates a 95/650 ms line break, selected via a diode option.

FUNCTION DESCRIPTION (continued)

Chip enable input (CE)

The CE input is used for hook-detection.
Hook-off will result in CE = HIGH. This will change the circuit state from standby to operational mode and also initialize the circuit.
When the circuit detects a line break longer than the reset delay time, it will switch the IC to the standby mode. This essentially achieves a low standby current during hook-on.
During access pauses the reset delay time is longer because the telephone line supply is switched over, which may result in longer line drops.

Mute output (M1)

This output is active:

- In pulse dialling mode; Mute = HIGH during inter-digit pause plus dialling pulses
- In DTMF dialling mode; Mute = HIGH during DTMF bursts plus hold-over time
- During access pauses; Mute = HIGH during the mute hold-over time
- During flash; Mute = HIGH
- During programming.

Hold input ($\overline{\text{HOLD}}$); **access pause output** ($\overline{\text{APO}}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during the inter-digit pause.
The hold function facilitates an extra time delay during dialling under the control of external circuitry, i.e. a dialling tone recognizer.
In the hold state ($\overline{\text{HOLD}}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode.
The $\overline{\text{HOLD}}$ input can be controlled by the access pause output ($\overline{\text{APO}}$) directly, or indirectly via a dialling tone recognizer (see Fig. 3). The $\overline{\text{APO}}$ output will go LOW when an access pause is recognized.

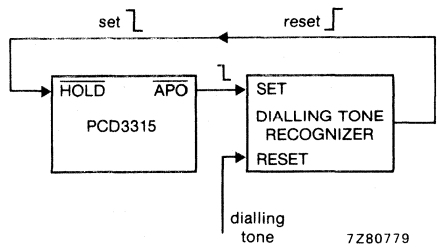


Fig. 3 Automatic variation of length of an access pause under the control of a dialling tone recognizer.

Serial data (SDA); **serial clock** (SCL)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode (see Fig. 5). Both outputs require external pull-up resistors.

Dialling mode selection input ($\overline{\text{PD}}$/DTMF)

This input selects the dialling mode:

- $\overline{\text{PD}}$/DTMF = LOW selects pulse dialling
- $\overline{\text{PD}}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3315/503 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is in the standby mode.
The oscillator is switched off and the IC requires only a low standby current (1,2 μA typ.) for memory retention.
0,5 ms after CE becomes HIGH the circuit will leave the standby mode and enter the conversation mode.

Conversation mode

In this mode the IC is active in order to scan the keyboard entries. Mute and dialling pins are inactive.
The current consumption is 270 μA (typ.) at V_{DD} = 3 V.

Dialling mode

The IC will be switched to the fully operational mode in the following circumstances:

- A valid keyboard entry
- Dialling mode
- Programming mode

The current consumtion is 500 μA (typ.) at V_{DD} = 3 V.

The PCD3315/503 has two dialling modes:

- Pulse dialling direct via DP/FL output
- DTMF dialling via PCD3312 using the serial I/O lines SDA and SCL

Pulse dialling

The timing sequence for pulse dialling is shown in Fig. 4a.
Output DP/FL starts with an inter-digit pause, followed by a sequence of pulses corresponding with the digit for transmission. The dialling frequency is fixed at 10 Hz, the break and make times are 60 ms and 40 ms respectively.
With diode option the user can also select break and make times of 67 ms and 33 ms respectively.
The muting pulse will overlap the total dialling sequence. After dialling the muting output (M1) goes LOW and the circuit is switched to the conversation mode.

DTMF dialling

The timing sequence for DTMF dialling is shown in Fig. 4b.
The PCD3312 generates the selected DTMF tones via the serial I/O lines SDA and SCL. These tones are transmitted with minimum tone burst durations of 70,70 ms or 100,100 ms with diode option.
The maximum tone burst duration is equal to the key depression time.
After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

OPERATION

Normal dialling

The IC has a working register with a maximum capacity of 18 positions. Entries in these positions maybe:

- 10 numeric digits 0 to 9
- Manually programmed access pauses
- 6 non-numeric special keys (*, #, A, B, C, D) in DTMF mode

If none of the special keys have been pressed the contents of the working register will be stored automatically in the Redial Buffer.
The number of digits can be extended but this will result in a redial memory clear after hook-on.
Up to 18 digits can be stored in the redial register. After the main store overflows, a 10-digit First-in First-out (FIFO) register takes over as buffer. After transmitting the first digit of the FIFO register this place is automatically cleared and new data can be stored there. In this way an unlimited number can be transmitted if the key-in rate is not too fast. However if this FIFO register also overflows (more than 10 digits in store) further input will be ignored.
This is also valid for manual dialling after automatic dialling.

Automatic dialling

In addition to manual dialling the IC provides the following automatic functions:

- Redial of the last dialled number
- Extended redial
- Electronic notepad
- Maximum of 10 repertory dialling numbers

The maximum capacity of the registers for these numbers is also 18 positions. The 6 non-numeric digits (*, #, A, B, C, D) will not be stored.

To achieve these automatic dialling functions an extra row of the keyboard is required which contains the following special function keys:

- P programming/automatic dialling
- FL flash or register recall
- R redial
- AL manual access pause entry

Besides the operational procedure for automatic dialling, there are also procedures for programming these numbers into the memory (see Table 1).

Table 1 Keying procedures for dial and program operation

mode	operation	program
redial	R	automatic
extended redial	P · R	TN · P
notepad	P · R	$\underline{\text{dial}}$ · P · P · TN · P
repertory dial	P · d	$\overline{\text{P}}$ · d · TN
or	M	$\overline{\text{P}}$ · M · TN
PABX digits	automatic	$\overline{\text{P}}$ · R · d_1 (d_2) R d_3 (d_4)
reset autodial	$\underline{\text{hook-on}}$	
RAM	$\underline{\text{2, 5, 8, 0}}$	
	hook-off	
	2, 5, 8, 0	

Where:

P = press and release P-key
$\overline{\text{P}}$ = press and keep P-key pressed
R = press and release R-key
TN = telephone number
$\underline{\text{d}}$ = digit 0 to 9
$\underline{\text{2, 5, 8, 0}}$ = press and keep pressed keys 2, 5, 8 and 0
2, 5, 8, 0 = release keys 2, 5, 8 and 0
M = press and release M-key

DEVELOPMENT DATA

Successive repertory dialling during a call

It is possible to dial more than one repertory number during one single telephone call using the following procedures:

- Redial, extended redial or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial followed by one or more repertory numbers

Repertory button dialling via extended keyboard

The PCD3315/503 has the facility to store 10 repertory numbers, activated by the P-button with a number key or by using direct button action. Then the stored numbers can be re-called by pressing one of the 10 name buttons. The keyboard extension is connected via pins 26 and 27.

OPERATION (continued)

Access pause

During a dialling sequence it may be necessary to insert a wait time to ensure correct dialling.
A dialling sequence can always be interrupted by the $\overline{HOLD}$ input through an access pause recognition, which results in a fixed time delay.
There are 3 possibilities **to enter** an access pause:

- At manual dialling by pressing the AP key
- At auto dialling by recognition of the AP-code in the memory
- Recognition of PABX digits, after which an automatic access pause will be inserted

There are 4 possibilities **to terminate** an access pause:

- $\overline{HOLD}$, $\overline{APO}$ pins directly interconnected; after a fixed time delay of 3 or 5 seconds in pulse dialling; 1,5 or 2,5 seconds in DTMF dialling. The fixed time delay is determined by a diode strap
- $\overline{HOLD}$, $\overline{APO}$ pins interconnected via an RC network; after a fixed time delay of 3 or 5 seconds in pulse dialling; 1,5 or 2,5 seconds in DTMF dialling – plus an additional time delay determined by the RC values
- $\overline{APO}$ pin enables a dialling tone recognizer, which controls the $\overline{HOLD}$ input (see Fig. 3)
- $\overline{HOLD}$ input connected to V_{DD}; no access pause

During the access pause the muting output remains active during hold-over time. In order to handle longer line drops during access pauses, the PCD3315 automatically switches to the maximum reset delay time of 320 ms.

PABX digits

The PCD3315/503 will detect pre-programmed PABX digits and insert an access pause in the dialling sequence. The reserved capacity is for two different PABX numbers with a maximum of 2 digits each.

Program procedure: $\overline{P} \cdot R \cdot d_1, d_2\ R\ d_3\ d_4$.

Notepad

In the conversation mode the notepad procedure will overwrite the extended redial buffer, without dialling-out digits. After hook-off this number can be recalled through the extended redial buffer.

Store procedure : P · P · TN P
Dial : P · R

Flash (see Fig. 4b)

Flash or register recall is activated by the flash key which results in a timed line break at output pin DP/FL. This line break is of a fixed 95 or 650 ms duration in both pulse and DTMF dialling modes. In the dialling procedure a flash entry will initialize the IC and thus the working register which acts like a chip enable procedure.

Memory clear

A built-in manually total memory clear to facilitate resetting of the autodial RAM after servicing, maintenance or telephone set delivery.

Procedure: hook-on, press and keep depressed keys 2, 5, 8, 0;
hook-off, release keys 2, 5, 8, 0.

Program security

Security measures are incorporated in the IC to avoid incorrect dialling operations and hang-ups. The program has a built-in RAM check procedure to protect the autodial numbers stored in the RAM. If one or more bits of this RAM are changed during standby or the battery falls below 1,3 V (typ.), this will result in a memory clear to avoid subsequent incorrect dialling.

Diode options

There are 4 different diode or strap options which are an extension of the keyboard matrix. Addressing is via the 4 columns and diode pins.
There are two possibilities:

- Without diode
- With diode (cathode on row-side)

The built-in selections are shown in Table 2.

Table 2 Diode option selections

column	description	without diode	with diode	remarks
4	tone burst	100,100 ms	70,70 ms	–
1	break, make-time	60,40 ms	67,33 ms	–
2	access pause	3 s	5 s	pulse dialling
2	access pause	1,5 s	2,5 s	DTMF dialling
3	flash time	95 ms	650 ms	–

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input of output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT136A	$R_{th\ j\text{-}a}$	max.	150	K/W

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	2,5	–	6	V
STOP mode for RAM retention	V_{DD}	1,0**	–	6	V
Supply current					
dialling mode					
at V_{DD} = 3 V	I_{DD}	–	500	–	μA
conversation mode					
at V_{DD} = 3 V	I_{DD}	–	270	–	μA
STOP mode*					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	1,5	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH (except SDA, SCL)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA

* Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and $\overline{PD}$/DTMF at V_{SS}.

** Because RAM is cleared if POR is activated by software, this value must be max. V_{RESET}.

Table 3 Timing data

parameter	symbol	typ.		unit
		without diode	with diode	
Reset delay time	t_{rds}	160	160	ms
Reset delay time during access pause	t_{rds}	320	320	ms
Keyboard debounce time	t_{db}	20	20	ms
Flash time	t_{fl}	95	650	ms
Pulse dialling				
Dial frequency	f_d	10	10	Hz
Break/make time	$t_{b/m}$	60,40	67,33	ms
Interdigit pause	t_{idp}	840	840	ms
Access pause	t_{ap}	3	5	s
Mute hold-over time *	t_h	1	1	s
DTMF dialling				
Tone transmission time	t_t	min. 100 or key-down time	min. 70 or key-down time	ms
Tone pause time	t_p	min. 100	min. 70	ms
Mute hold-over time during dialling	t_h	80 + t_p	80 + t_p	ms
Mute hold-over time during access pause	t_h	1	1	s
Access pause	t_{ap}	1,5	2,5	s

DEVELOPMENT DATA

* Only during access pause.

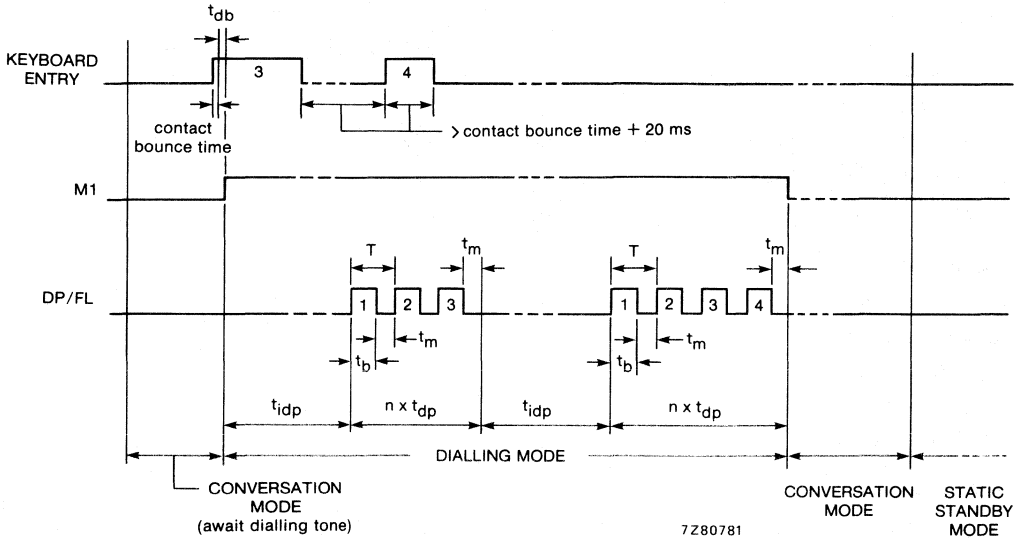


Fig. 4a Timing diagram for pulse dialling mode, defined by $\overline{PD}$/DTMF = LOW (V_{SS}).

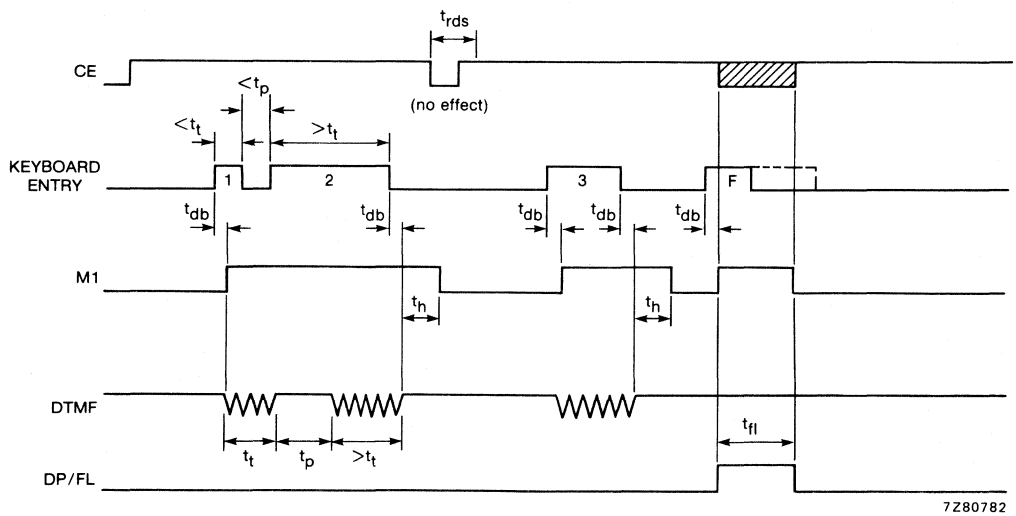


Fig. 4b Timing diagram for DTMF dialling mode, defined by $\overline{PD}$/DTMF = HIGH (V_{DD}).

DEVELOPMENT DATA

APPLICATION INFORMATION

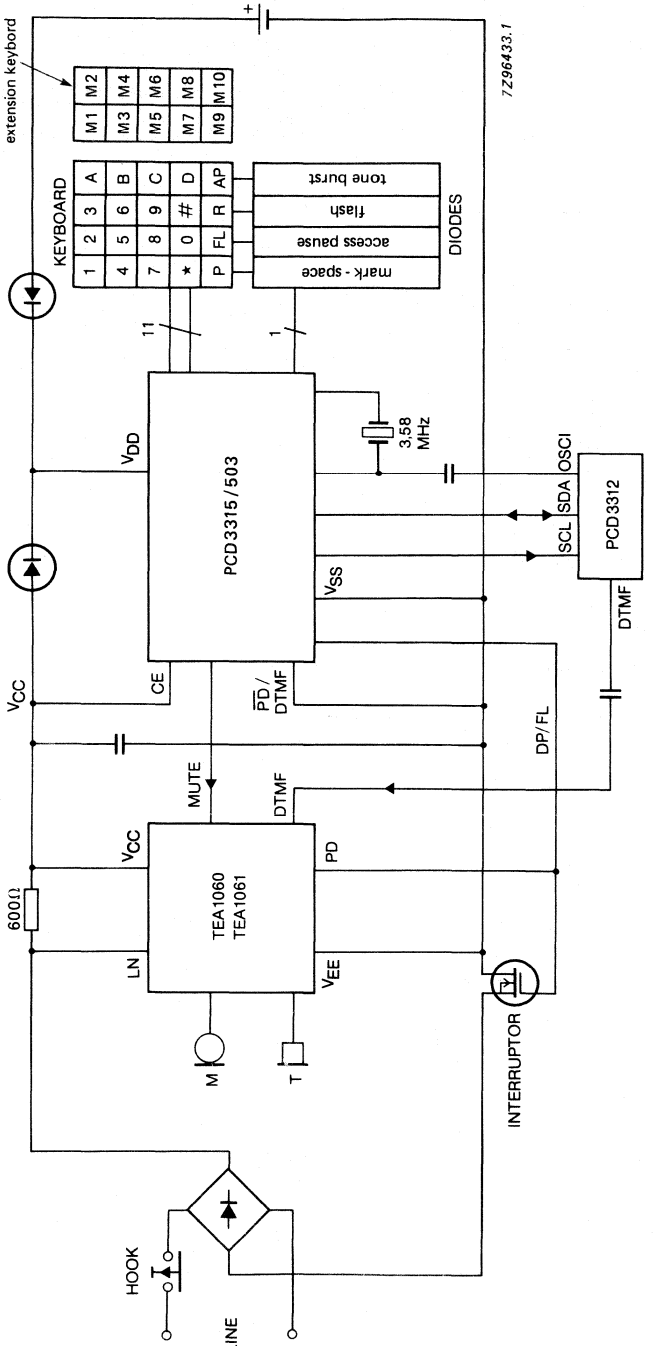


Fig. 5 Block diagram of feature phone.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3315C is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3343 family. It has special on-chip features for application in telephone sets.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 1536 ROM bytes
- 160 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400, PCD3343 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3315CP: 28-lead DIL; plastic (SOT117).
PCD3315CT: 28-lead mini-pack; plastic (SO28; SOT136A).

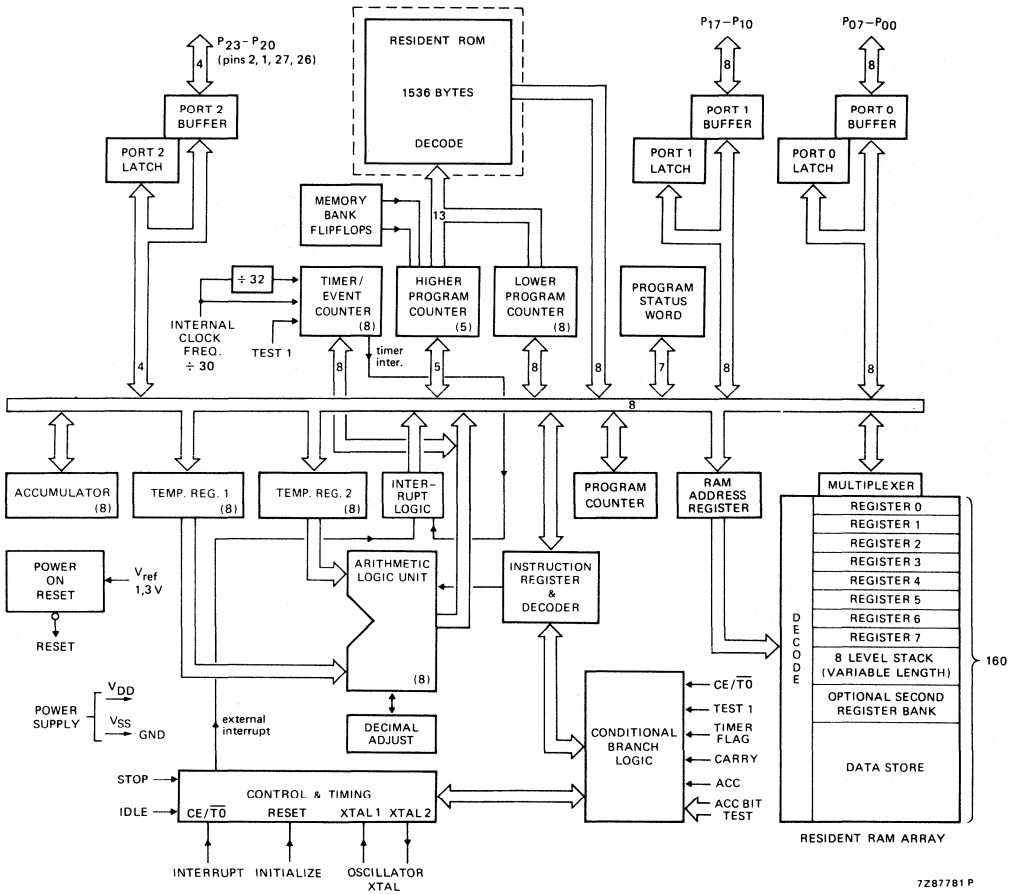
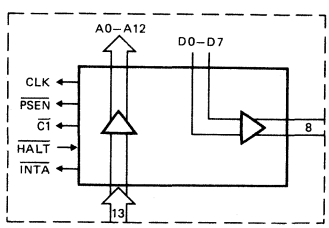
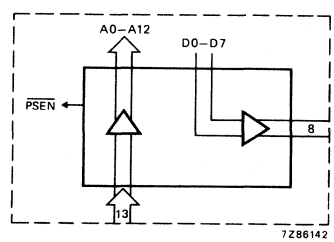


Fig. 1 Block diagram; PCD3315C.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCD8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

PULSE DIALLER CIRCUITS WITH REDIAL

GENERAL DESCRIPTION

The PCD332X family comprises eight CMOS pulse dialler circuits with redial. Each circuit converts 3x4 matrix keyboard entries into correctly-timed line current interruptions. For redial, the last-dialled number (up to 23 digits) is stored in an on-chip RAM. A RAM overflow is handled by inhibiting the redial but manual dialling of more than 23 digits still can be made. The circuits include a delayed reset for line power breaks to ensure correct operation.

Most ICs of the family regenerate an access pause during redial. Insertion of the access pause during the original entry is either automatic or via the '*' key. Termination of the regenerated access pause during redial is via the '#' key after a built-in delay or controlled by an external tone recognizer. Other differences between the circuits are selections of pulse dialling frequency, mark/space ratio, regenerated access pause duration, inter-digit pause duration, reset delay time, mute and hold/access pause output control.

Features

- Operating supply voltage range: 2,5 to 6,0 V
- Static supply voltage (with redial memory data retention): down to 1,8 V
- Low operating supply current: typ. 40 μA
- Low static standby supply current: typ. 1 μA
- On-chip RAM capacity: 23 keyboard entries (digits + access pauses)
- Redial inhibited after memory overflow
- Manual dialling can continue beyond 23 keyboard entries (excess entries are stored at lower RAM addresses)
- (Re)dialling procedure is not affected by line interruptions shorter than the reset delay time (if the supply voltage does not fall below the static standby voltage)
- Line interruptions longer than the reset delay time are regarded as on-hook situations
- Hold facility for lengthening the inter-digit period
- On-chip oscillator for 3,58 MHz crystal (type for ceramic resonator is also available)
- Fully decoded and debounced inputs for 3x4 matrix keyboard
- Pull-up or pull-down circuits at all inputs except CE
- Electrostatic discharge protection at all inputs
- High input noise immunity
- Test mode in which the dialling frequency is raised to 932 Hz

The PCD332X family of ICs comprises the following types:

PCD3320	dialler with several mute signals
PCD3321	dialler with two automatic access pauses
PCD3322	variant of PCD3320
PCD3323	dialler for sophisticated PABX applications
PCD3324	dialler with one automatic access pause
PCD3325A	dialler with manual access pause control
PCD3326	variant of PCD3321
PCD3327	variant of PCD3325A for ceramic resonator with automatic reset of access pause

functional survey		PCD							
		3320	3321	3322	3323	3324	3325A	3326	3327*
Number of pins		18	18	18	28	18	18	18	18
Dialling pulse frequency	10 Hz	●	●	●	●	●	●	●	●
selectable with F01, F02	16, 20 Hz		●		●	●	●	●	●
Mark/space ratio	3:2	●	●	●	●	●	●	●	●
selectable with M/S	2:1		●		●	●	●		●
Inter-digit pause duration	8 x T_{DP}	●	●	●	●	●	●	●	●
selectable with IDP	9 x T_{DP}				●				
Reset delay for line power breaks	1,6 x T_{DP}	●	●	●	●	●	●	●	●
selectable with RDS	3,2 x T_{DP}				●				
Access pauses repeated during redial			●		●	●	●	●	●
Manual insertion of access pauses			●		●	●	●	●	●
Automatic access pause insertion	1 max.					●			
	2 max.		●		●			●	
Access pause duration	32 x T_{DP}		●		●	●		●	
selectable with APD	64 x T_{DP}				●			●	
not automatically terminated							●		●
$\overline{M1}$, inverted mute output		●		●	●				
M2, strobe output				●	●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs		●			●				
CL, clock output					●				
APO, access pause output					●				
HOLD, dialling-interrupt input		●		●	●				
APO + HOLD, internally connected			●			●	●	●	●
APR, access pause reset input					●				
AAE, automatic access pause enable					●				

T_{DP} = dialling pulse period.

* PCD3327 for ceramic resonator

Features common to all PCD332X family

OSC IN, OSC OUT } on-chip oscillator input and output

COL1 to COL3, column keyboard inputs with on-chip pull down

ROW1 to ROW4, row keyboard inputs with on-chip pull-up

CE, chip enable input

DP, dialling pulse drive output to external line-switching transistor or relay

M1, mute output

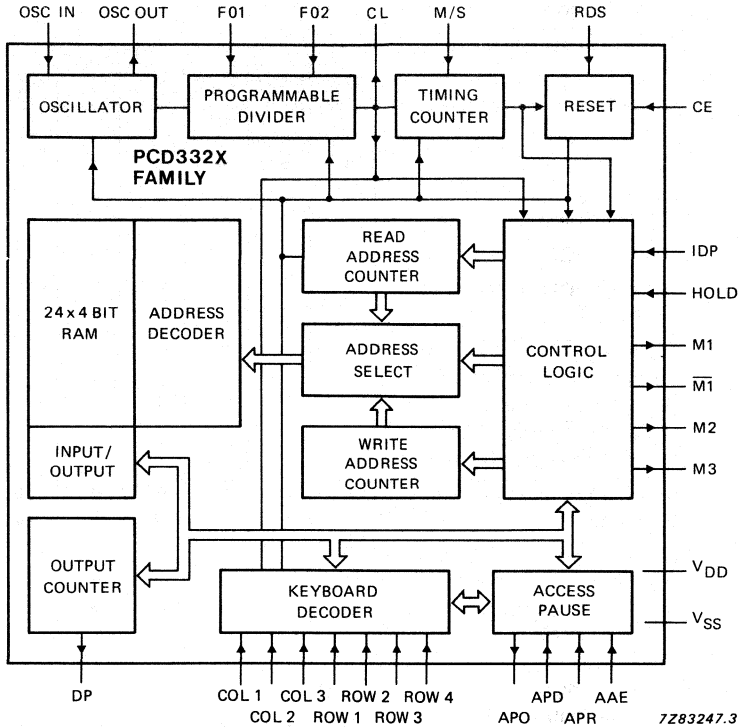


Fig. 1 Block diagram.

DEVELOPMENT DATA

PACKAGE OUTLINES

PCD3320P
PCD3321P
PCD3322P
PCD3324P
PCD3325AP
PCD3326P
PCD3327P — 18-lead DIL; plastic (SOT102G).

PCD3323P: 28-lead DIL; plastic (SOT117).

PCD3320D
PCD3321D — 18-lead DIL; ceramic (SOT133B).

PCD3323D: 28-lead DIL; ceramic (SOT135A).

PCD3323T: 28-lead mini-pack; plastic (SOT128; SOT136A).

PCD3321T
PCD3322T
PCD3327T — 20-lead mini-pack; plastic (SOT163A).

PCD3327U: uncased chip in tray.

PINNING

pin	purpose	PCD...							
		3320	3321	3322	3323	3324	3325A	3326	3327
Supplies									
V_{DD}	positive supply	●	●	●	●	●	●	●	●
V_{SS}	negative supply	●	●	●	●	●	●	●	●
Inputs									
M/S	controls mark/space ratio of the line pulses		●		●	●	●		●
IDP	Inter-Digit Pause: occurs before each digit arrives at the output; the inter-digit pause duration can be controlled by this pin				●				
F01	define the dialling pulse frequency	●	●	●	●	●	●	●	●
F02			●		●	●	●	●	●
CE	Chip Enable: used to initialize the system, to select between operating and static standby modes and to handle line power breaks	●	●	●	●	●	●	●	●
COL1 COL2 COL3	keyboard **column** inputs with on-chip pull-down	●	●	●	●	●	●	●	●
RDS	Reset Delay Selection: delay select for chip-enable (CE) activity				●				
AAE	Automatic Access pause Enable: AAE = HIGH causes the circuit to generate a maximum of two automatic pauses; AAE = LOW allows only manual pauses (via the keyboard)				●				
APR	Access Pause Reset: resets an existing access pause when an external circuit makes APR = HIGH				●				
APD	Access Pause Duration: selects the maximum duration of an access pause if no external APR appears				●			●	
ROW1 ROW2 ROW3 ROW4	keyboard **row** inputs with on-chip pull-up	●	●	●	●	●	●	●	●

pin	purpose	PCD...							
		3320	3321	3322	3323	3324	3325A	3326	3327
HOLD	interrupts dialling **after** completion of the current digit or **immediately** during an inter-digit pause	•		•	•				
Outputs									
CL	output of internal system clock; external forcing is possible for frequencies not selectable via F01, F02				•				
DP	Dialling Pulse: drive of the external switching transistor or relay	•	•	•	•	•	•	•	•
M1	Muting: normally used for muting during the dialling sequence	•	•	•	•	•	•	•	•
$\overline{M1}$	inverted output of M1	•		•	•				
M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause			•	•				
M3	AND-function with $\overline{DP}$ and M1 as inputs; for direct drive of a switching transistor for dialling pulses and muting	•			•				
APO	Access Pause Output: goes HIGH when an access pause code is read from the memory during pulsing				•				
Oscillator									
OSC IN OSC OUT	input and output of the on-chip oscillator	• •	• •	• •	• •	• •	• •	• •	• •
Input/outputs									
HOLD/APO	the HOLD and APO features are connected together at this pin, normally an output pin but can be forced as an input		•			•	•	•	•

DEVELOPMENT DATA

PINNING (continued)

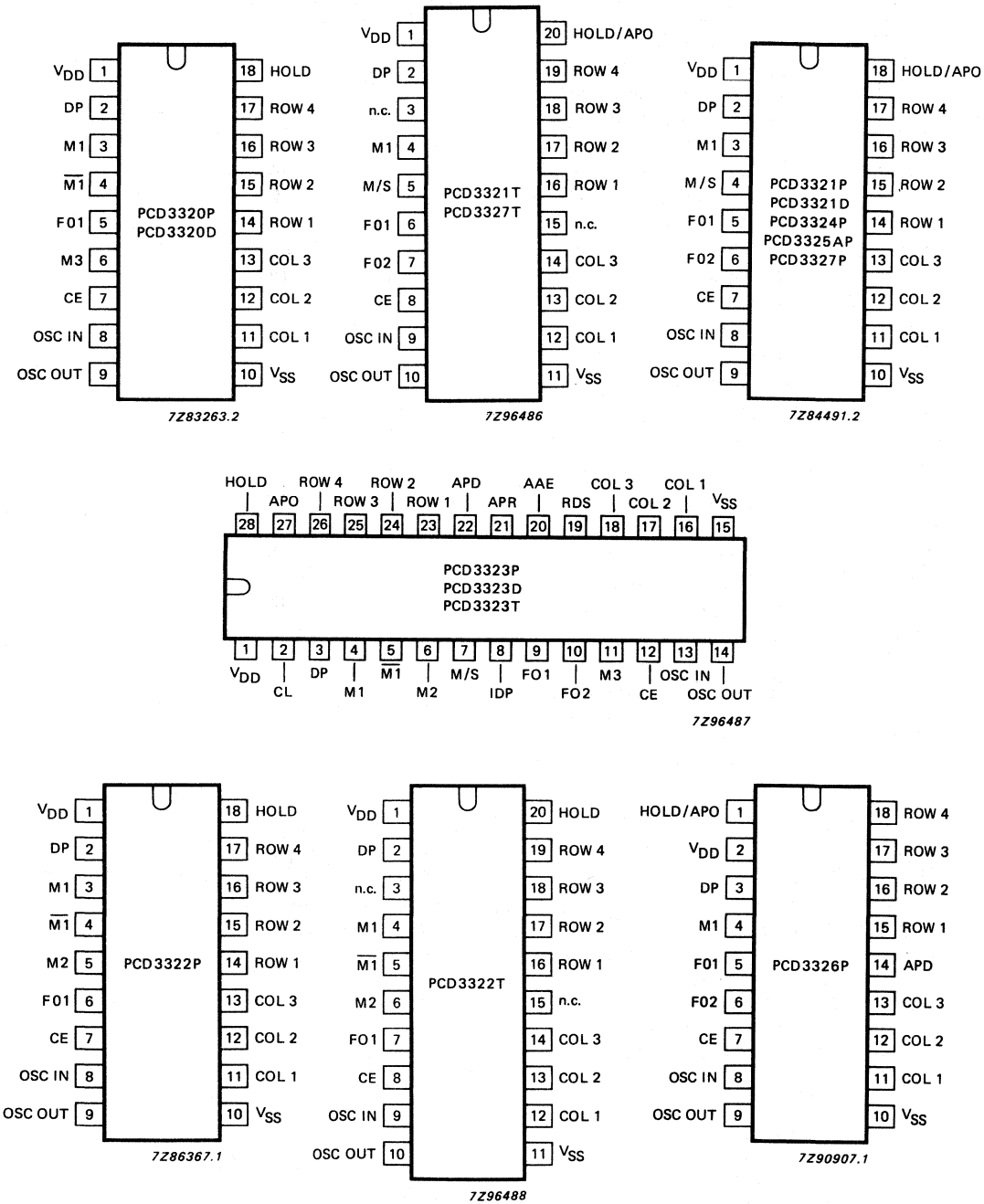


Fig. 2 Pinning diagrams.

FUNCTIONAL DESCRIPTION

Clock oscillator (OSC IN, OSC OUT)

The time base for the circuit is a crystal-controlled on-chip oscillator which is completed by the connection of a crystal between the OSC IN and OSC OUT pins (a ceramic resonator may be used with the PCD3327). Alternatively, the OSC IN pin can be driven by an external clock signal.

Clock divider (F01, F02, CL)

The oscillator is followed by a frequency divider, the division ratio of which can be set externally (F01, F02) to provide one of four chip system clocks, i.e. three 'normal' clock frequencies and one higher frequency for testing.

The system clock is available at pin CL and can be used for external logic. External forcing of CL is possible for frequencies that are not selectable through F01/F02. Other frequencies can also be obtained by driving OSC IN, as previously stated.

Chip enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped at reset, excepting the WRITE ADDRESS COUNTER (WAC). The keyboard input is prohibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced. The t_{rd} pulse duration is selected by the RDS input.

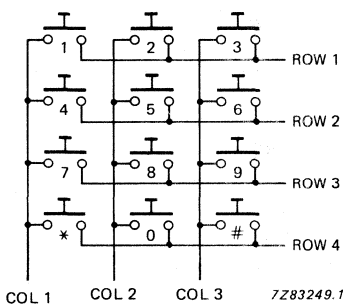
Debouncing keyboard entries (COL1, COL2, COL3; ROW1, ROW2, ROW3, ROW4)

The column keyboard inputs to the integrated circuit (COLn) and the row keyboard inputs (ROWn) are for direct connection to a 3x4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input, or when one column input is set HIGH and one row input is set LOW. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been left open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 codes are written into the RAM, memory overflow results and the access keycodes replace the data in the lower-numbered locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly-timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset (see 'Access Pause System'). During redial, no keyboard entry will be accepted and stored in the RAM. But, when all numbers stored in the RAM have been pulsed out, new keyboard entries will be accepted and stored in the RAM position after the last digit code of the original entry and converted into correctly-timed dialling pulses.



* Access pause set.

\# Redial or access pause reset.

Fig. 3 Single contact keyboard.

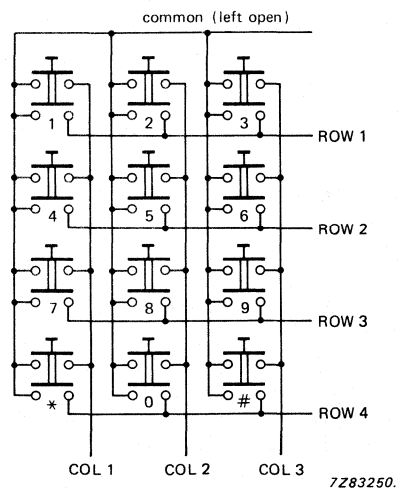


Fig. 4 Double contact keyboard.

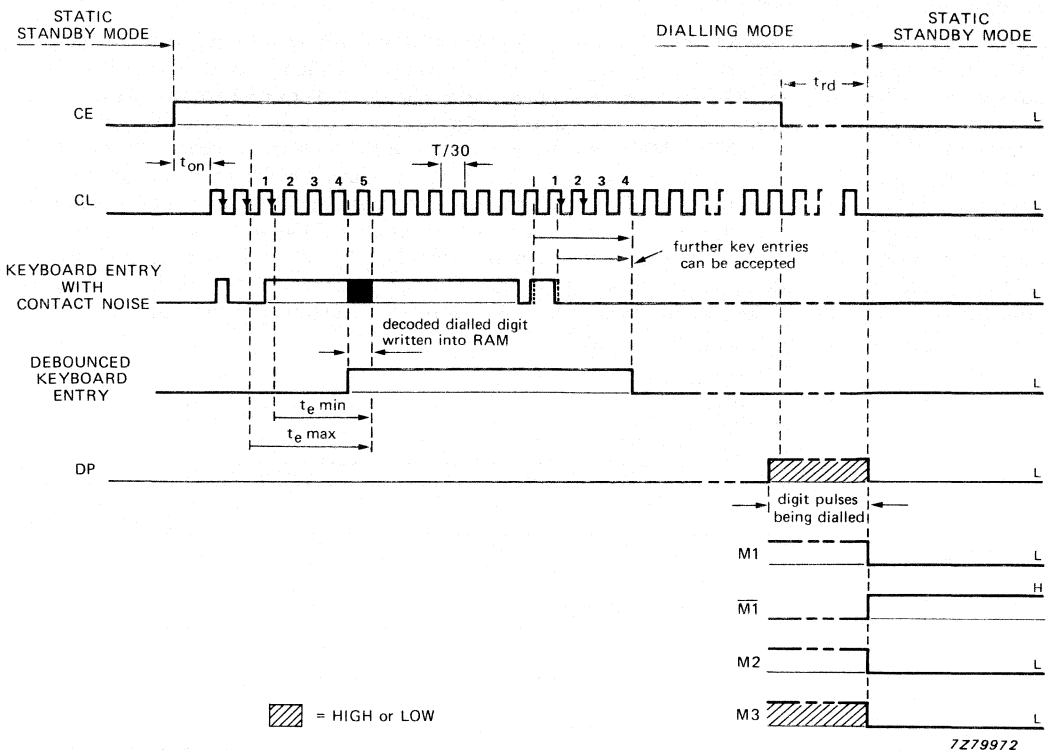


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

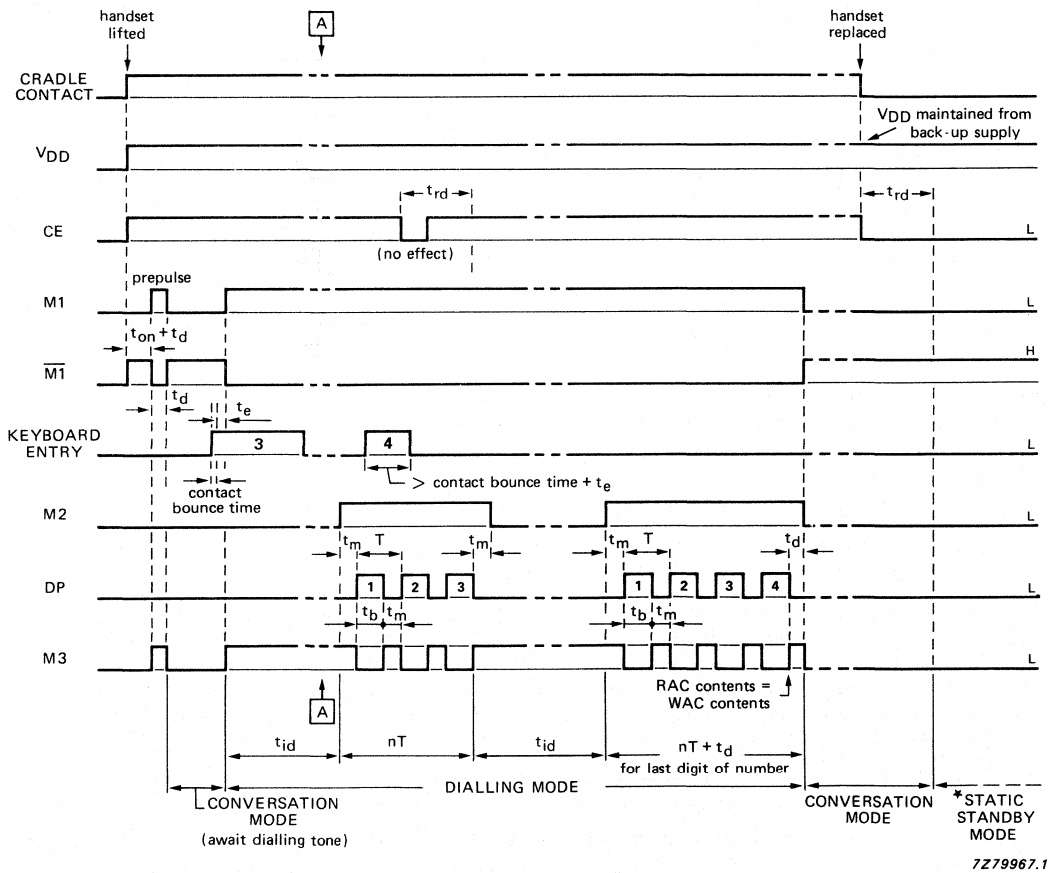
Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and ten clock pulse periods later a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that if a polarized muting relay with two stable positions is used it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4ms (t_{on}) after CE goes high, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

Dialling sequence (continued)

Referring to Fig. 6, when the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensures. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 or 3,2 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.



* Oscillator off; all registers reset; keyboard input inhibited; number stored in RAM until V_{DD} <1,8 V.

Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keybord entry (e.g. supply via the cradle contacts).

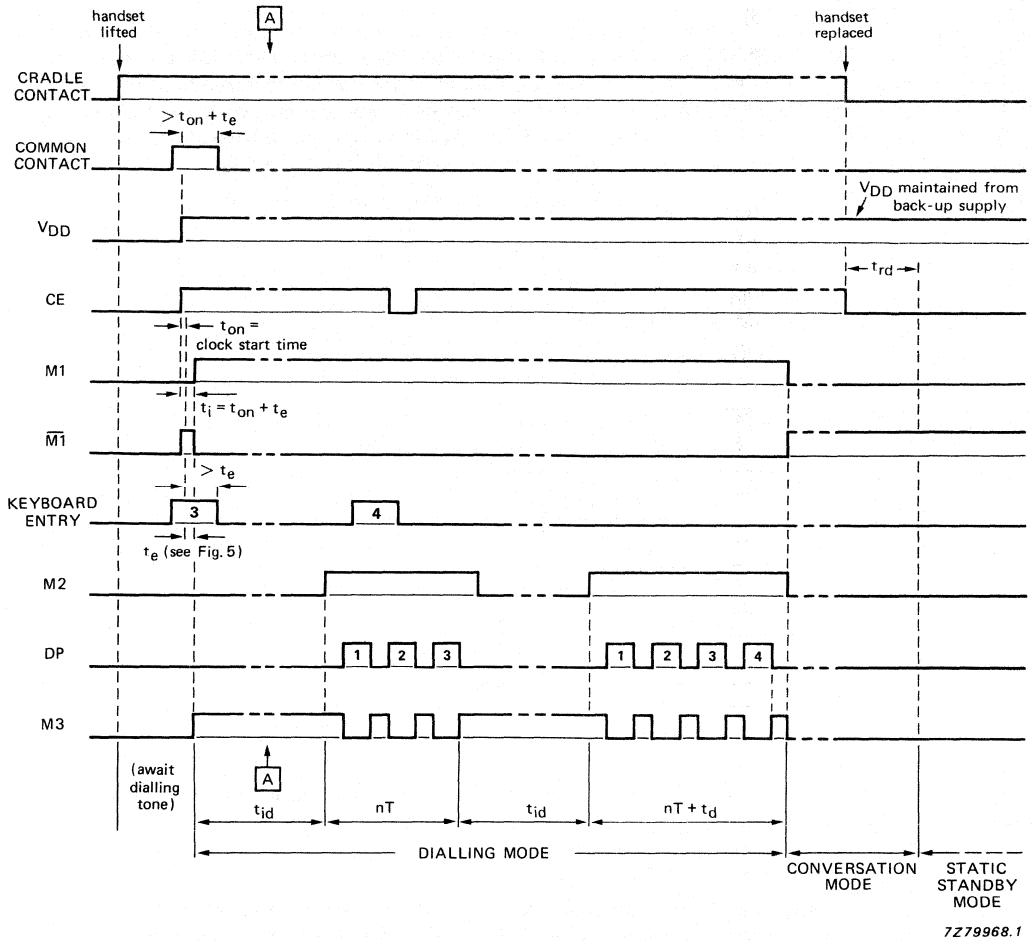


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function (HOLD)

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM to be converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see next section).

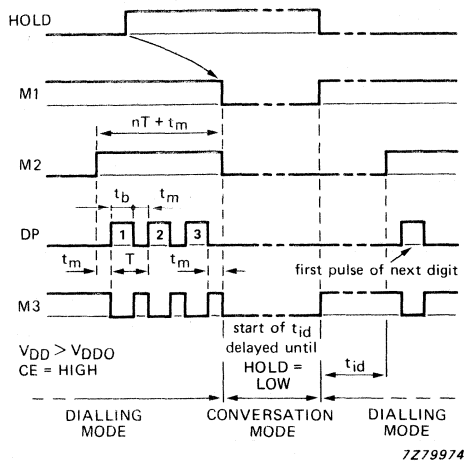


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

Access pause system (APO, HOLD/APO, APR)

Access pauses can be stored at appropriate positions in the RAM during the original entry of a number. As soon as the access pause code is read from the RAM during redial, the access pause output (APO) goes HIGH. The APO can be used to initiate an access pause by making HOLD = HIGH so that dialling is interrupted. In some ICs of this family, the HOLD and APO functions are connected internally to a common pin. This pin (HOLD/APO) can be used as an output, or forced as an input (e.g. by an external tone recognizer). With other ICs of the family, the access pause system is disabled completely by an Access Pause Reset (APR) that is set HIGH internally and prevents access pauses being reproduced during redial.

Storing access pauses during dialling (AAE)

Access pauses can be stored in one or both of the following ways:

- Manually by pressing the access pause key (*). The number of access pauses that can be stored in this way is limited only by the capacity of the RAM (digits + access pauses $\leqslant 23$).
- Automatically when AAE is HIGH (see Fig. 9) an access pause is stored automatically in the RAM during the original entry after all the digits so far entered have been transmitted (when M1 goes LOW, see Fig. 6). The maximum number of access pause codes that can be entered in this manner is either one or two, depending on the type of IC.

Note that if AAE is HIGH for automatic insertion and access pauses are inserted manually, the circuit automatically adds an access pause code after the number. This increases the RAM digit-count by one and reduces the maximum number of digits to 22 (including actual access pauses). The same would happen if the maximum number of access pauses for automatic entry is not reached before the end of the number.

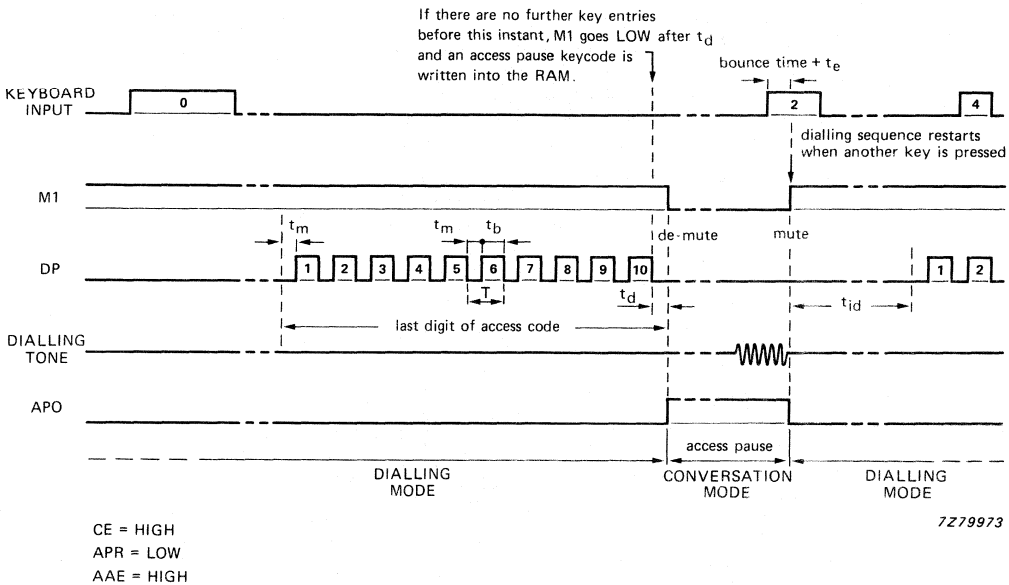


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Terminating access pauses during redial (APR, APD)

If APO is connected to HOLD, there are three ways of terminating access pauses during redial (see Fig. 10):

- Manually by pressing the redial key before t_{ap} expires.
- Automatically if the built-in time t_{ap} expires; APO, and also HOLD, then go LOW so that the next digit will be dialled. With the Access Pause Delay (APD) select input, t_{ap} can be set to one of two values. With ICs that do not terminate access pauses in this way, t_{ap} is virtually infinity.
- By making APR = HIGH before t_{ap} expires e.g. with an external tone recognizer, see Fig. 11).

Another method of terminating access pauses during redial is by connecting APO to HOLD via a latching device. This allows access pauses to be longer than the time t_{ap}. Fig. 12 shows a tone recognizer which automatically terminates access pauses upon receipt of the access tone, regardless of whether it occurs before or after the expiry of t_{ap}.

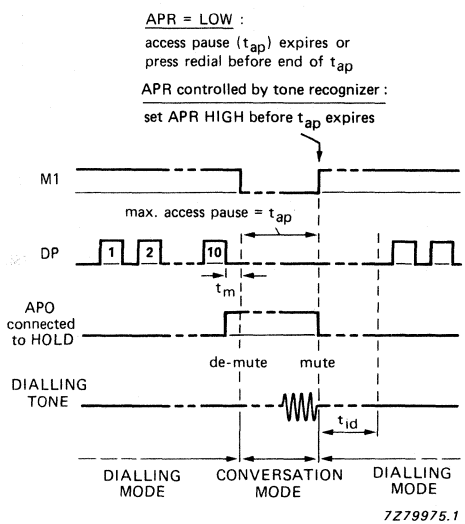


Fig. 10 Timing diagram showing access pause reset for APR = LOW, or for APR controlled by a tone recognizer.

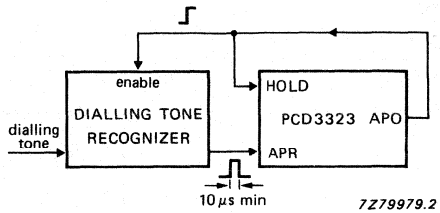


Fig. 11 Circuit for automatic termination of an access pause during redialling by using a tone recognizer to set APR to HIGH for more than 10 μs.

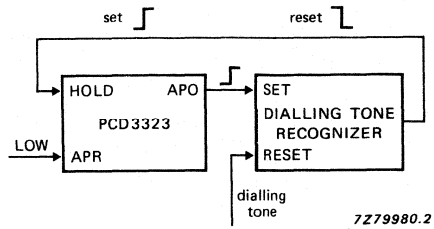


Fig. 12 Circuit for automatically shortening or lengthening an access pause under the control of a tone recognizer. For timing see Fig. 13.

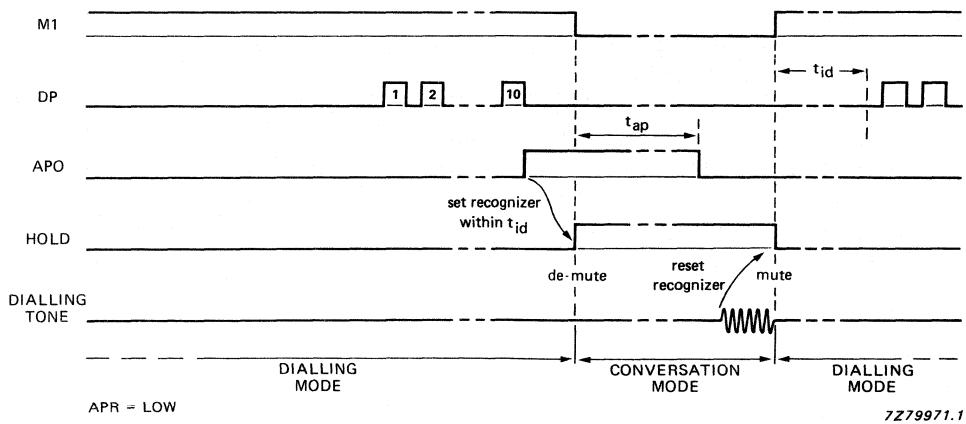


Fig. 13 Timing diagram for the circuit of Fig. 12.

FAMILY RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0,5	8,0	V
Voltage on any pin		V_I	V_{SS}−0,3	V_{DD}+0,3	V
Operating ambient temperature range		T_{amb}	−25	+70	°C
Storage temperature range		T_{stg}	−55	+125	°C

FAMILY CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters f_{osc} = 3,58 MHz and R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage	T_{amb} = −25 to +70 °C	V_{DD}	2,5	3,0	6,0	V
Standby supply voltage (note 1)	T_{amb} = −25 to +70 °C	V_{DDO}	1,8	–	6,0	V
Operating supply current	CE = V_{DD}; notes 2,3	I_{DD}	–	40	–	μA
	V_{DD} = 6 V; CE = V_{DD}; notes 2,3	I_{DD}	–	50	100	μA
Standby supply current	CE = V_{SS}; note 2	I_{DDO}	–	1	2	μA
	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C	I_{DDO}	–	–	2	μA
Input voltage LOW	1,8 V ≤ V_{DD} ≤ 6 V	V_{IL}	–	–	0,3xV_{DD}	
Input voltage HIGH	1,8 V ≤ V_{DD} ≤ 6 V	V_{IH}	0,7xV_{DD}	–	–	
CE input leakage current LOW	CE = V_{SS}	$-I_L$	–	–	50	nA
HIGH	CE = V_{DD}	I_{IH}	–	–	50	nA
M/S, APR pull-up input current	V_I = V_{SS}	$-I_L$	30	100	300	nA
IDP, F01, F02, HOLD, AAE, APD, RDS, pull-down input current	V_I = V_{DD}	I_{IH}	30	100	300	nA

parameter	conditions	symbol	min.	typ.	max.	unit
Matrix keyboard operation						
Keyboard current	COL connected to ROW; CE = HIGH	I_K	–	10	–	μA
Keyboard 'ON' resistance	contact 'ON' (note 4)	R_{KON}	–	–	500	Ω
Keyboard 'OFF' resistance	contact 'OFF' (note 4)	R_{KOFF}	1	–	–	MΩ
Other keyboard operation						
Input current for COLn 'ON'	V_I = 1,5 to 3 V	I_{IH}	–	–	30	μA
Input current for ROWn 'ON'	V_I = 0 to 2,5 V	$-I_{IL}$	10	–	–	μA
Input current ROWn	$V_I = V_{SS}$	$-I_I$	–	–	0,7	mA
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	V_{OL} = 0,5 V	I_{OL}	0,7	1,5	3,2	mA
source current	V_{OH} = 2,5 V	$-I_{OH}$	0,65	1,3	2,7	mA
Outputs CL, APO						
sink current	V_{OL} = 0,5 V	I_{OL}	50	130	300	μA
source current	V_{OH} = 2,5 V	$-I_{OH}$	45	110	250	μA

Notes to family characteristics

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between OSC IN and OSC OUT pins < 3 pF.
4. Guarantees correct keyboard operation.

FAMILY TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

parameter	conditions	symbol	min.	typ.	max.	unit
Clock start-up time	CE: from V_{SS} to V_{DD} see note	t_{on}	–	4	–	ms
APR hold time	see Fig. 11	t_{APRH}	10	–	–	μs

Note to family timing data

Stray capacitance between OSC IN and OSC OUT < 3 pF.

DEVELOPMENT DATA

FAMILY CURVES

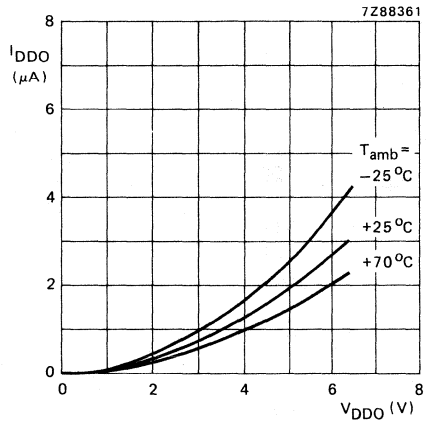


Fig. 14 Standby supply current as a function of standby supply voltage.

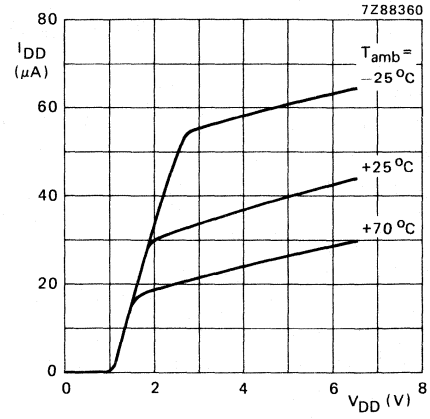


Fig. 15 Operating supply current as a function of operating supply voltage.

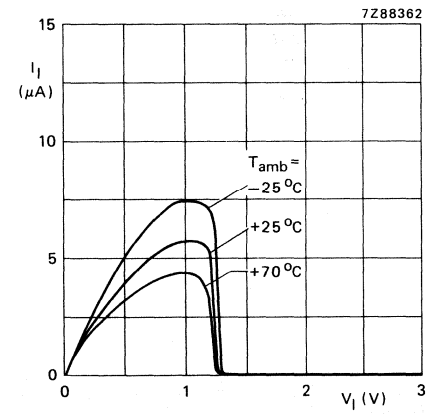


Fig. 16 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

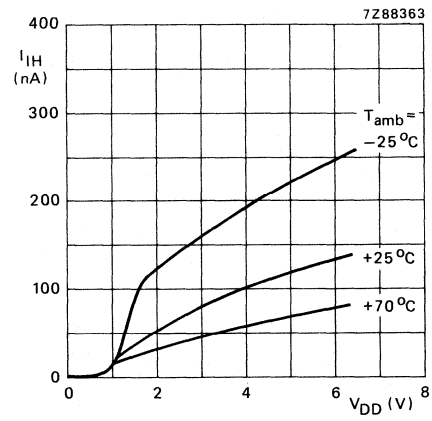


Fig. 17 Pull-down input current as a function of supply voltage; $V_I = V_{DD}$.

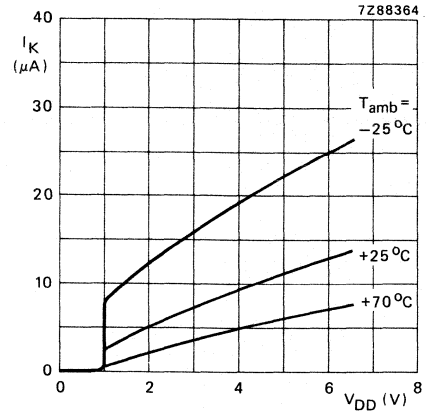


Fig. 18 Keyboard current as a function of supply voltage; COL-pins connected to ROW-pins.

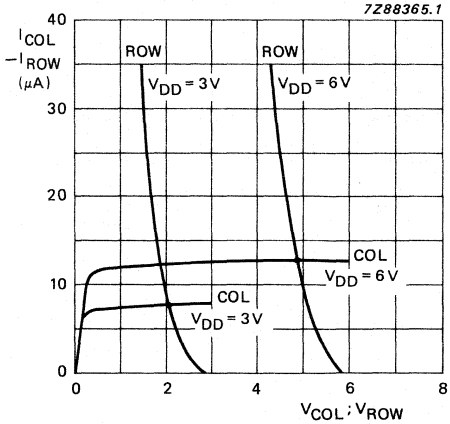


Fig. 19 Keyboard input characteristics at T_{amb} = 25 °C.

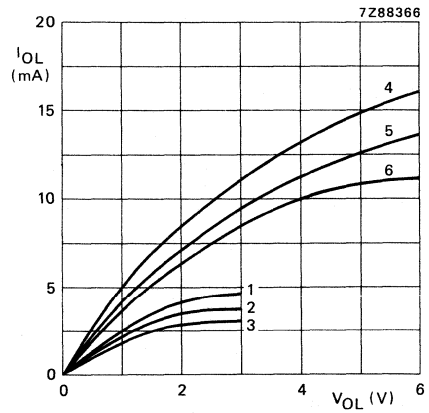


Fig. 20 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

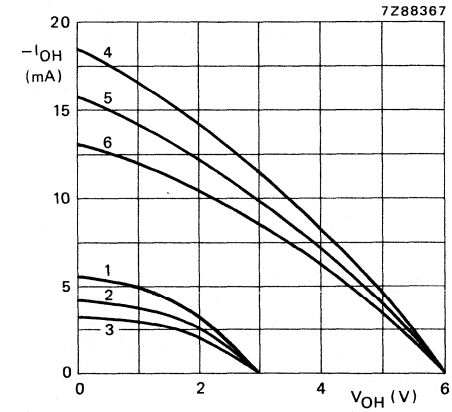


Fig. 21 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Key to Figs 20 and 21

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	curve 1	curve 4
+25 °C	curve 2	curve 5
+70 °C	curve 3	curve 6

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE

PCD3320 specification

Inputs that are not available are defined internally as follows:

F02 = RDS = IDP = AAE = APD = LOW M/S = APR = HIGH

Outputs not available are CL, M2 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M3	AND-function of mute (M1) and inverted dialling pulse (DP) outputs
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

PCD3320 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

parameter	conditions	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)	unit
Dialling pulse frequency	see note	f_{DP}	10,13	932,2	Hz
Dialling pulse period; $1/f_{DP}$	Figs 6 and 7	T_{DP}	98,7	1,073	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	303,9	27965	Hz
Break time; $3/5 \times T_{DP}$	Fig. 6	t_b	59,2	0,644	ms
Make time; $2/5 \times T_{DP}$	Fig. 6	t_m	39,5	0,429	ms
Inter-digit pause: $8 \times T_{DP}$	Figs 6 and 7	t_{id}	790	8,58	ms
Reset delay time; $1,6 \times T_{DP}$	Figs 5, 6 and 7	t_{rd}	158	1,7	ms
Prepulse duration; $1/3 \times T_{DP}$	Figs 6 and 7	t_d	33	0,358	ms
Debounce time					
min. $4/30 \times T_{DP}$	Fig. 5	$t_{e\ min}$	13,2	0,143	ms
max. $1/6 \times T_{DP}$	Fig. 5	$t_{e\ max}$	16,5	0,179	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	4	ms

Note

f_{DP} is exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

PCD3321 specification

The PCD3321 is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for Private Automatic Branch Exchange (PABX) systems. Two access pauses can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

RDS = IDP = APD = APR = LOW AAE = HIGH

Outputs not available are CL, $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 — inputs giving selection between one of the three dialling speeds or the test speed

HOLD/APO — input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)

M/S — input for M/S ratio selection to 3:2 or 2:1

PCD3321 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

parameter	conditions	symbol	F01: LOW F02: LOW	HIGH HIGH	LOW HIGH	HIGH (test mode) LOW	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10,13	15,54	19,42	932,2	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98,7	64,4	51,5	1,073	ms
Clock pulse frequency; 30 x f_{DP}		f_{CL}	303,9	466,1	582,6	27965	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2, 3	t_b	59,2	38,6	30,9	0,644	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2, 3	t_m	39,5	25,8	20,6	0,429	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65,8	42,9	34,6	0,715	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32,9	21,5	17,2	0,358	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	8,58	ms
Reset delay time; 1,6 x T_{DP}		t_{rd}	158	103	82,4	1,72	ms
Access pause time; 32 $T_{DP}-t_m-1/f_{CL}$		t_{ap}	3,12	2,03	1,63	0,034	s

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3321 timing data (continued)

parameter	conditions	symbol	F01: LOW HIGH LOW HIGH (test mode) F02: LOW HIGH HIGH LOW					unit
Prepulse duration; 1/3 x T_{DP}		t_d	33	21,5	17,2	0,358		ms
Debounce time								
min. 4/30 x T_{DP}		$t_{e\ min}$	13,2	8,58	6,87	0,143		ms
max. 1/6 x T_{DP}		$t_{e\ max}$	16,5	10,7	8,58	0,179		ms
Initial data time (typ.); $t_{on} + t_e$		t_i	18	14	12	4		ms

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3322 specification

Inputs that are not available are defined internally as follows:

F02 = RDS = IDP = AAE = APD = LOW M/S = APR = HIGH

Outputs not available are CL, M3 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M2	strobe; HIGH during pulsing of a digit, LOW during an inter-digit pause
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

PCD3322 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

parameter	conditions	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)	unit
Dialling pulse frequency	see note	f_{DP}	10,13	932,2	Hz
Dialling pulse period; $1/f_{DP}$	Figs 6 and 7	T_{DP}	98,7	1,073	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	303,9	27965	Hz
Break time; $3/5 \times T_{DP}$	Fig. 6	t_b	59,2	0,644	ms
Make time; $2,5 \times T_{DP}$	Fig. 6	t_m	39,5	0,429	ms
Inter-digit pause; $8 \times T_{DP}$	Figs 6 and 7	t_{id}	790	8,58	ms
Reset delay time; $1,6 \times T_{DP}$	Figs 5, 6 and 7	t_{rd}	158	1,7	ms
Prepulse duration; $1/3 \times T_{DP}$	Figs 6 and 7	t_d	33	0,358	ms
Debounce time					
min. $4/30 \times T_{DP}$	Fig. 5	$t_{e\ min}$	13,2	0,143	ms
max. $1/6 \times T_{DP}$	Fig. 5	$t_{e\ max}$	16,5	0,179	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	4	ms

Note

f_{DP} is exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

CHARACTERISTICS PER TYPE (continued)

PCD3323 specification

The PCD3323 includes many additional features that make it ideal for sophisticated PABX systems. Two access pauses can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Features additional to the common family specification are:

AAE	automatic access pause enable
APD	input for selecting access pause duration
APO	access pause output
CL	clock output
F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed
HOLD	input that interrupts dialling
IDP	input for selection of inter-digit pause duration
$\overline{M1}$	inverted mute output
M2	strobe; HIGH during pulsing of a digit, LOW during an inter-digit pause
M3	AND-function of mute (M1) and inverted dialling pulse (DP) outputs
M/S	input for M/S ratio selection to 3:2 or 2:1
RDS	input for selecting reset delay time

DEVELOPMENT DATA

PCD3323 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

parameter	conditions	symbol	F01: LOW F02: LOW	HIGH HIGH	LOW HIGH	HIGH (test mode) LOW	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10,13	15,54	19,42	932,2	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98,7	64,4	51,5	1,073	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	303,9	466,1	582,6	27965	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_b	59,2	38,6	30,9	0,644	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_m	39,5	25,8	20,6	0,429	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	t_b	65,8	42,9	34,6	0,715	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	t_m	32,9	21,5	17,2	0,358	ms
Inter-digit pause; $8 \times T_{DP}$	I_{DP} = LOW	t_{id}	790	515	412	8,58	ms
$9 \times T_{DP}$	I_{DP} = HIGH	t_{id}	888	579	463	9,65	ms
Reset delay time; $1,6 \times T_{DP}$	RDS = LOW	t_{rd}	158	103	82,4	1,72	ms
$3,2 \times T_{DP}$	RDS = HIGH	t_{rd}	316	206	165	3,43	ms
Access pause time; $32 \times T_{DP} - t_m - 1/f_{CL}$	APD = LOW	t_{ap}	3,12	2,03	1,63	0,034	s
$64 \times T_{DP} - t_m - 1/f_{CL}$	APD = HIGH	t_{ap}	6,28	4,09	3,28	0,069	s
Prepulse duration; $1/3 \times T_{DP}$		t_d	33	21,5	17,2	0,358	ms
Debounce time min. $4/30 \times T_{DP}$		$t_{e\,min}$	13,2	8,58	6,87	0,143	ms
max. $1/6 \times T_{DP}$		$t_{e\,max}$	16,5	10,7	8,58	0,179	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	14	12	4	ms

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3324 specification

The PCD3324 is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. One access pause can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined als follows:

RDS = IDP = APD = APR = LOW AAE = HIGH

Outputs not available are CL, $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
M/S	input for M/S ratio selection to 3:2 or 2:1

DEVELOPMENT DATA

PCD3324 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

parameter	conditions	symbol	F01: LOW F02: LOW	HIGH HIGH	LOW HIGH	HIGH (test LOW mode)	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10,13	15,54	19,42	932,2	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98,7	64,4	51,5	1,073	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	303,9	466,1	582,6	27965	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_b	59,2	38,6	30,9	0,644	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_m	39,5	25,8	20,6	0,429	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	t_b	65,8	42,9	34,6	0,715	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	t_m	32,9	21,5	17,2	0,358	ms
Inter-digit pause; $8 \times T_{DP}$		t_{id}	790	515	412	8,58	ms
Reset delay time; $1,6 \times T_{DP}$		t_{rd}	158	103	82,4	1,72	ms
Access pause time; $32\,T_{DP} - t_m - 1/f_{CL}$		t_{ap}	3,12	2,03	1,63	0,034	s
Prepulse duration; $1/3 \times T_{DP}$		t_d	33	21,5	17,2	0,358	ms
Debounce time min. $4/30 \times T_{DP}$		$t_{e\,min}$	13,2	8,58	6,87	0,143	ms
max. $1/6 \times T_{DP}$		$t_{e\,max}$	16,5	10,7	8,58	0,179	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	14	12	4	ms

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3325A specification

The PCD3325A is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. Access pauses can be stored via the keyboard during the original entry of a number (there is no automatic storage of access pauses). The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

RDS = IDP = APD = APR = AAE = LOW

Outputs not available are CL, $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
M/S	input for M/S ratio selection to 3:2 or 2:1

DEVELOPMENT DATA

PCD3325A timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

parameter	conditions	symbol	F01: LOW F02: LOW	HIGH HIGH	LOW HIGH	HIGH (test LOW mode)	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10,13	15,54	19,42	932,2	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98,7	64,4	51,5	1,073	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	303,9	466,1	582,6	27965	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_b	59,2	38,6	30,9	0,644	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_m	39,5	25,8	20,6	0,429	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	t_b	65,8	42,9	34,6	0,715	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	t_m	32,9	21,5	17,2	0,358	ms
Inter-digit pause; $8 \times T_{DP}$		t_{id}	790	515	412	8,58	ms
Reset delay time; $1,6 \times T_{DP}$		t_{rd}	158	103	82,4	1,72	ms
Prepulse duration; $1/3 \times T_{DP}$		t_d	33	21,5	17,2	0,358	ms
Debounce time min. $4/30 \times T_{DP}$		$t_{e\ min}$	13,2	8,58	6,87	0,143	ms
max. $1/6 \times T_{DP}$		$t_{e\ max}$	16,5	10,7	8,58	0,179	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	14	12	4	ms

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3326 specification

The PCD3326 includes many additional features that make it ideal for PABX systems. Two access pauses can be stored automatically during the original entry of a number, or several stored via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

RDS = IDP = APR = LOW AAE = M/S = HIGH

Outputs not available are CL, $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
APD	input for selecting access pause duration

DEVELOPMENT DATA

PCD3326 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

parameter	conditions	symbol	F01: LOW F02: LOW	HIGH HIGH	LOW HIGH	HIGH (test LOW mode)	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10,13	15,54	19,42	932,2	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98,7	64,4	51,5	1,073	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	303,9	466,1	582,6	27965	Hz
Break time $3/5 \times T_{DP}$	note 2	t_b	59,2	38,6	30,9	0,644	ms
Make time; $2/5 \times T_{DP}$	note 2	t_m	39,5	25,8	20,6	0,429	ms
Inter-digit pause; $8 \times T_{DP}$		t_{id}	790	515	412	8,58	ms
Reset delay time; $1,6 \times T_{DP}$		t_{rd}	158	103	82,4	1,72	ms
Access pause time $32 \times T_{DP} - t_m - 1/f_{CL}$	APD = LOW or n.c.; (note 3)	t_{ap}	3,12	2,03	1,63	0,034	s
$64 \times T_{DP} - t_m - 1/f_{CL}$	APD = HIGH	t_{ap}	6,28	4,09	3,28	0,069	s
Prepulse duration; $1/3 \times T_{DP}$		t_d	33	21,5	17,2	0,358	ms
Debounce time min. $4/30 \times T_{DP}$		$t_{e\,min}$	13,2	8,58	6,87	0,143	ms
max. $1/6 \times T_{DP}$		$t_{e\,max}$	16,5	10,7	8,58	0,179	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	14	12	4	ms

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark/space ratio = 3:2.
3. In the n.c. (not connected) condition, the input is drawn to the LOW state by the internal pull-down current.

CHARACTERISTICS PER TYPE (continued)

PCD3327 specification

The PCD3327 contains an oscillator with sufficient gain to provide oscillation when using an inexpensive 455 kHz ceramic resonator. Two additional capacitors are required as shown in Fig. 22. Alternatively, the OSC IN pin may be driven from an external 455 kHz clock signal.

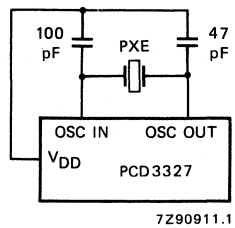


Fig. 22 PCF3327 oscillator circuit.

This IC is pin-compatible with the DF320 and MT4320 types and includes additional features that make it ideal for PABX systems. The circuit allows several access pauses to be stored via the keyboard and regenerates the access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

RDS = IDP = APD = APR = AAE = LOW

Outputs not available are CL, $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
M/S	input for M/S ratio selection to 3:2 or 2:1

DEVELOPMENT DATA

PCD3327 timing data

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

parameter	conditions	symbol	F01: LOW F02: LOW	HIGH HIGH	LOW HIGH	HIGH (test LOW mode)	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10,3	15,8	19,7	948	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	97	63	51	1,05	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CL}	309	474	592	28438	Hz
Break time; $3/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_b	58	38	30	0,63	ms
Make time; $2/5 \times T_{DP}$	M/S = HIGH or n.c.; notes 2, 3	t_m	39	25	20	0,42	ms
Break time; $2/3 \times T_{DP}$	M/S = LOW note 4	t_b	65	42	34	0,70	ms
Make time; $1/3 \times T_{DP}$	M/S = LOW note 4	t_m	32	21	17	0,35	ms
Inter-digit pause; $8 \times T_{DP}$		t_{id}	776	506	405	8,4	ms
Reset delay time; $1,6 \times T_{DP}$		t_{rd}	155	101	81	1,7	ms
Access pause time; $32\,T_{DP} - t_m - 1/f_{CL}$		t_{ap}	3,12	2,03	1,63	0,034	s
Prepulse duration; $1/3 \times T_{DP}$		t_d	32	21	17	0,35	ms
Debounce time min. $4/30 \times T_{DP}$		$t_{e\,min}$	13	8,4	6,7	0,14	ms
max. $1/6 \times T_{DP}$		$t_{e\,max}$	16	10,5	8,4	0,18	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	18	14	12	4	ms

Notes

1. Exactly 10 Hz with 441,6 kHz PXE ceramic resonator.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

CMOS REPERTORY DIALLER TELEPHONE SET CONTROLLER

GENERAL DESCRIPTION

The PCD3341 is a low threshold voltage IC fabricated in CMOS. It is designed to control display, redial and repertory dialling in a telephone set. The IC has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). The architecture of the PCD3341 is identical to that of the PCD3343. It comprises an 8-bit CPU, 224 RAM bytes and 3K ROM bytes (the ROM is already programmed). The operating supply voltage is 2,5 to 6,0 V with a low current consumption in all operating modes: standby, conversation and dialling modes.
Up to 18 digits and 2 manual access pauses can be stored for redial, extended redial and direct dial purposes together with on-chip storage for 10 repertory numbers.
For expansion of the system the PCD3341 provides a two wire serial input/output port, in accordance with the I^2C bus specifications, to control the DTMF tone generator, LCD drivers and additional RAMs for additional repertory numbers.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Direct dialling (emergency call)
- On-chip storage for 10 repertory dial numbers
- 18-digit capacity for each autodial memory
- Flash or register recall
- Access pause generation and termination
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity
- Extention possible with external RAM for up to 110 repertory dial numbers
- Uses standard 4 x 4 keyboard (single or double contact)
- Additional 10-digits first in first out memory, for infinite long numbers control an LCD via the I^2C bus.
- Four extra function keys: program/autodial, flash, redial, access pause
- Keyboard expansion possible for 10 separated repertory dialled numbers
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Six diode or strap functions: mark-to-space ratio, tone burst time, inter-digit pause time, access pause time, normal or expanded keyboard, normal or direct dialling

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DD}	min. 1,8	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DDC}	typ. 270	μA
dialling mode	I_{DDD}	typ. 600	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3341P: 28-lead DIL; plastic (SOT117).
PCD3341T: 28-lead mini-pack; plastic (SO28; SOT136A).

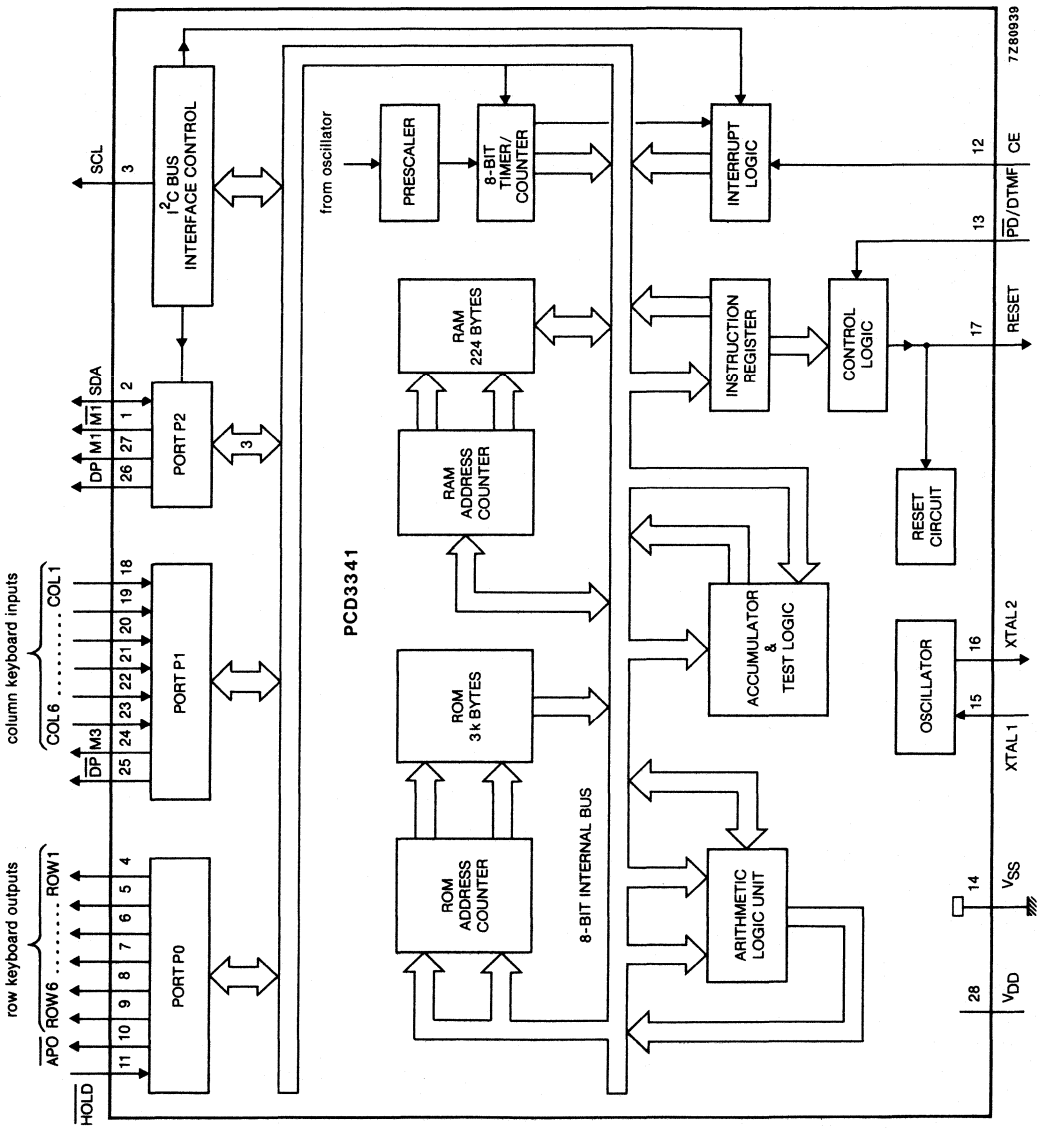


Fig. 1 Block diagram.

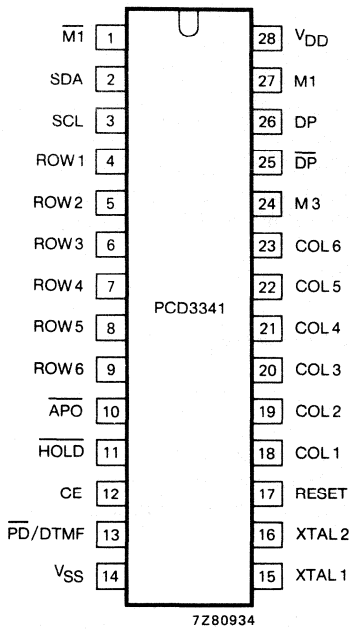


Fig. 2 Pinning diagram.

PINNING

1	$\overline{M1}$	inverted output of M1
2	SDA	serial data
3	SCL	serial clock
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	ROW 6	
10	$\overline{APO}$	access pause output
11	$\overline{HOLD}$	hold input
12	CE	chip enable input
13	$\overline{PD}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	input to on-chip oscillator
16	XTAL 2	output from on-chip oscillator
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	COL 5	
23	COL 6	
24	M3	muting output
25	$\overline{DP}$	inverted pulse dialling output
26	DP	pulse dialling output
27	M1	muting output
28	V_{DD}	positive supply

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

Power supply must be retained for data storage.

Clock oscillator (XATL 1; XTAL 2)

The time base for the PCD3341 is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between XTAL 1 and XTAL 2. The oscillator starts when V_{DD} reaches the operating voltage level and CE = HIGH. The output XTAL 2 can be used to drive the oscillator input of the PCD3312.

Chip Enable (CE)

This active HIGH input is used to initialize part of the system, to select the operational or standby mode and to handle line power breaks.

Pulse dialling outputs (DP; $\overline{DP}$)

DP output drives an external switching transistor or relay in pulse dialling mode. This output is also used to pulse out a calibrated FLASH pulse (recall register) of 90 ms duration as soon as the keyboard input FLASH is activated by depressing the key F. The FLASH function acts like CE with respect to redial.

Muting outputs (M1; $\overline{M1}$; M3)

M1 output is used for muting during the dialling sequence. For pulse dialling M1 goes HIGH with the first inter-digit pause and remains active for 33 or 40 ms (mark-to-space selection) following the last break pulse after the last digit held in store has been transmitted. In DTMF dialling, input $\overline{PD}$/DTMF is HIGH. M1 is HIGH as long as two out of the eight frequency signals are sent, then remains HIGH for an additional 80 ms (hold-over time).
$\overline{M1}$ output is the inverted output of M1.
M3 output is an AND function with $\overline{DP}$ and M1 as input, used for direct drive of a switching transistor for dialling pulses and muting.

Hold input ($\overline{HOLD}$); **access pause output** ($\overline{APO}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during an inter-digit pause.
The hold function facilitates an extra time delay during dialling under control of external circuits (dialling tone recognizer). In the hold state ($\overline{HOLD}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode. The $\overline{HOLD}$ input can be controlled by the access pause output (APO) directly or indirectly via a dialling tone recognizer (see Fig. 3). The tone recognizer automatically terminates access pauses upon receipt of the access tone, regardless of whether this occurs during or after the access pause time (t_{ap}). The $\overline{APO}$ output will go LOW when an access pause is recognized.

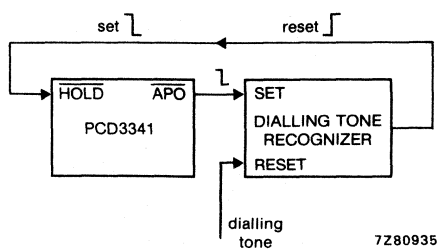


Fig. 3 Automatic variation of length of an access pause under control of a dialling tone recognizer.

Serial data (SDA); **serial clock** (see Fig. 8)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode, additional RAMs (PCD8570) for repertory dialling and LCD drivers (PCF8577). Both outputs require external pull-up resistors.

Keyboard inputs/outputs (COL 1 to 6; ROW 1 to 6)

The sense column inputs COL 1 to COL 6 and the scanning row outputs ROW 1 to ROW 6 are directly connected to a 4 x 4 single contact keyboard matrix. The keyboard organization is shown in Fig. 4.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid. On-chip repertory dialling uses the 10 numeric numbers (no external RAM).
With extended repertory dialling 10 extra keys (M1 to M10) are used (on-chip or external RAM).
Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- AP manual access pause entry

Diode options (ROW 6)

Row 6 is added to the keyboard matrix to provide the following selections:

Mark-to-space ratio (M/S)
OFF M/S 3:2
ON M/S 2:1

Tone burst time (t_{tb})
OFF t_{tb} = 70 ms
ON t_{tb} = 100 ms

Inter-digit pause (IDP)
OFF IDP = 900 ms
ON IDP = 500 ms

Access pause time (t_{ap})
OFF t_{ap} = 1,5 s (DTMF); 3 s (PD)
ON t_{ap} = 2,5 s (DTMF); 5 s (PD)

Keyboard expansion (EKB)
OFF normal keyboard
ON expanded keyboard

Normal/direct call (N/D)
OFF normal call mode
ON direct call (emergency)

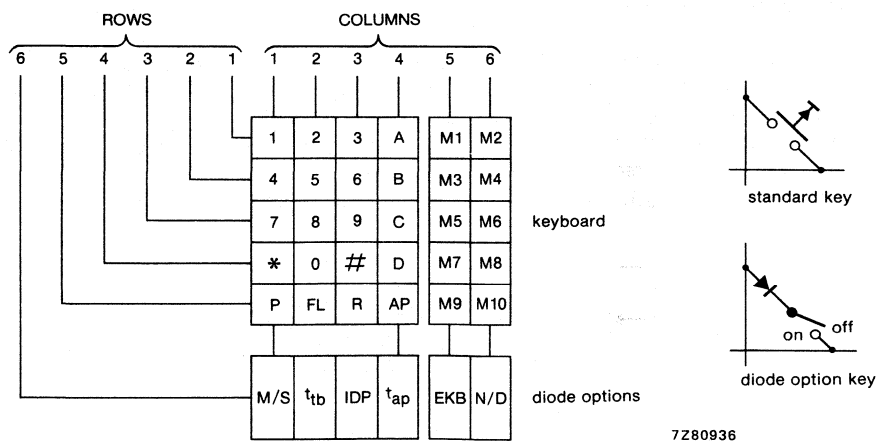


Fig. 4 Keyboard organization.

FUNCTIONAL DESCRIPTION (continued)

Dialling mode selection input ($\overline{PD}$/DTMF)

This input selects the dialling mode:

- $\overline{PD}$/DTMF = LOW selects pulse dialling
- $\overline{PD}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3341 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is disabled. In the standby mode the only current drawn is from a back up supply (battery or line powered), for memory retention, holding up to 13 call numbers for repertory and redialling.

Conversation mode

After the handset is lifted CE is activated and V_{DD} rises to the working voltage. M1 muting is inactive and speech or dial tone can be heard. With the oscillator operating the chip is ready to accept keyboard entries. Current consumption is $< 300\ \mu A$.

Dialling mode

The dialling mode starts with first valid keyboard entry when it initiates:

- a normal call of a newly dialled number
  or
- a repertory or redialling cycle of previously entered and stored numbers

The current consumption is $< 600\ \mu A$.

Pulse dialling ($\overline{PD}$/DTMF = LOW)

The keyboard entry initiates a recall from a previously stored number or is a simultaneous keying-in and pulsing-out activity, with storing for possible later recall. If in the recalled number or at keying-in the keys *, #, A, B, C, D keys are used these digits will not be transmitted. Normally, keying-in is faster than pulsing-out (fed from the redial register). Pulsing sequences start with M1 going HIGH followed by an inter-digit pause of 900 or 500 ms duration (diode option IDP), followed by a sequence of pulses corresponding to the present digit in store. Each pulse starts with a mark (line break) followed by space (line make).
The pulse period is 100 ms with a mark-to-space ratio of 3:2 or 2:1 (diode option). After transmission os a digit, the next digit will be processed again starting with an inter-digit pause. The pulsing is suspensed if $\overline{HOLD}$ goes LOW. It will be terminated if the current memory content has been transmitted or the handset is replaced (CE = LOW $< t_{rd}$). The pulses are available on the DP line.
After completion of the number string M1 goes LOW and the circuit changes from dialling mode to conversation mode.

Dual Tone Multi Frequency dialling ($\overline{PD}$/DTMF = HIGH)

The PCD3341 converts keyboard inputs into serial data, via the I^2 bus lines SDA and SCL, suitable for control of the PCD3312 DTMF tone generator. These tones are transmitted with minimum tone burst durations of 70, 70 ms. The maximum tone burst duration is equal to the key depression time. With redial and repertory dialling tones are automatically fed at a rate of 70, 70 ms. After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

DEVELOPMENT DATA

SYSTEM EXTENSION

The PCD3341 can control the extensions of a telephone set via its I²C bus. Both in DTMF dialling and pulse dialling, an extended repertory dialler provides more than 10 stored on-chip numbers and the indication on a L.C. display of all keys pressed (programming or dialling procedure).
The following ICs can be used in combination with the PCD3341:

- PCD3312 DTMF generator
- PCD8570 256 x 8 static CMOS RAM
- PCF8577 2 LCD drivers in LCD module

DTMF dialling

By using a PCD3312 DTMF generator with I²C bus interface, the PCD3341 may be extended to Dual Tone Multi Frequency dialling applications. This is selected when the input pin $\overline{PD}$/DTMF = HIGH. DTMF dialling is much faster than pulse dialling. Each keypad digit corresponds to a unique combination of two frequencies; one from a group of 4 high frequencies, and one from a group of 4 low frequencies. Both frequencies are applied simultaneously to the line.
The PCD3341 is capable of directly driving the PCD3312 oscillator.

Repertory dialling

If more than 10 stored numbers are required repertory dialling can be extended by the I²C bus lines and external CMOS RAMs (PCD8570) with serial interface. With a RAM capacity of 256 x 8 bits another 20 stored numbers can be added. A maximum of 5 external RAMs can be served by the PCD3341 directly. This provides a telephone with a total capacity of 110 (100) stored numbers.
The number of external RAMs connected on the I²C bus lines is automatically checked by the PCD3341 at initial turn-on.
To identify each RAM, the PCD8570 has 3 hardware address pins (A2, A1, A0) which allows a maximum of 8 RAMs to be connected.

Table 1 Repertory number organisation

PCD8570 address			Keyboard digit(s)	
A2	A1	A0	Without EKB	With EKB
0	0	0	10 to 29	00 to 19
0	0	1	30 to 49	20 to 39
0	1	0	50 to 69	40 to 59
0	1	1	70 to 89	60 to 79
1	0	0	90 to 99	80 to 99
PCD3341			00 to 09	M1 to M10

Display

To display the dialled phone number or programmed number the PCD3341 provides the signals to control a LC Display module using two PCD8577 duplex drivers. These signals are fed via the I²C bus lines.
In the dialling and programming modes the digits are displayed from right to left in the sequence entered by the keyboard. The access pause is indicated by the bar. If the number of digits exceeds 16, they drop out on the left side of the display.

OPERATING PROCEDURE

Initialization

At the first application of the standby power supply, the PCD3341 will clear the RAM in order to avoid a wrong content.
By lifting the handset the buffer capacitor for V_{DD} is charged to the operating voltage. CE will than be activated. Within start-up time the oscillator starts and the initialization program begins.

Automatic access pause setting

Before the start procedure, the system can also be initialized by setting the access pause system (e.g. for PABX applications). The circuit will automatically insert an access pause after recognition of access of a number within a digit group. This (or these) digit(s) must be programmed. Up to a maximum of 3 digits per group can be programmed.
The procedure is as follows:

- Depress and hold pushbutton P
- Press and release pushbutton R
- Enter 1, 2 or 3 digits as access digit for first group
- Release pushbutton P (only if no second group is required)
- Press and release pushbutton R
- Enter 1, 2 or 3 digits for second group
- Release pushbutton P

Apart from the procedure that automatically detectes and insertes access pause(s), a telephone number with up to 2 additional manually inserted access pauses can be dialled or programmed, by pressing button AP. In DTMF dialling mode each access pause has a duration of 1,5 or 2,5 seconds. In PD mode each access pause has a duration of 3 or 5 seconds.

Data entry

The debounce keyboard entries are written into the on-chip CMOS RAM in consecutive order.

Dialling

If the first pushbutton pressed is 0 to 9 in pulse dialling or 0-9, A to D, *, # in DTMF dialling, digits are entered into the redial register after initial clearing. During the data entry the circuit starts with the transmission of the call and is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed. Up to 18 digits can be stored in the redial register. After the main store overflows, a 10 digit First-In First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for the storage of new data. In this way, the total number that can be transmitted is unlimited, provided the key-in rate is not excessive. However, if the FIFO register overflows (more than 10 digits in store) further input will be ignored.

Redial

If the first digit entered is "REDIAL" R, the stored number in the redial register will be recalled and transmitted.
If the current content is less than 18 digits, new digits entered are appended automatically to the redial number. After the 18th digit has been entered the FIFO register will take over as previously described in the dialling section.

OPERATING PROCEDURE (continued)

Extended Redial

The dialled number is saved in the extended redial buffer if pushbutton P is the last key pressed before the handset is replaced.
By pressing and releasing pushbutton P followed by pressing and releasing pushbutton R, will cause the extended redial register to be recalled and transmitted in the same manner as by redial. If less than 18 digits are contained in the extended redial register, digits can be added until the total content is 18. After the 18th digit the FIFO register will take over as before. The original number is not affected by the new digits

Direct call/Emergency call

This is a diode option usually operated by a turn key switch. If set the programmed number will be dialled by pressing ANY key. In normal mode the turn key switch is positioned OFF with the diode option OFF.
Programmed is achieved by lifting the handset, depressing the P pushbutton with key in the OFF position, then turning the key switch to ON position (diode option ON). The required telephone number is now entered. Pushbutton P can now be released and the handset replaced.
After programming, the key switch can remain in the ON position (activating emergency call) or be switched off (normal mode). If the key switch is the ON position, emergency calling is possible by removing the handset and pressing ANY pushbutton.

Repertory dialling

The PCD3341 has an on-chip CMOS RAM to store up to ten 18 digit numbers, and can be extended up to 100 (110) numbers using external CMOS RAMs with 2-line serial interface. The circuit automatically checks the number of external RAMs. If no external RAM is connected the on-chip repertory is limited to 10 numbers. In this application the standard keypad (0 to 9) and one digit address can be used. With the diode option EKB (expanded keyboard) ON the extended keypad matrix (M1 to M10) can be used to access the on-chip repertory. If external RAMs are connected the capacity of the repertory can be increased up to 100 (110) numbers. In this application the standard keypad (0 to 9) and/or the extended keypad (M1 to M10) can be used to access the repertory (see Table 1).
Programming is possible only after the handset is lifted and no pushbutton is operated before P.
Programming is achieved by pushbutton P being continually depressed, entering the repertory address of one or two digits, followed by the number (including access digits) then releasing pushbutton P.
The designated telephone number, including access digits, is dialled after pressing pushbutton P followed by the address. With extended keypad a single address pushbutton is required. After transmission of the repertory sequence, it is possible to manually enter additional digits (see redial).

Successive repertory dialling during a call (chain dialling)

It is possible to dial more than one repertory number during one single telephone call.
The following procedures are possible:

- Redial, extended redial or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial followed by one or more repertory numbers

Note pad

Note pad provides the facility to store a number during conversation mode without dialling and muting. This number will be stored in the extended redial register and recalled with the extended redial procedure.
The programming procedure is as follows:

- Depress and release pushbutton P
- Depress and release pushbutton P
- Enter the telephone number
- Depress and release pushbutton P

If a wrond number is entered, correction is achieved by re-starting the programming procedure.

Memory clear

A built-in manually total clear facilitates resetting of the autodial RAM after servicing, maintenance or telephone set delivery.
The procedure is as follows:

- Hook-on, depress and keep depressed keys 2, 5, 8, 0
- Hook-off, release keys 2, 5, 8, 0

Table 2 Display indications

procedure	key procedure	display indication
Programming automatic access pauses after access digits	$\bar{P}$R00R9	P r – 0 0 – 9
dialling	004627530	0 0 – 4 6 2 7 5 3 0
redial	R	r = 0 0 – 4 6 2 7 5 3 0
Extended redial		
programming	004627530P	0 0 – 4 6 2 7 5 3 0 P
dialling	PR	P r = 0 0 – 4 6 2 7 5 3 0
emergency redial		
programming	N/D OFF, $\bar{P}$, N/D ON(+ TN)	P H – 0 0 – 4 6 2 7 5 3 0
dialling	N/D ON any key	H = 0 0 – 4 6 2 7 5 3 0
repertory programming	$\bar{P}$12004627530	P 1 2 – 0 0 – 4 6 2 7 5 3 0
programming	$\bar{P}$12004627530	P 1 2 – 0 0 – 4 6 2 7 5 3 0
dialling	P12	P 1 2 = 0 0 – 4 6 2 7 5 3 0
repertory with extended keyboard		
programming	$\bar{P}$ M1 004627530	P M 1 – 0 0 – 4 6 2 7 5 3 0
dialling	M1	M 1 = 0 0 – 4 6 2 7 5 3 0
note pad programming	PP0080808P	7 5 3 0 P P 0 0 – 8 0 8 0 8 0 P
note pad dialling	PR	0 0 – 8 0 8 0 8 0
error	incorrect key procedure	≡

Where: TN = telephone number
P = depress and release pushbutton P
$\bar{P}$ = depress pushbutton P continually during programming
R = depress and release pushbutton R

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute maximum System (IEC 134)

Supply voltage range (pin 28)	V_{DD}		−0,8 to 8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I	V_{SS} −0,8 V to V_{DD}	+ 0,8	V
Total power dissipation	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,57954 MHz; R_S = 50 Ω max.; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	3	6,0	V
Operating supply current					
conversation mode (CE = 1)	I_{DDC}	–	270	–	μA
dialling mode (CE = 1)	I_{DDD}	–	600	–	μA
Standby supply voltage (CE = 0)	V_{DDO}	1,8	3	6,0	V
Standby supply current (CE = 0)	I_{DDO}	–	–	2,5	μA
RESET I/O					
Switching level					
at $V_{DD} < V_{RESET}$	V_{RESET}	–	1,3	1,5	V
Sink current					
at $V_{DD} < V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	$0,3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0,7V_{DD}$	–	–	V
Input leakage current; CE					
at $V_I = V_{SS}$ to V_{DD}	$-I_{IL}$	–	–	100	nA
at CE = 1	I_{IL}	–	–	1	μA
Keyboard contact resistance					
Keyboard ON	R_{KON}	–	–	1	kΩ
Keyboard OFF	R_{KOFF}	100	–	–	kΩ
Outputs					
M1, $\overline{M1}$, M3, DP, $\overline{DP}$					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	–	1,5	–	mA
Output source current					
at V_{OH} = 2,6 V (push-pull)	$-I_{OH}$	–	1,5	–	mA
SDA, SCL					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	1,5	–	–	mA
Output source leakage current					
at V_{OH} = 0 to V_{DD} (open drain)	$-I_{OH}$	–	–	1	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs/Outputs					
COL 1 to 6, ROW 1 to 6, $\overline{HOLD}$, $\overline{APO}$					
Output sink current at V_{OL} = 0,4 V	I_{OL}	0,6	1,5	–	mA
Output source current at V_{OH} = 2,6 V	$-I_{OH}$	25	–	–	μA
Output source current at $V_{OH} = V_{SS}$	$-I_{OH}$	–	–	200	μA
TIMING (see Figs. 5, 6 and 7)					
Clock start-up time	t_{ON}	–	–	10	ms
Oscillator period	C_P	–	–	0,279	μs
Pulse dialling ($\overline{PD}$/DTMF input LOW; M/S diode OFF)					
Mark-to-space ratio 3:2					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	60,3	–	ms
Make time	t_m	–	40,3	–	ms
Mark-to-space ratio 2:1 (M/S diode ON)					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	67	–	ms
Make time	t_m	–	33,5	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	3	–	s
t_{ap} diode ON	t_{ap}	–	5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s
Inter-digit pause					
IDP diode OFF	t_{id}	–	892	–	ms
IDP diode ON	t_{id}	–	496	–	ms
Reset delay time	t_{rd}	–	160,9	180	ms
Reset delay time during access pause	t_{rd}	–	302	320	ms
Debounce time	t_e	13,5	–	–	ms
Flash pulse duration	t_{FL}	–	94	–	ms

parameter	symbol	min.	typ.	max.	unit
DTMF dialling ($\overline{PD}$/DTMF input HIGH; SDA timing via PCD3312)					
Tone transmission time (t_{tb} diode OFF)	t_t	–	74	–	ms
Tone break time	t_b	–	74	–	ms
Mute hold-over time during dialling	t_h	–	154	–	ms
Tone transmission time (t_{tb} diode ON)	t_t	–	101	–	ms
Tone break time	t_b	–	101	–	ms
Mute hold-over time during dialling	t_h	–	101	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	1,5	–	s
t_{ap} diode ON	t_{ap}	–	2,5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s

DEVELOPMENT DATA

Timing diagrams

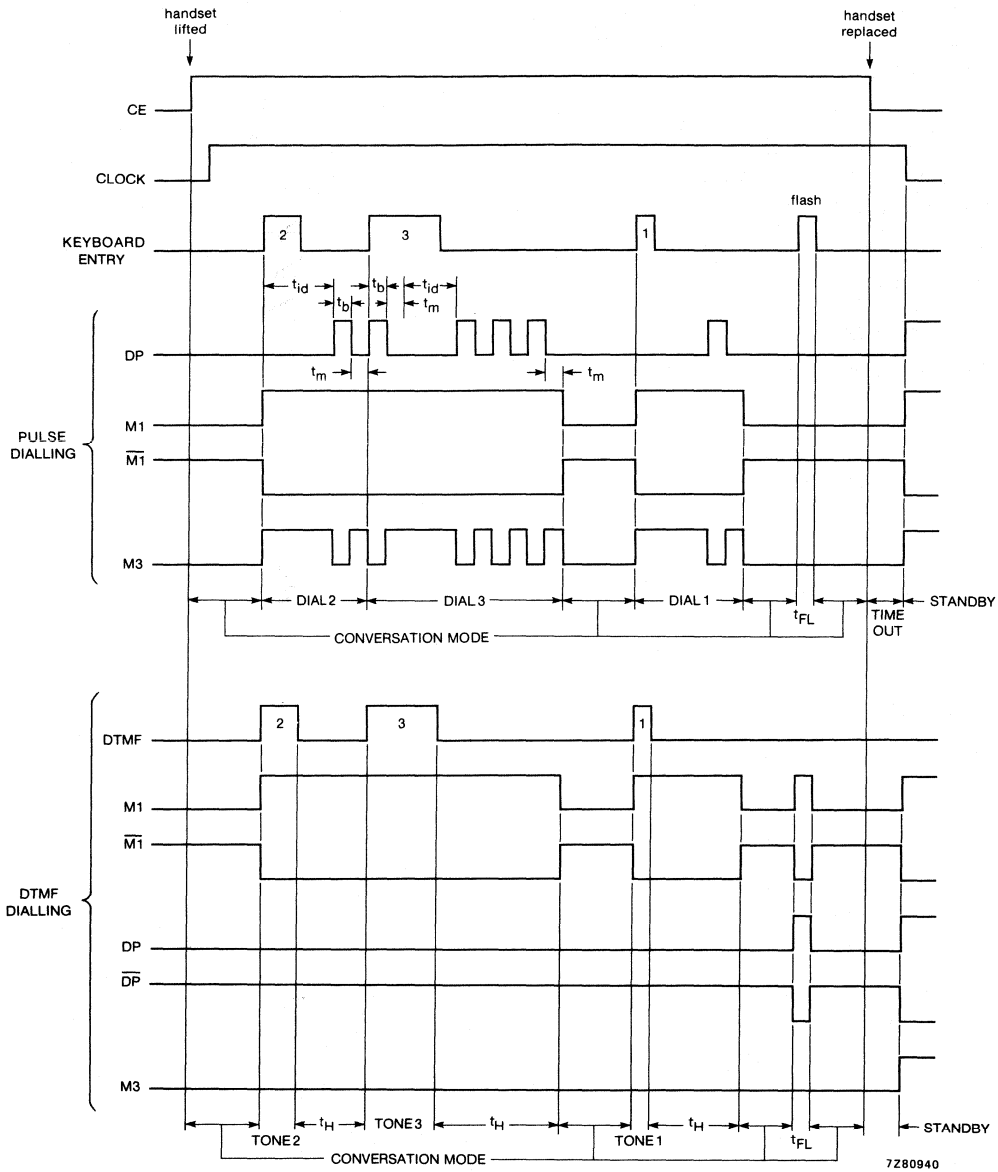


Fig. 5 Pulse dialling; DTMF dialling.

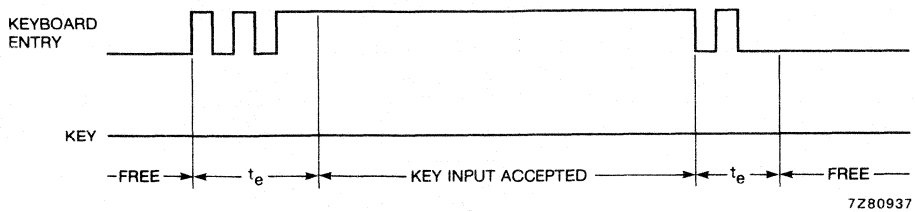


Fig. 6 Keyboard entry with noise debounced.

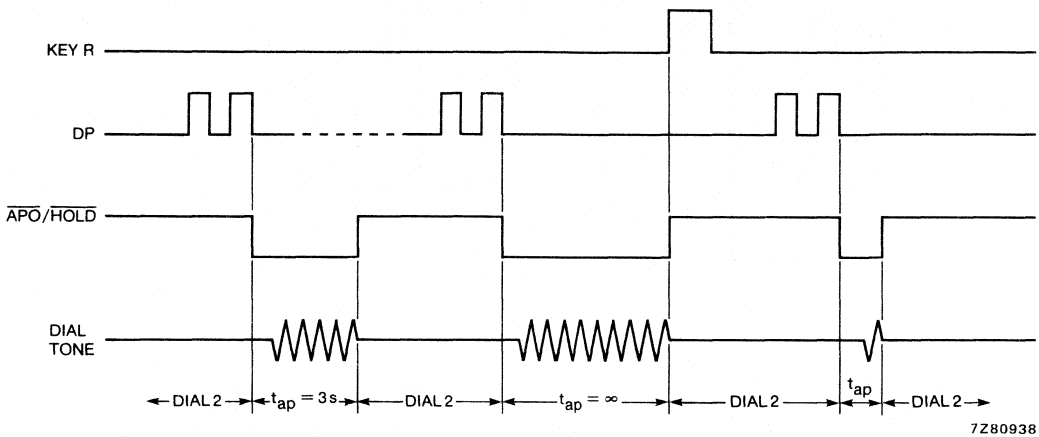


Fig. 7 Access pause with reset by; internal 3 s timer, key R, tone recognizer.

APPLICATION INFORMATION

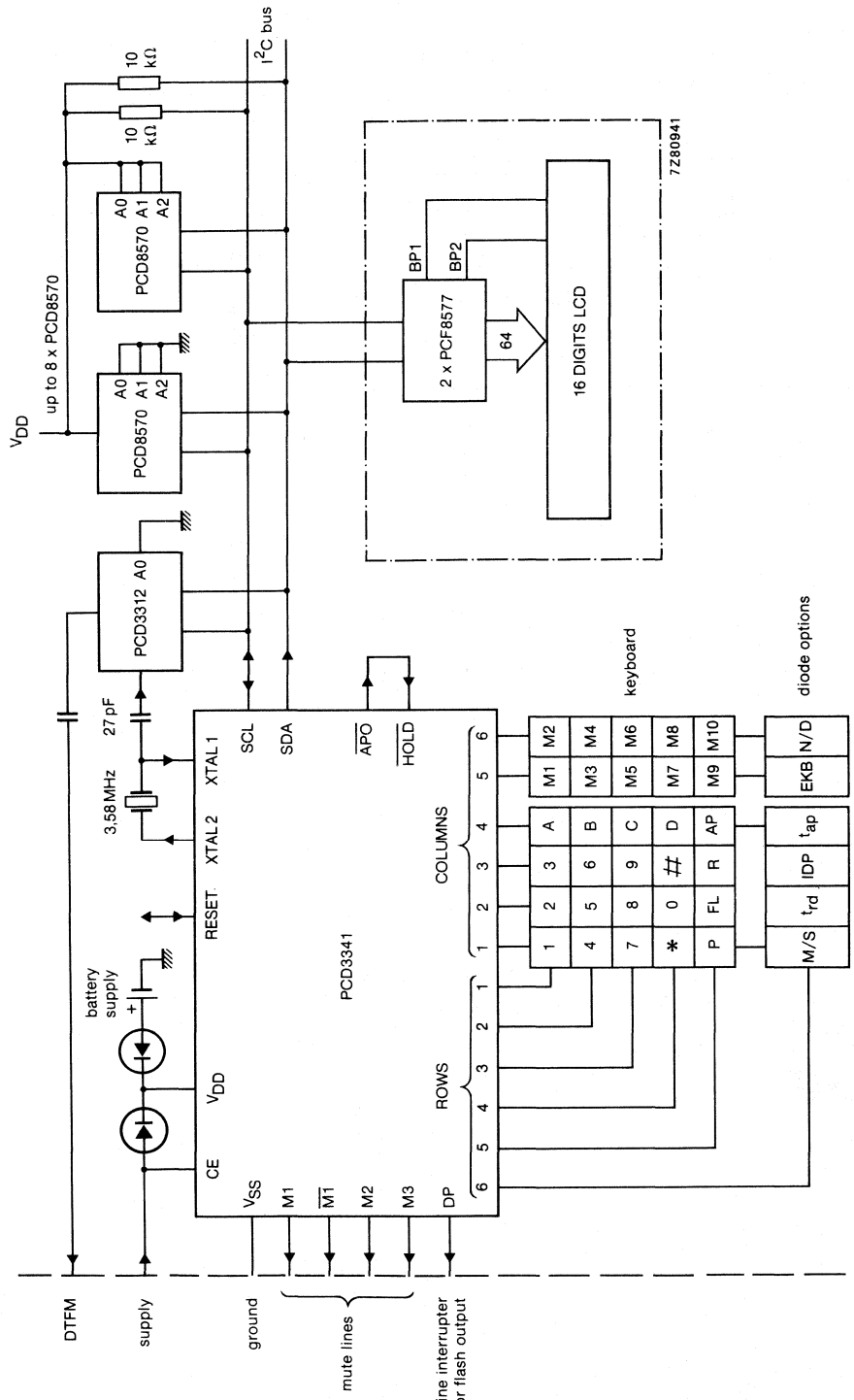


Fig. 8 PCD3341 in combination with PCD3312 (DTMF dialler), PCD8570 (2 K RAM) and PCF8577 (display drivers).

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS. It has special on-chip features for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3343P: 28-lead DIL; plastic (SOT117).
PCD3343D: 28-lead DIL; ceramic (CERDIP) (SOT135A).
PCD3343T: 28-lead mini-pack; plastic (SO28; SOT136A).

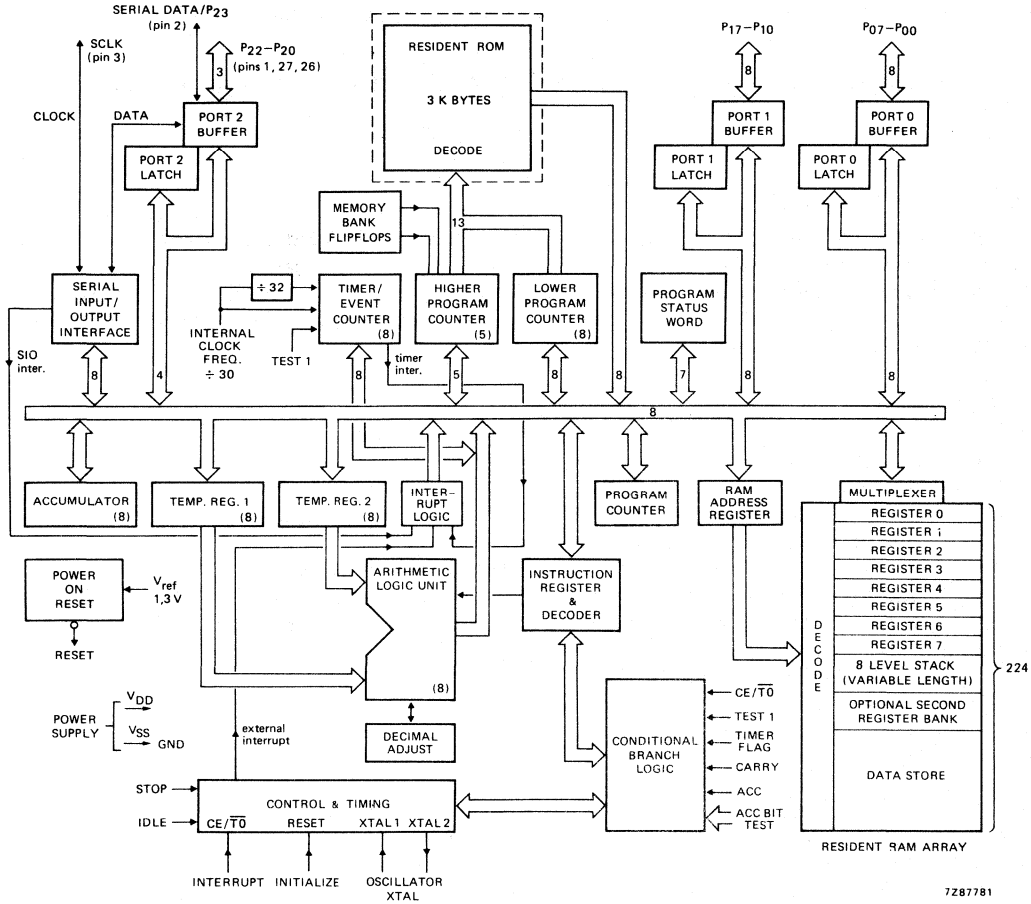
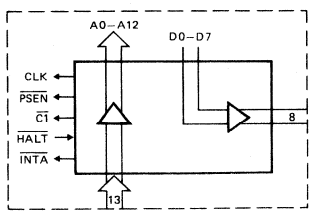
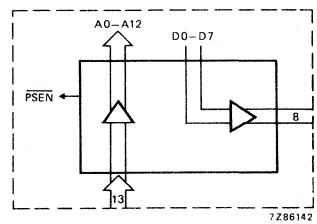


Fig. 1 Block diagram; PCD3343.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

The PCD3344 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3343 family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2048 ROM bytes
- 224 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, PCD3343 and PCD84C00)
- All instructions 1 or 2 cycles
- Clock frequency 3,58 MHz
- Single supply voltage from 2,5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3344P: 28-lead DIL; plastic (SOT117).
PCD3344T: 28-lead mini-pack; plastic (SO28; SOT136A).

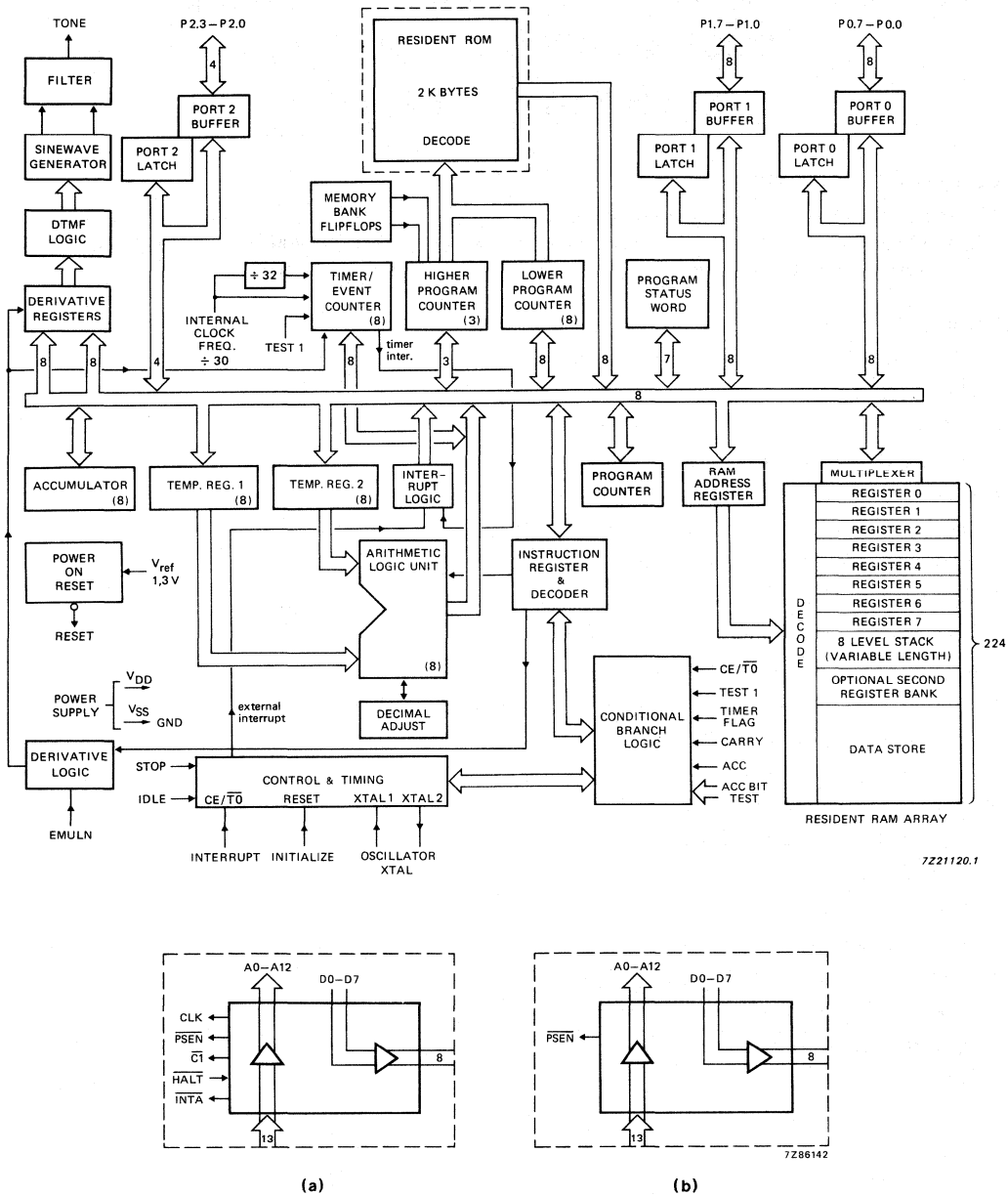


Fig. 1 PCD3344 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCF84C00 bond-out version or as shown in (b) for the PCF84C00 'piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

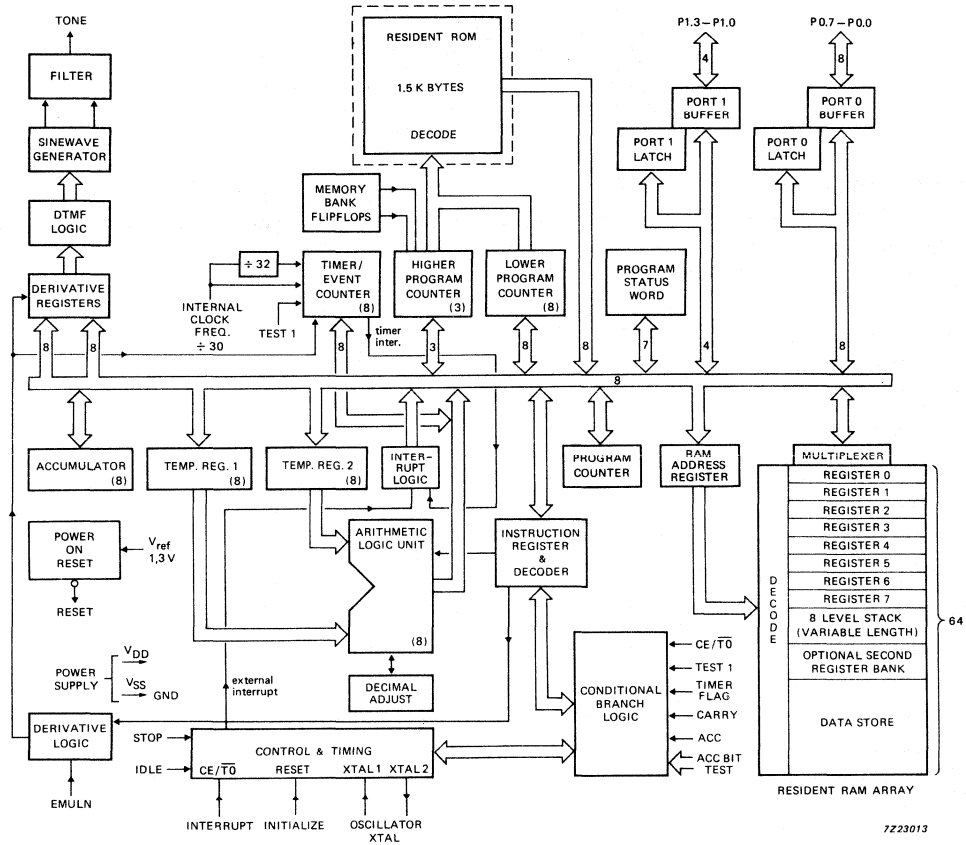
The PCD3347 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3344 family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1536 ROM bytes
- 64 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 12 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, PCD3343 and PCD84C00)
- All instructions 1 or 2 cycles
- Clock frequency 3,58 MHz
- Single supply voltage from 2,5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3347P: 20-lead DIL; plastic (SOT146).
PCD3347T: 20-lead mini-pack; plastic (SO20; SOT163A).



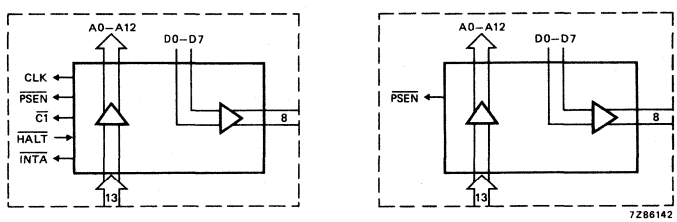


Fig. 1 PCD3347 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCF3300 bond-out version or as shown in (b) for the PCF3300 'piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

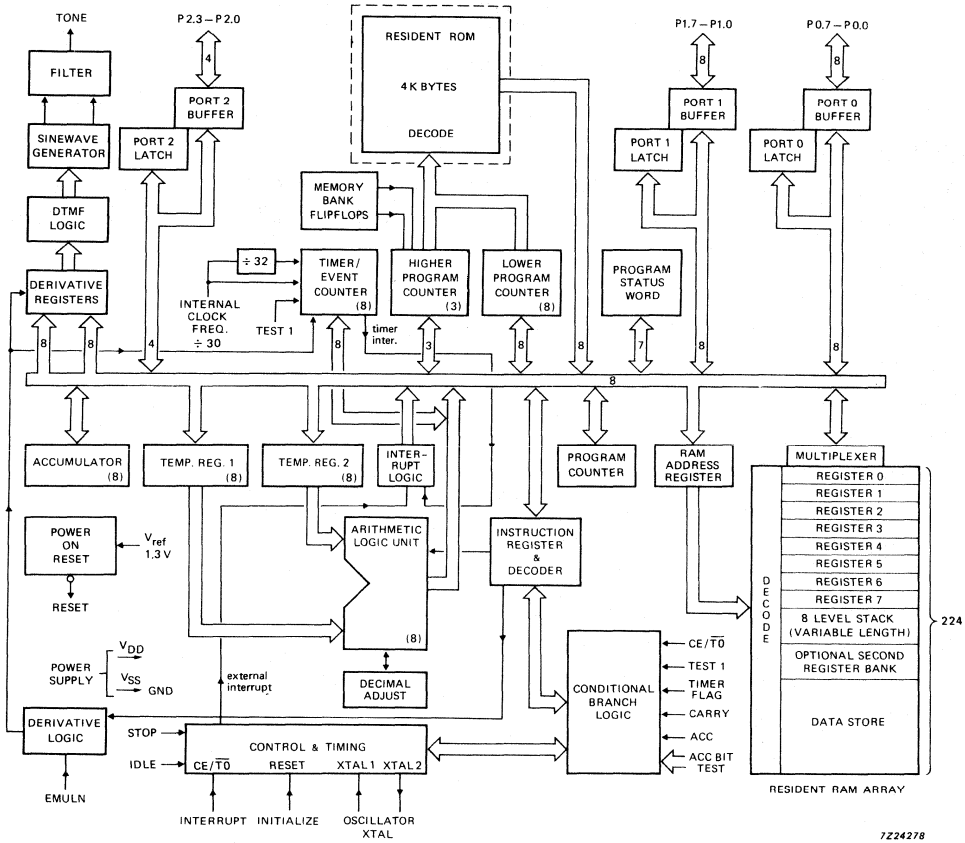
The PCD3349 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3343 family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets.

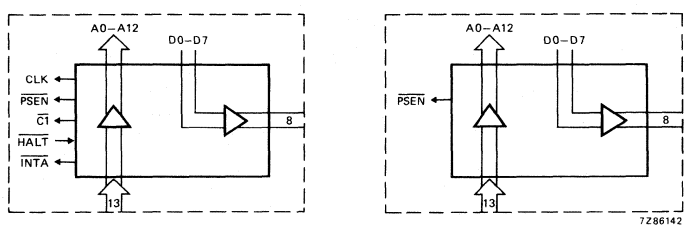
Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 4096 ROM bytes
- 224 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, PCD3343 and PCD84C00)
- All instructions 1 or 2 cycles
- Clock frequency 3.58 MHz
- Single supply voltage from 2.5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3349P: 28-lead DIL; plastic (SOT117).
PCD3349T: 28-lead mini-pack; plastic (SO28; SOT136A).





(a) (b)

Fig. 1 PCD3349 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCF84C00 bond-out version or as shown in (b) for the PCF84C00 'piggy-back' version.

PROGRAMMABLE MULTI-TONE TELEPHONE RINGER

GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333 Hz
Number of intervals per tone sequence		15 or 16
Lower limits of frequency discriminator		13,33 or 20 Hz
Upper limits of frequency discriminator		30 or 60 Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5 kΩ
Switch-on delay at 25 Hz	max.	60 ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT38).
PCD3360T: 16-lead mini-pack; plastic (SO16L; SOT162A).

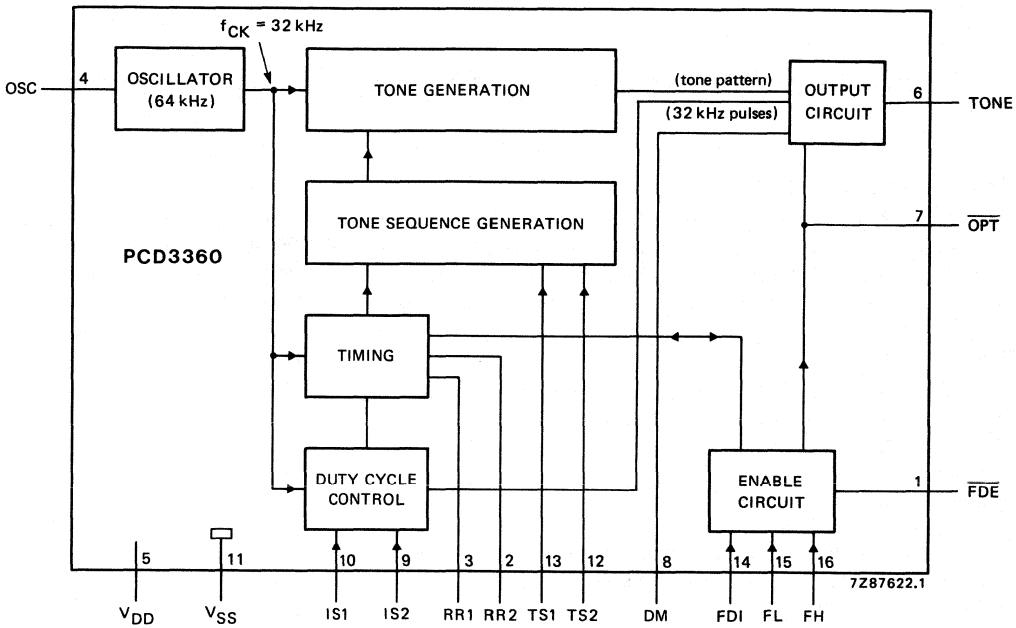


Fig. 1 Block diagram.

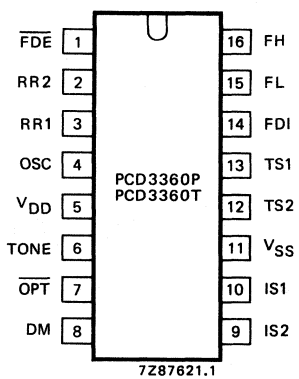


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{FDE}$	frequency discriminator enable
2	RR2	repetition rate selection
3	RR1	repetition rate selection
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	impedance setting and automatic swell
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	tone sequence selection
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

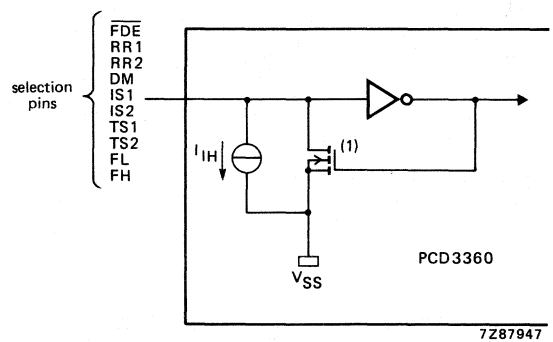
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 3). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 3 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

FUNCTIONAL DESCRIPTION (continued)

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 8) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 4.

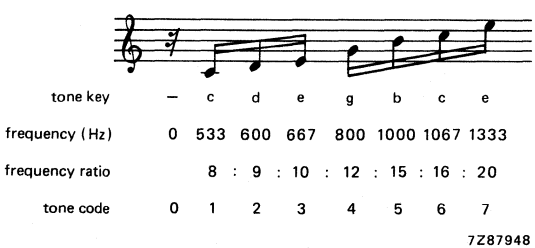


Fig. 4 Available tones and their corresponding internal ROM tone code.

Four tone sequences are programmed in the internal ROM (see Fig. 5). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 5.

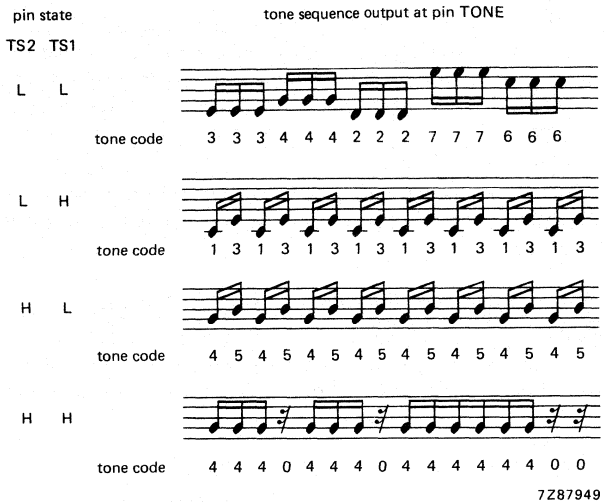


Fig. 5 Tone sequences mask-programmed in the PCD3360.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval
RR1	RR2	ms
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

FUNCTIONAL DESCRIPTION (continued)

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 6.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 8), the input impedance Z_I and and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
			1	1,9	–	40	tbf	tbf
L	L	automatic	2	2,9	–	20	17,5	–4
		swell	> 2	4,1	1,8	5	7	0
L	H		–	2,9	–	20	17,5	–4
H	L	constant	–	3,8	–	10	10,5	tbf
H	H	level	–	5,4	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} at 25 Hz in Fig. 8.

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:—

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

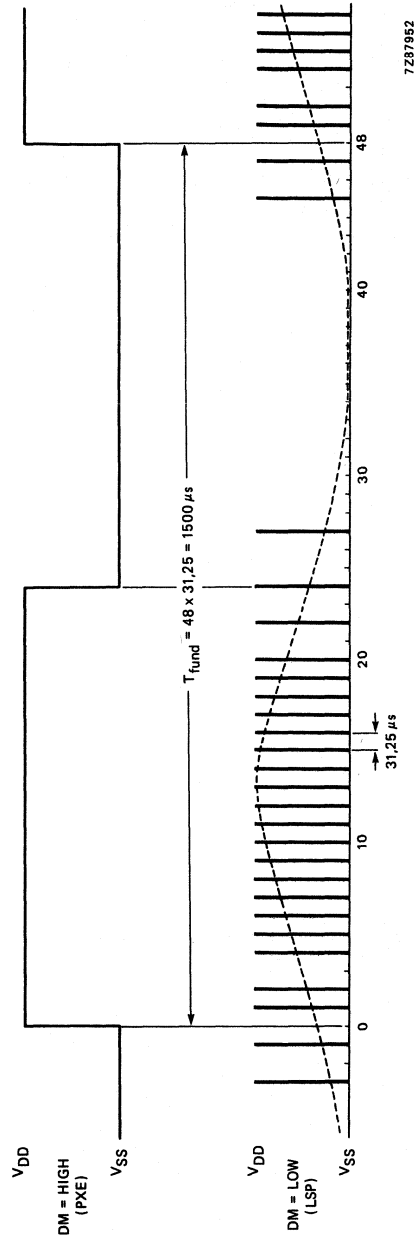


Fig. 6 Fundamental signal (667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

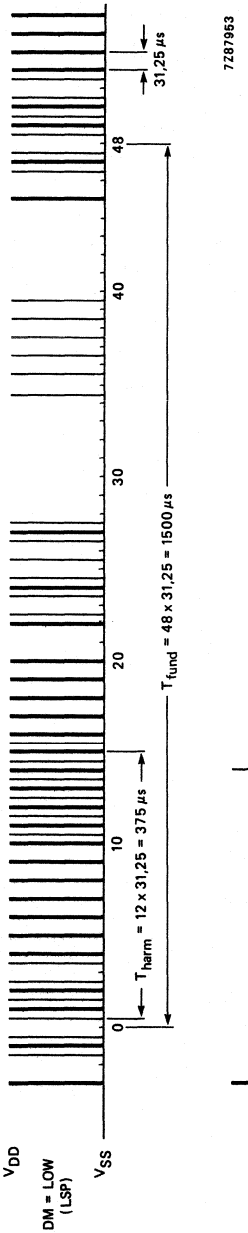


Fig. 7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	3,9	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current (note 3)	I_{DD}	–	110	140	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 4)	I_{SB}	–	3	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs					
FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}; T_{amb} = 25 °C	I_{SL}	14	23	32	μA
temperature coefficient of I_{SL}	$-\Delta I_{SL}$	–	0,5	–	%/°C
pull-down current with V_{FDI} = 0,8V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 5)	$\pm I_{IS}$	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at V_{OH} = V_{DD}−0,5 V	$-I_{OH}$	1	2	–	mA

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 6
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	50	ms
at FL = HIGH	$t_{d(off)}$	–	–	75	ms
Oscillator frequency at R_{osc} = 365 kΩ; C_{osc} = 56 pF; T_{amb} = 25 °C (note 7)	f_{osc}	60	64	68	kHz
Frequency variation					
as a function of V_{DD}	$-\Delta f_{osc}$	–	1	–	%/V
as a function of T_{amb}	$-\Delta f_{osc}$	–	0,05	–	%/K

DEVELOPMENT DATA

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{osc} = 365 kΩ; C_{osc} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open circuit.
4. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
6. The switch-on delay is measured in cycles of incoming ringing frequency.
7. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 8.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI $<$ 3,4 V)
- The value of R2 (680 kΩ in Fig. 8)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17 \text{ V}.$$

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3,4 V.

The minimum operating voltage across C3 is 17,8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,8 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R3 (100 kΩ in Fig. 8)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 9. The only significant difference between Fig. 8 and Fig. 9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

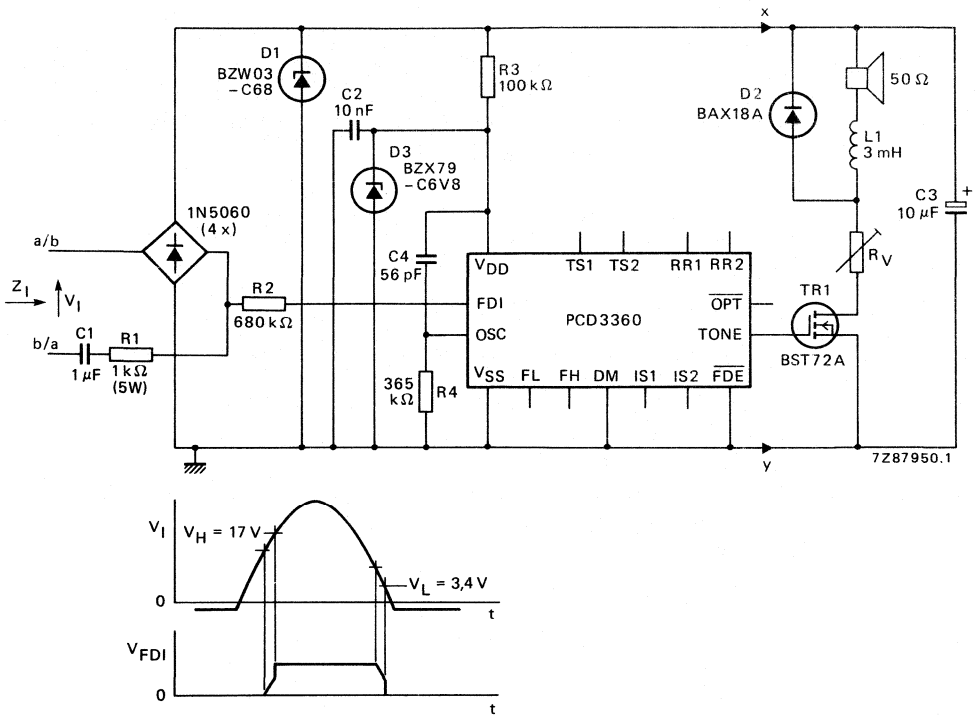


Fig. 8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

DEVELOPMENT DATA

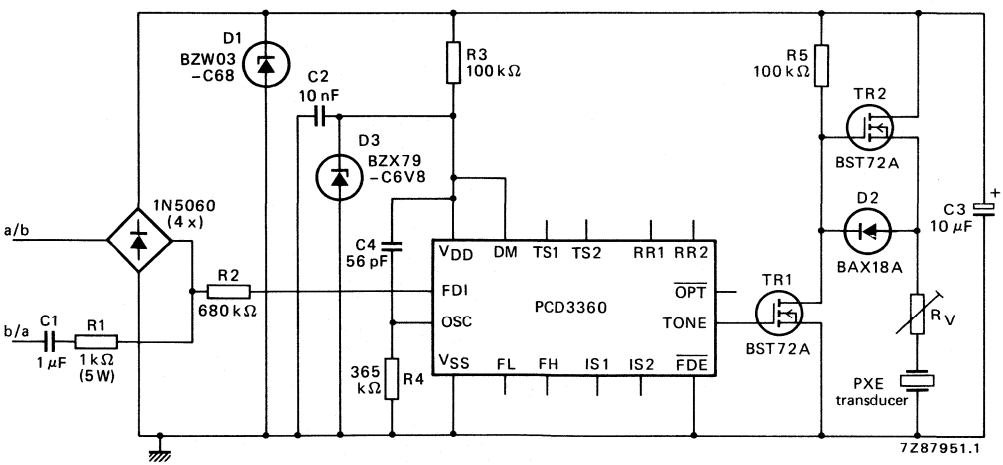


Fig. 9 PCD3360 ringer with PXE transducer.

PULSE AND DTMF DIALLER

GENERAL DESCRIPTION

The PCD4413 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit memory capacity
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Two function keys; * and FL (flash)
- DTMF timing:
  manual dialling — minimum duration for bursts and pauses
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

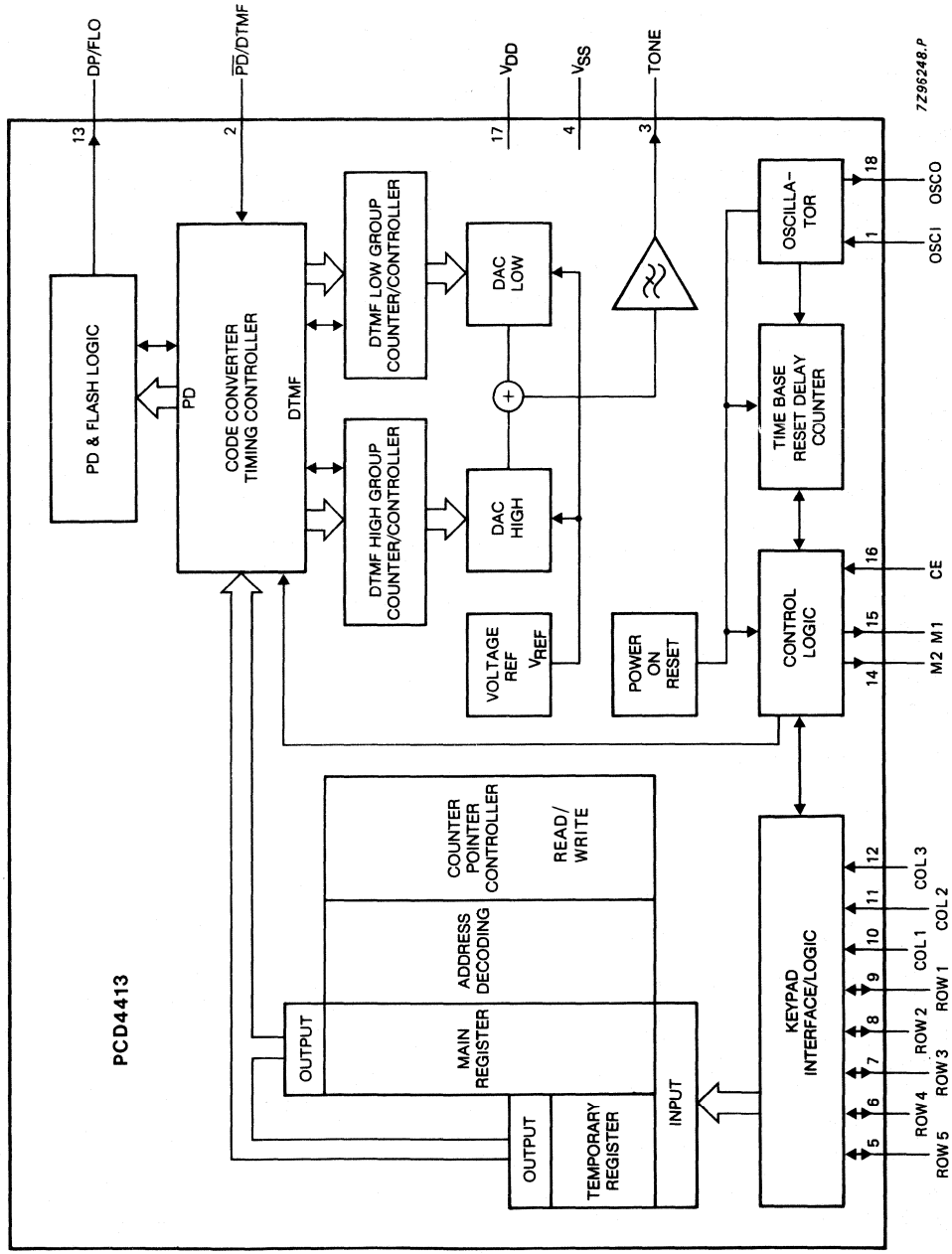


Fig. 1 Block diagram.

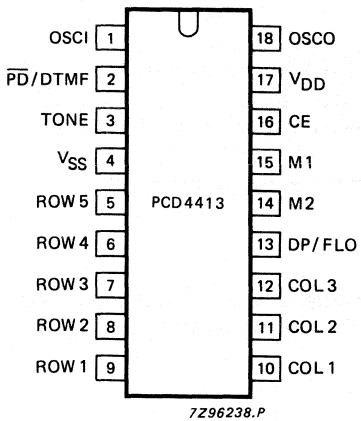


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	M2	strobe; active HIGH during transmission
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.

The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4413 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, the keyboard input is inhibited and all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 4).
The current drawn is I_{DDO} (standby current) during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 7, Fig. 8 and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

PD/Data transmission mode

If PD/DTMF = V_{SS} the pulse-data mode is selected. Starting with numeric keys digits will be dialled out in pulse dialling mode, until key * is depressed which selects the data transmission mode (the * tone is not transmitted). All keys (including * and #) will now be transmitted in DTMF tones.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4413 are directly connected to the keyboard as shown in Fig. 3.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 7, 8 and 9. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

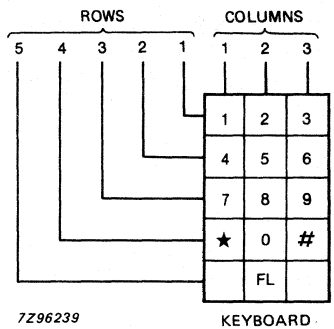


Fig. 3 Keyboard organization.

Row 5 of the keyboard contains the special function key FL — flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of 100 ms at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated at 100 ms.

The flash pulse resets the read address counter (RAC).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output stays HIGH for the period of the transmit and pause time. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4413 it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DEVELOPMENT DATA

DIALLING PROCEDURES (see also Figs 5 and 6)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 4). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the main register after validation. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Figs 7, 8 and 9. Each entry is tested for validity before being deposited in the main register.

In pulse dialling mode only the 0 to 9 keys result in dialling operations.

* is a special function key:

** key*

- Used to switch from dialling mode to data transmission mode. The * tones will not be transmitted.

In DTMF and data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1).

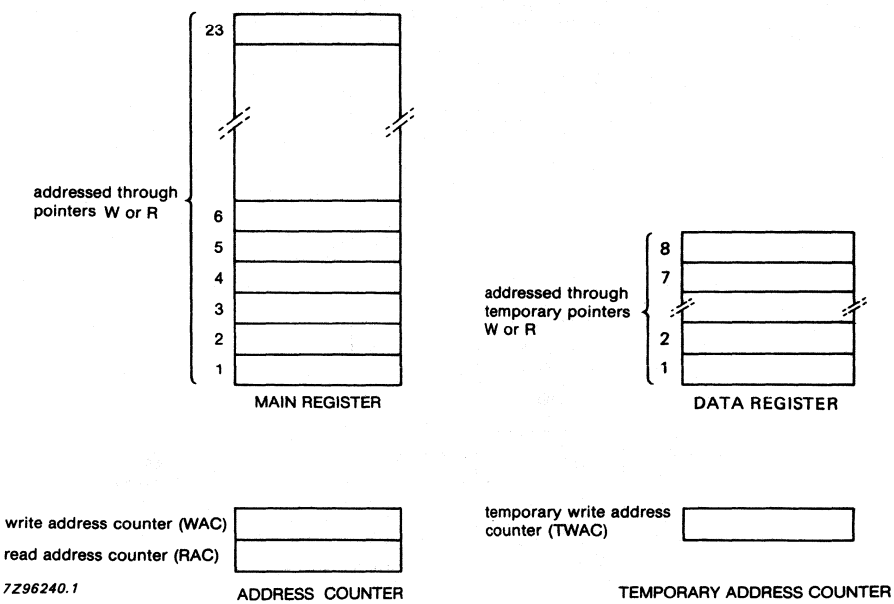


Fig. 4 Memory organization.

DIALLING PROCEDURES (continued)

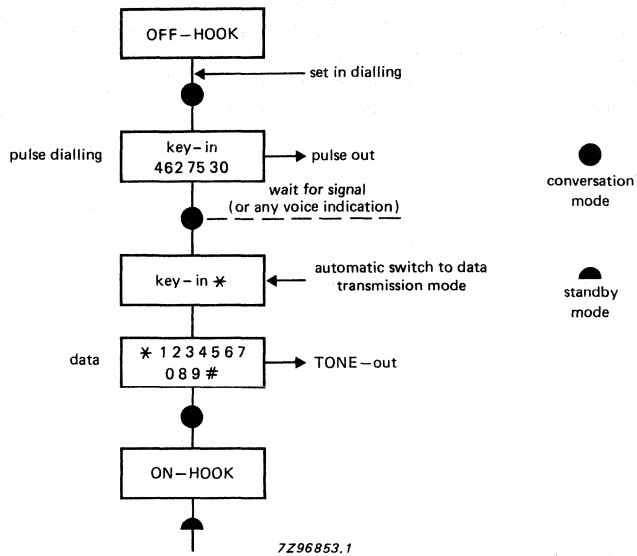


Fig. 5 Pulse and data transmission mode.

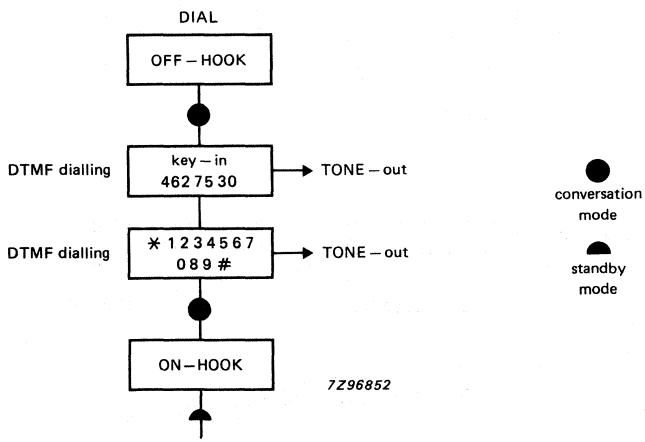


Fig. 6 DTMF mode.

DEVELOPMENT DATA

TIMING

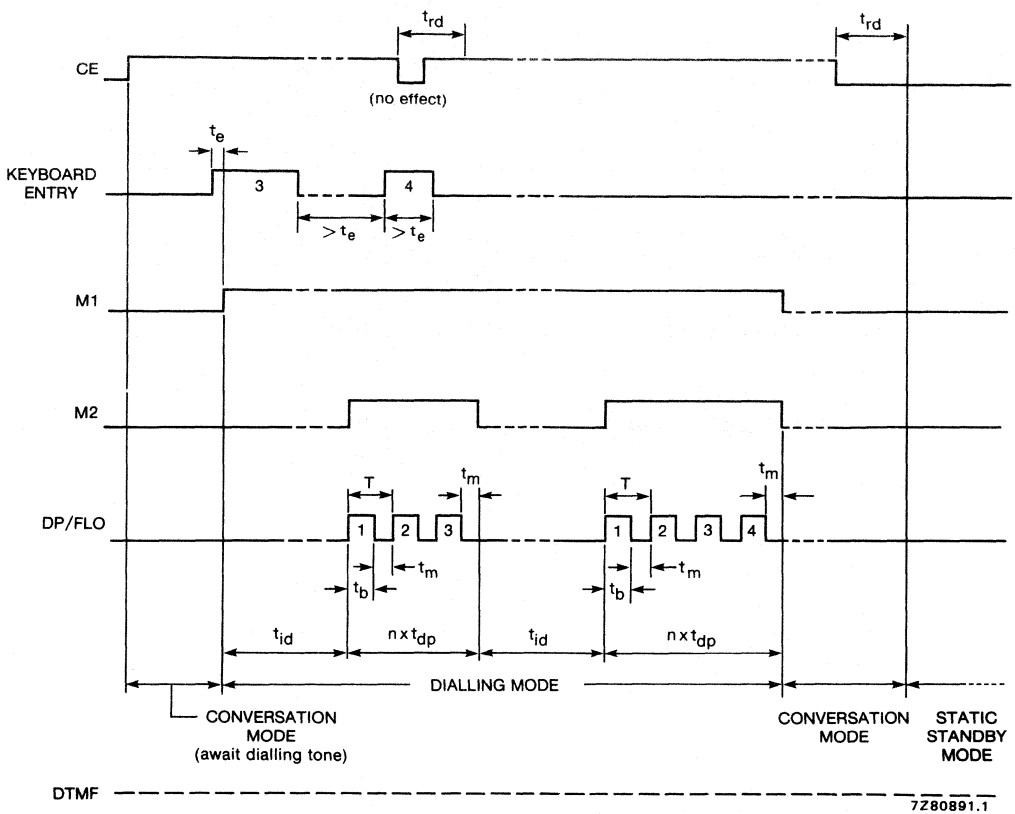


Fig. 7 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

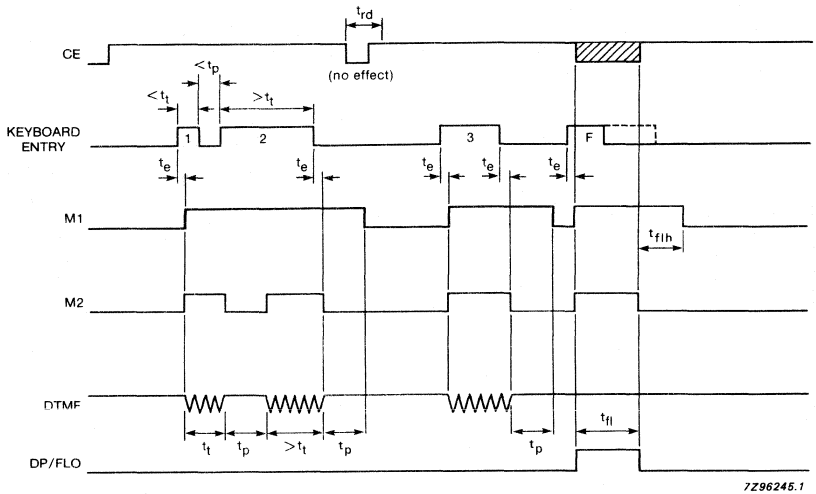


Fig. 8 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

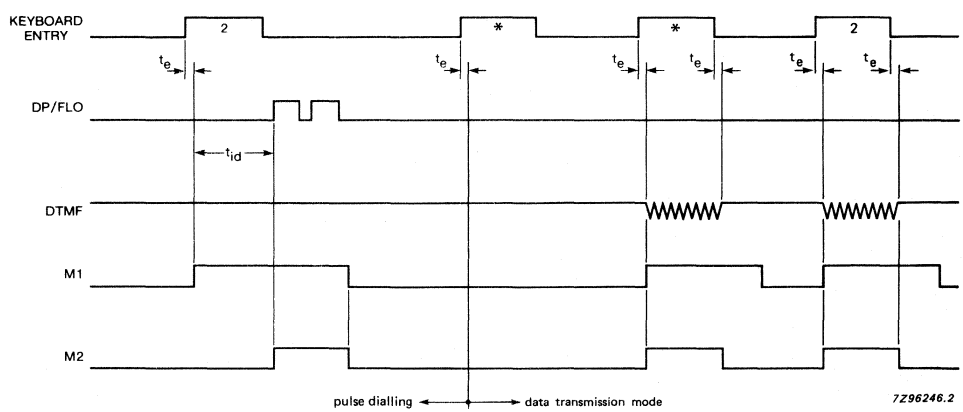


Fig. 9 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, M2, DP/FLO	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 10) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	$\frac{1}{2}V_{DD}$	−	V
Output impedance	$\lvert Z_O \rvert$	−	0,1	0,5	kΩ
Load resistance	R_L	10	−	−	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	−	−25	−	dB
Transmission and pause time					
Manual and data transmission dialling mode	t_t	65	−	−	ms
	t_p	65	−	−	ms
Flash pulse duration	t_{FL}	95	100	105	ms
Flash hold-over time	t_{flh}	30	32	34	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 3)	t_b	58	60	62	ms
Make time (note 3)	t_m	38	40	42	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Mark-to-space ratio 3 : 2.

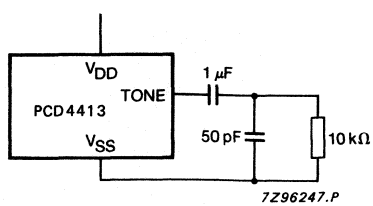
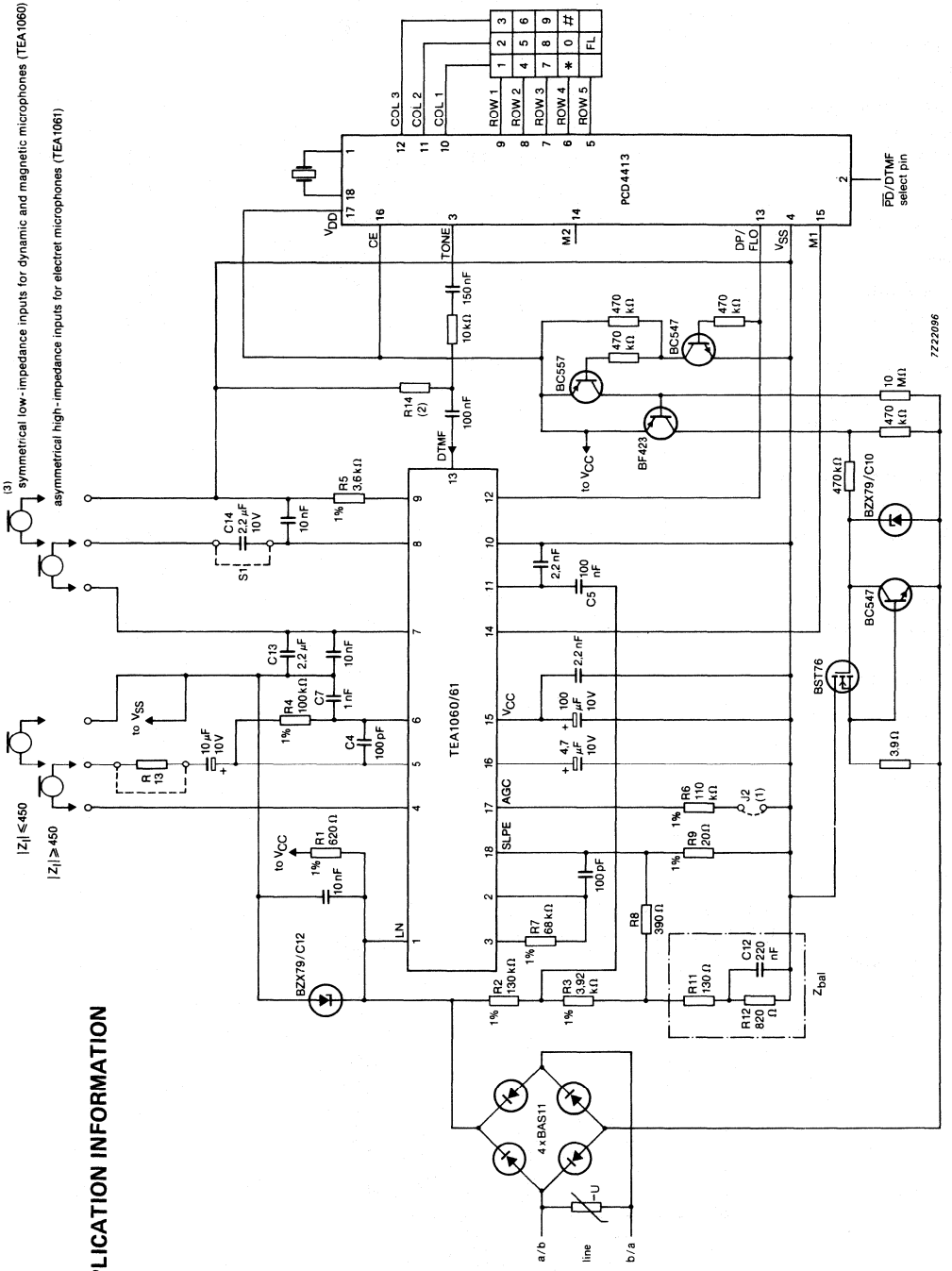


Fig. 10 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig. 11 Application diagram of the full electronic basic telephone set.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD4415 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Redial buffer for PABX and public calls
- Three function keys; * or >, # or R/AP and FL (flash)
- DTMF timing:
  - manual dialling — minimum duration for bursts and pauses
  - redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD4415P: 18-lead DIL; plastic (SOT102).
PCD4415T: 20-lead mini-pack; plastic (SO20; SOT163A).

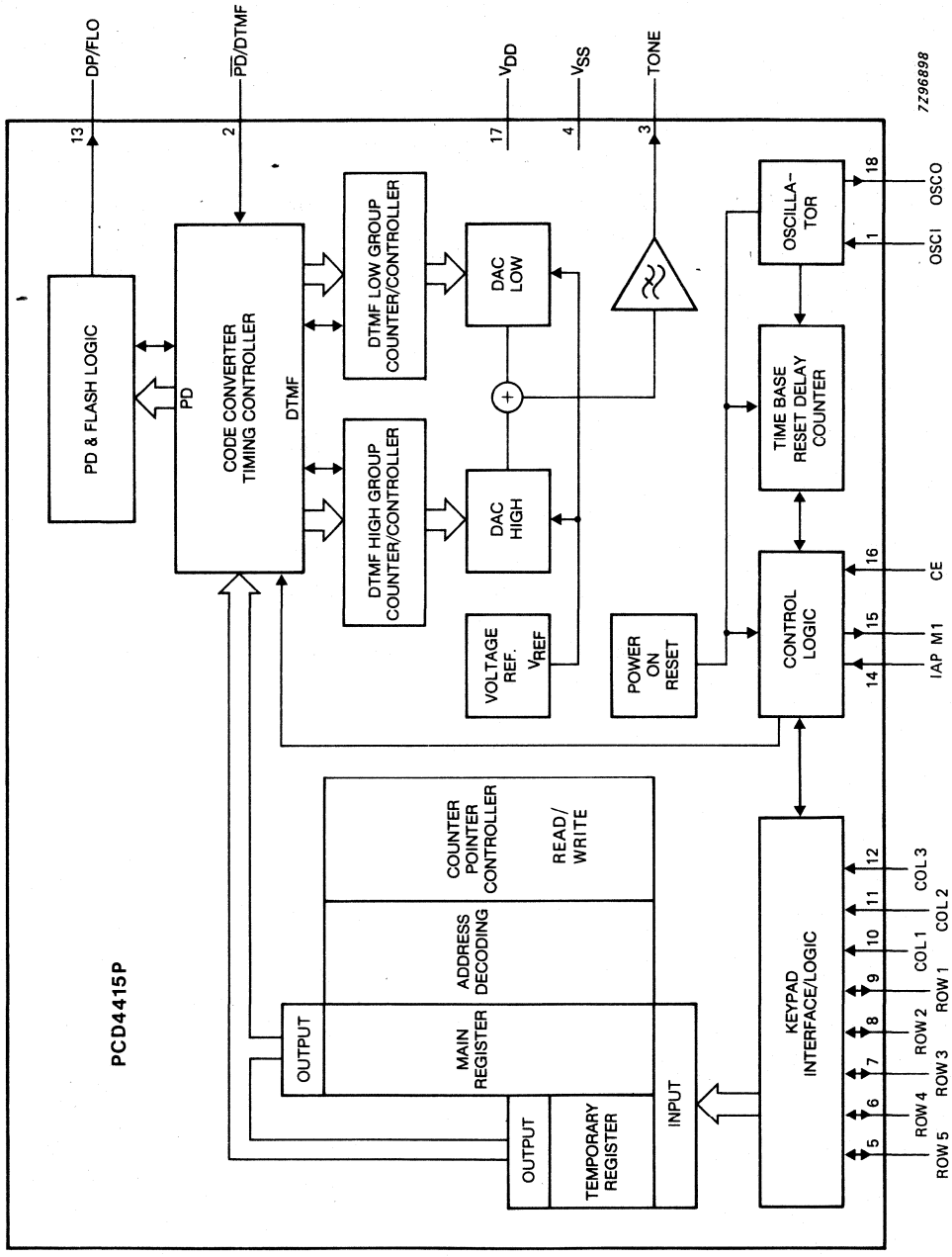


Fig. 1 Block diagram; PCD4415P.

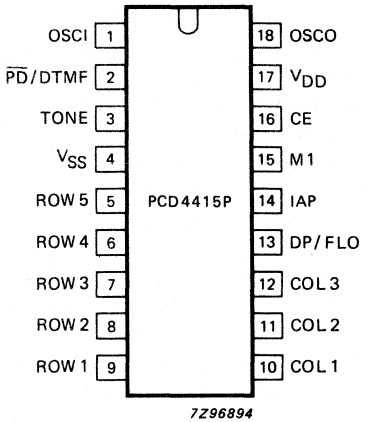


Fig. 2 Pinning diagram; PCD4415P.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	IAP	input access pause
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

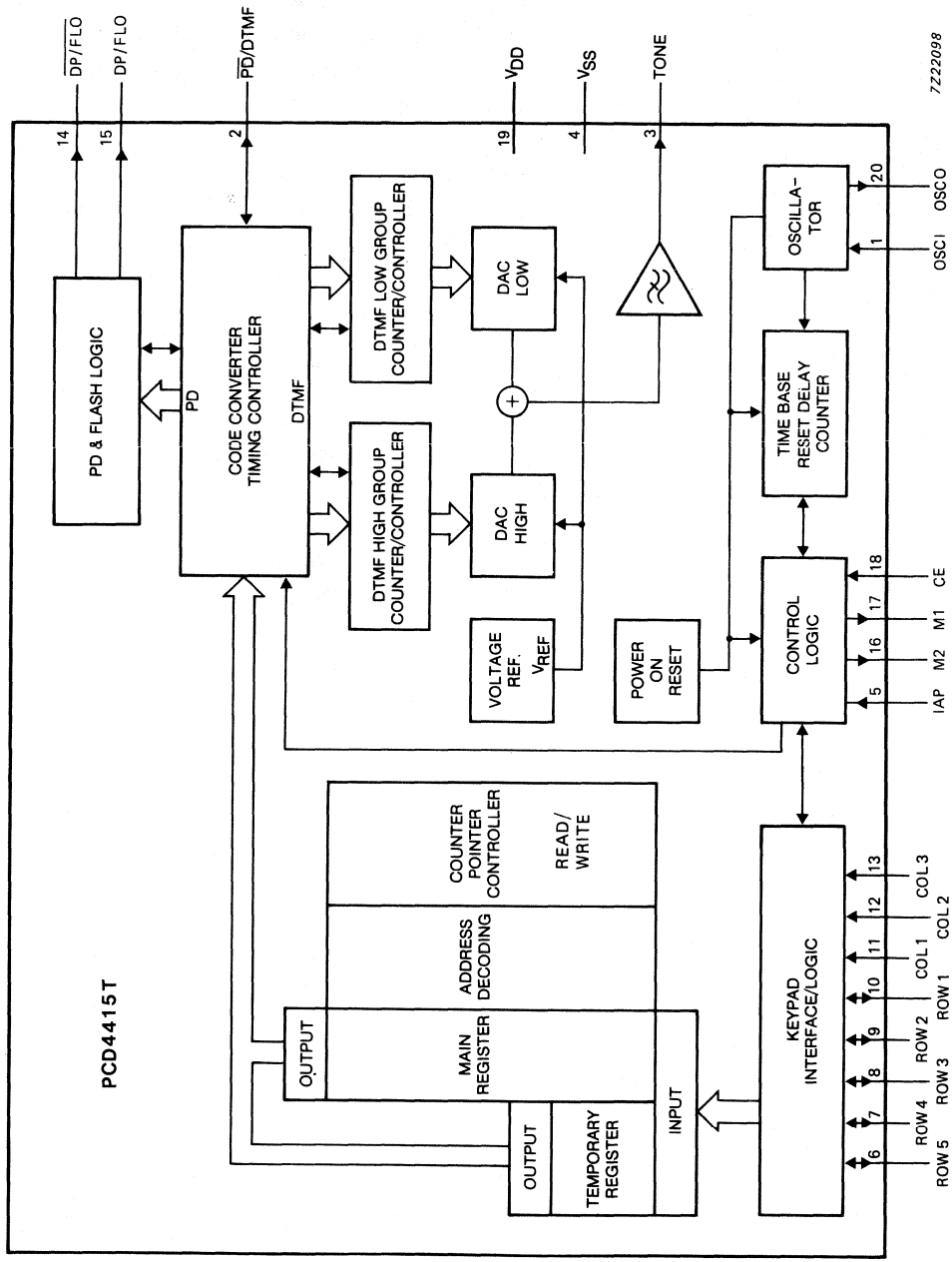


Fig. 3 Block diagram; PCD4415T.

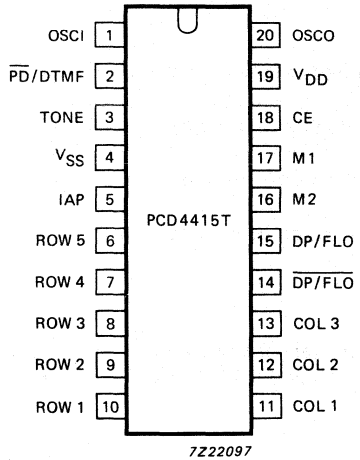


Fig. 4 Pinning diagram; PCD4415T.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	IAP	input access pause
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	$\overline{DP}$/FLO	inverted dialling pulse and flash output
15	DP/FLO	dialling pulse and flash output
16	M2	strobe; active HIGH during transmission
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4415 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 6). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 10a, Fig. 10b and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse dialling mode is selected.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each numeric push-button activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Data transmission mode

Data transmission mode is entered from the dialling mode (PD or DTMF) on first depression of key*, or key >. The "*" tones are not transmitted.
In the data transmission mode no digits are stored for later redial, "*" and "#" are purely DTMF keys, so are no longer special functions. The digits are temporarily stored in a special register, which has a maximum capacity of eight digits.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4415 are directly connected to the keyboard as shown in Fig. 5.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 10. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

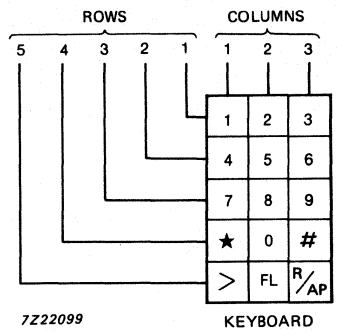


Fig. 5 Keyboard organization.

Keys* and # represent the DTMF tones and also special dialling functions. In ROW 5 the keys > and R/AP only are function keys, while key FL offers flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of 100 ms at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated at 100 ms.

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Dial pulse and flash output ($\overline{DP/FLO}$)

Inverted output of DP/FLO. In the PCD4415 it is only available as a bonding option of DP/FLO.

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes HIGH for the period of the tone transmission and pause times. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4415 it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling. Only available as a bonding option of IAP.

Input access pause (IAP)

This input can be used instead of the # (R/AP) key for programming access pause(s) in RAM when dialling and terminating access pause(s) during redial.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DIALLING PROCEDURES (see also Figs 7, 8 and 9)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 6). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. If more than 23 digits are entered redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 10. Each entry is tested for validity before being deposited in the redial register.

In manual dialling mode (pulses and DTMF) only the 0 to 9 keys result in dialling operations.

"#" and "*" are special function keys:

 # key or R/AP key

- If the first key after CE or Flash means: Redial (see redial procedure)
- If not the first key, then it is used to program access pause(s) in the RAM for later redial. If it is the last key it will be omitted before going "on-hook".

** key or > key*

- Used to switch from dialling mode (pulse or DTMF) to data transmission mode. The * tones will not be transmitted even if the previous mode was DTMF dialling.

In data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1), keys > and R/AP will be ignored.

DEVELOPMENT DATA

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4415 is in conversation mode.
If "#"or "R/AP" is the first keyboard entry the circuit starts redialling the contents of the register, Timing in the DTMF mode is calibrated for both tone bursts and pauses.
Only the first part entered (the pulse or DTMF dialled part of the stored number) can be redialled.
During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling. The # and R/AP keys are active only during access pauses.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory overflow (more than 23 valid data entries)

If an access pause is detected during redial, the circuit is switched back to the conversation mode and stays there until the # or R/AP key is depressed. Therefore when the # or R/AP key is depressed the access pause is ended. After termination of the access pause the circuit continues dialling the rest of the telephone number.

In addition to the manual use of the # or R/AP key for programming and terminating access pause(s), the input input IAP can be used. If during manual dialling and conversation mode IAP becomes HIGH, an access pause will be stored in the memory.
If after "on-hook" or "flash" the last stored digit is an access pause then it will be deleted out of the memory.
When during redialling an access pause occurs and IAP becomes HIGH, then the access pause will be automatically terminated and redialling continues.

As soon as the conversation mode is entered depressing the * or > key will again switch the circuit to the data transmission mode.

Redial takes place in the main register (max. 23 digits). After redial when a numeric key is pressed (first digit of an extension number) the redial number will be cleared. Thus the total capacity of the main register is available for extension number dialling. This extension number is stored in the main register

DIALLING PROCEDURES (continued)

(max. 23 digits) and is available later after "on-hook", "off-hook".

The main register will also store digits that have been keyed-in at a rate faster than dialled out.

Access pause

- The number of access pauses is unlimited.
- Consecutive pauses will be stored as a single pause.

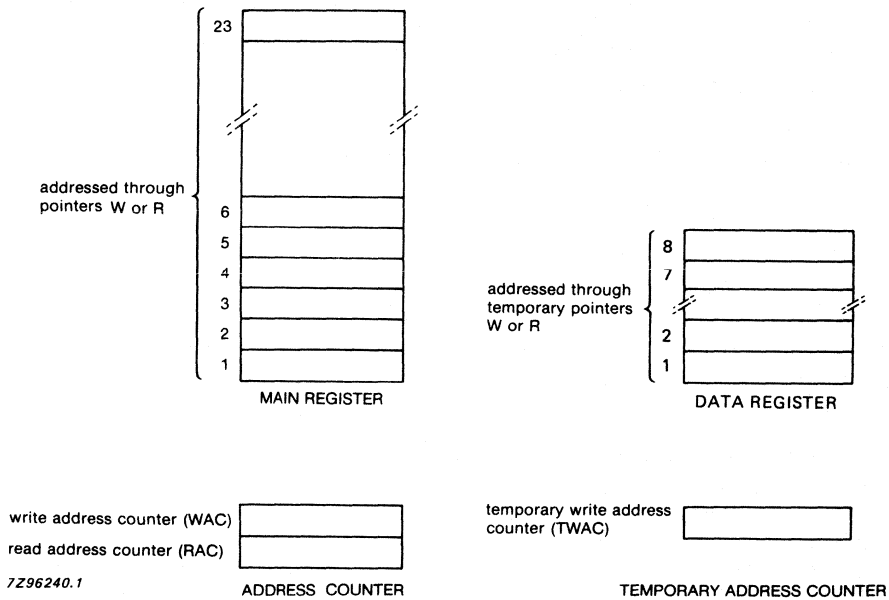


Fig. 6 Memory organization.

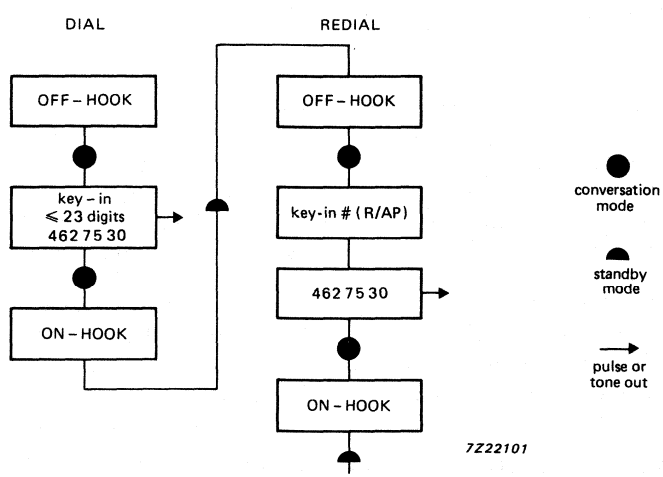


Fig. 7 Pulse/DTMF dialling mode.

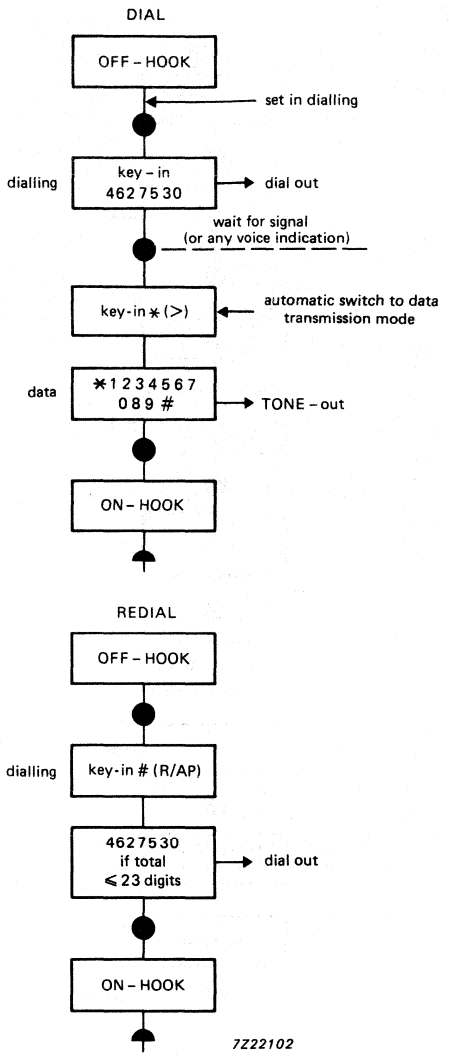


Fig. 8 Pulse/DTMF dialling and data transmission mode.

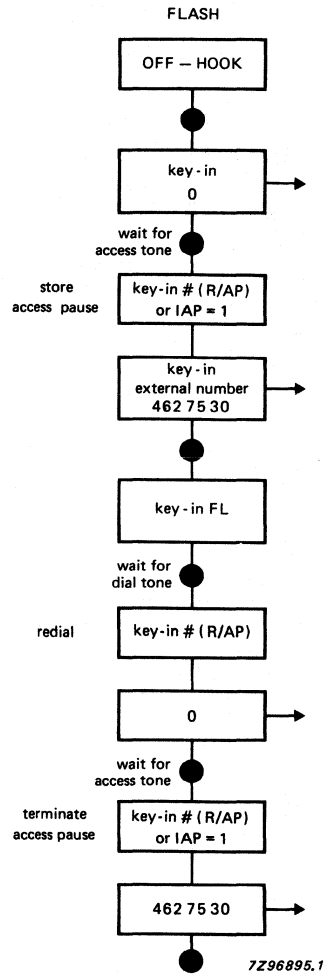


Fig. 9 Flash; independent of dialling mode.

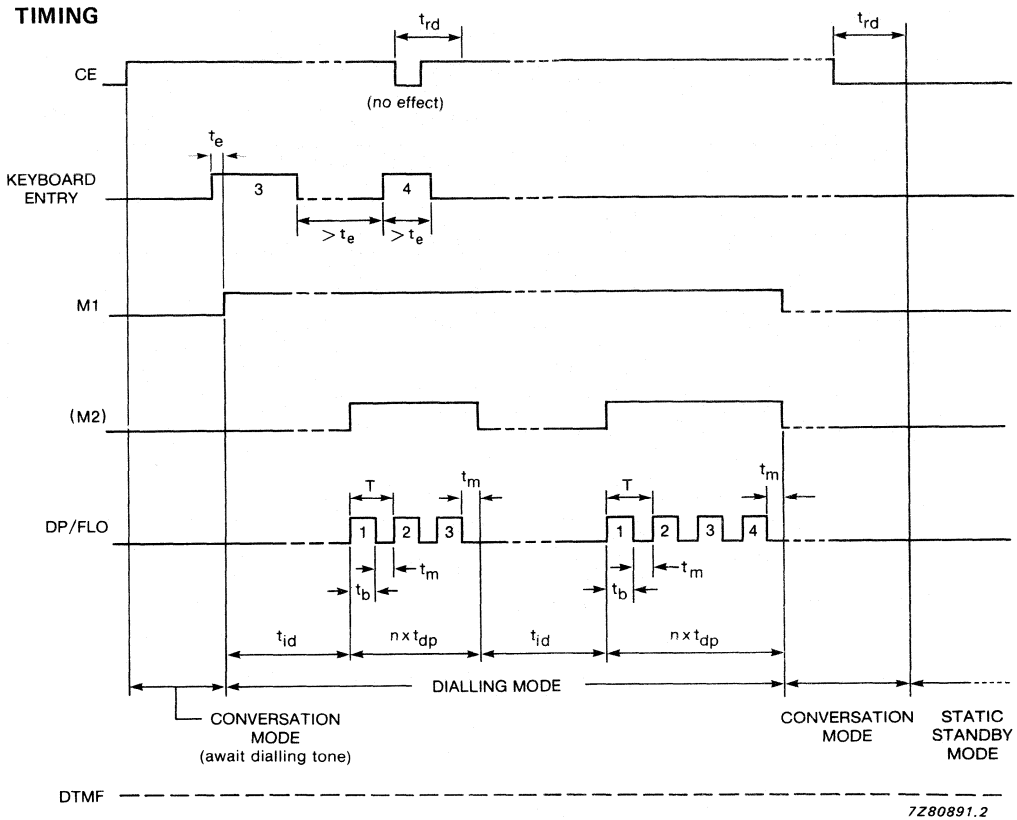


Fig. 10a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

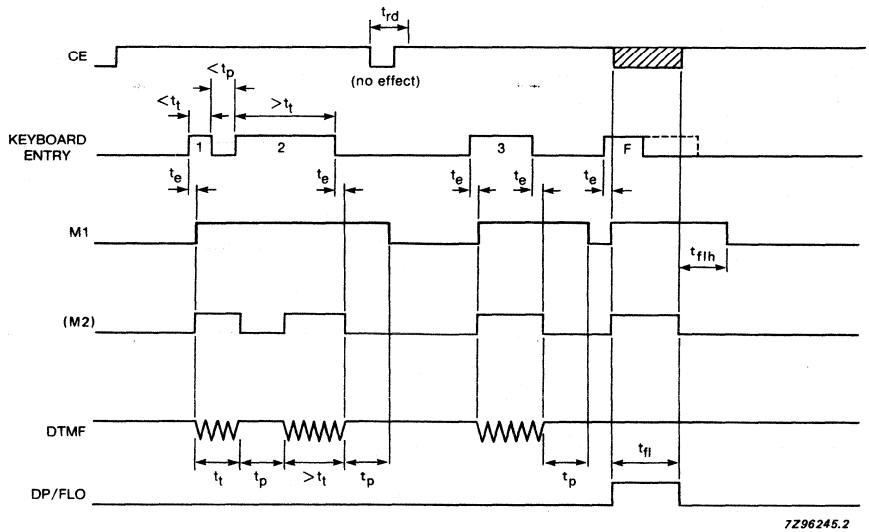


Fig. 10b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

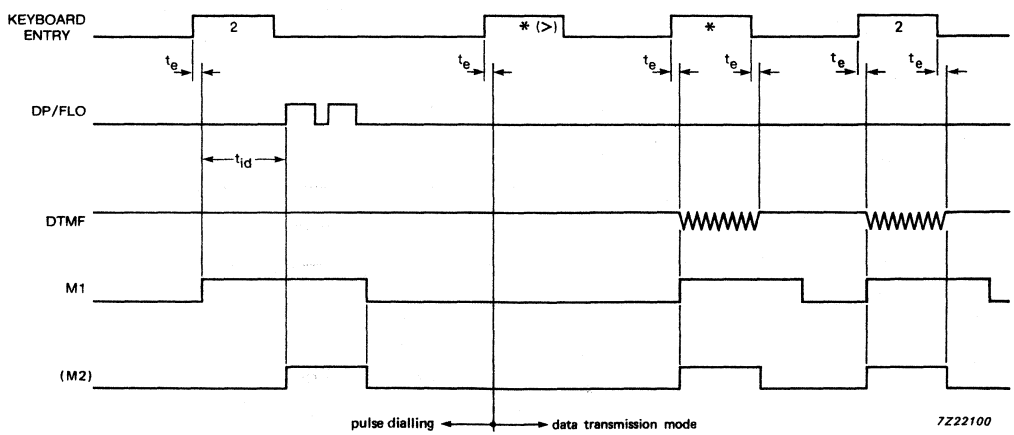


Fig. 10c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

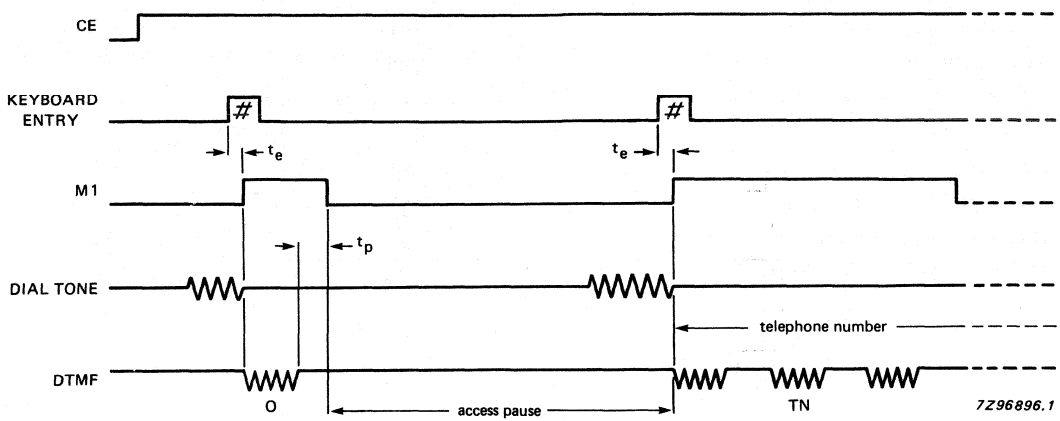


Fig. 11a Timing diagram showing REDIAL where PABX access digit(s) are the first keyboard entries and access pause is terminated by the # or R/AP key; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

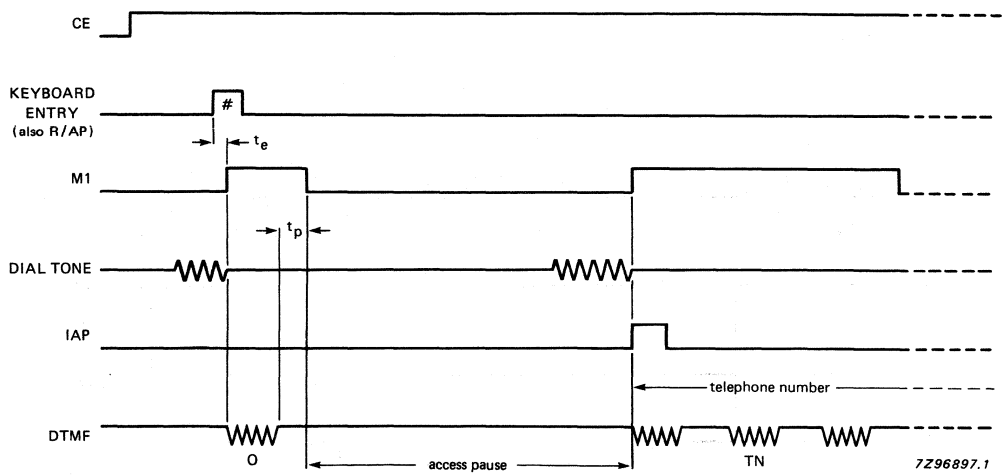


Fig. 11b Timing diagram showing REDIAL where PABX access digit(s) occur and are terminated by IAP; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V M1, M2, DP/FLO, $\overline{DP/FLO}$	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 12) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	$\frac{1}{2}V_{DD}$	−	V
Output impedance	$\lvert Z_O \rvert$	−	0,1	0,5	kΩ
Load resistance	R_L	10	−	−	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	−	−25	−	dB
Transmission and pause time (note 3)					
Manual and data transmission dialling mode	t_t	65	−	−	ms
	t_p	65	−	−	ms
Redialling	t_t	65	70	75	ms
	t_p	65	70	75	ms
Flash pulse duration	t_{FL}	95	100	105	ms
Flash hold-over time	t_{flh}	32	34	36	ms
Pulse dialling (PD) (note 3)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 4)	t_b	64	66	68	ms
Make time (note 4)	t_m	32	34	36	ms

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Other timing is possible on request.
4. Mark-to-space ratio 2:1.

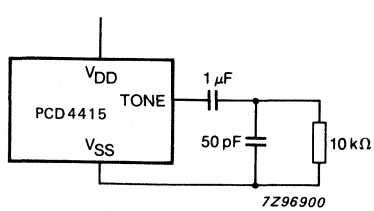
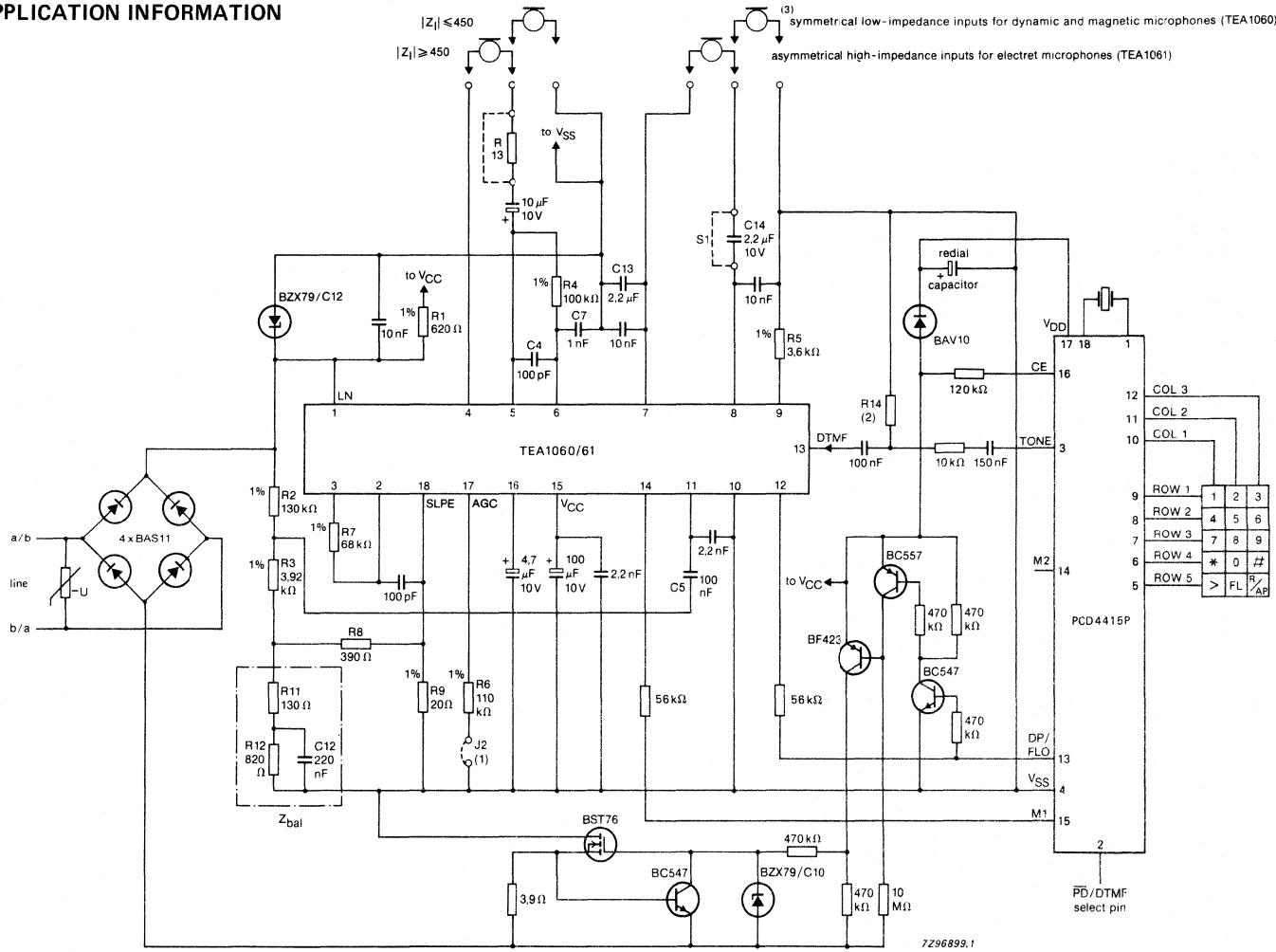


Fig. 12 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig. 10 Application diagram of the full electronic basic telephone set.

MICROPOWER DC VOLTAGE DETECTOR

GENERAL DESCRIPTION

The PCF1251 is a CMOS micropower DC voltage detector and it is especially designed for power-on/off voltage detection monitoring and reset. The IC has an extremely low current consumption and is therefore particularly suited for battery operated applications. The internal bandgap reference voltage is stable with temperature variations. The voltage trip-point and the hysteresis can be set independently with external resistors. Two of the four outputs can be delayed with an external capacitor.

Features

- Extremely low current consumption
- Built-in bandgap voltage reference
- Wide range of voltage trip-points
- Two pairs of outputs; one pair with delay possibility
- 8-lead DIL or SO8 mini-pack (plastic packages).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	1	–	6	V
Supply current	I_{DD}	–	1	–	μA
Output currents at V_{DD} = 1 V	I_O	–	2	–	mA
Bandgap voltage reference at 25 °C	V_{REF}	1,05	1,15	1,25	V

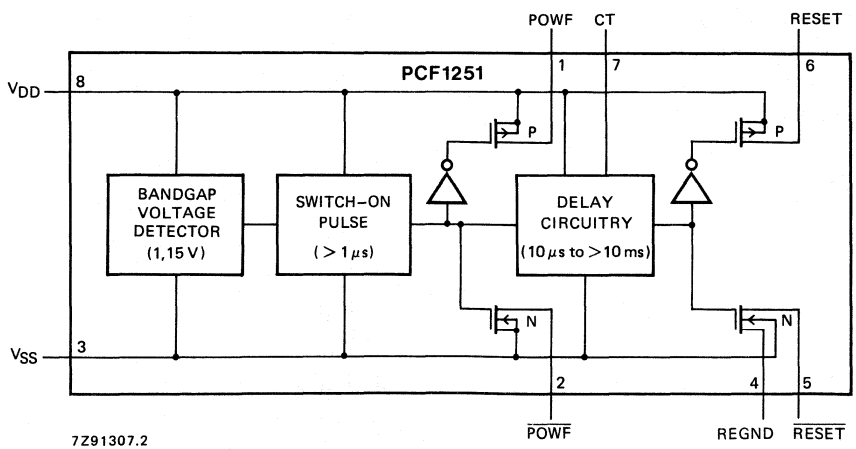


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF1251P: 8-lead DIL; plastic (SOT97).
PCF1251T: 8-lead mini-pack; plastic (SO8; SOT96A).

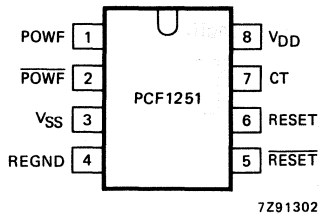


Fig. 2 Pinning diagram.

PINNING

1	POWF	power-fail output
2	$\overline{\text{POWF}}$	power-fail output (inverted)
3	V_{SS}	negative supply voltage
4	REGND	reset ground
5	$\overline{\text{RESET}}$	reset output (inverted; delayed)
6	RESET	reset output (delayed)
7	CT	capacitor for additional delay
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

The PCF1251 consists of a bandgap voltage reference, a comparator and delay circuitry (see Fig. 1). The supply voltage of the circuit (V_{DD} with respect to V_{SS}) is compared with an internal bandgap voltage reference by means of a special comparator. This comparator is connected to the circuit supply voltage. As long as the supply voltage is above the reference voltage level, the four open-drain outputs are all switched off and an extended drain-source voltage of up to 6 V is allowed. When the supply voltage is reduced and reaches the reference voltage level (V_{REF}), the power-fail outputs are switched on (p-channel for POWF and n-channel for $\overline{\text{POWF}}$ outputs). After a delay, determined by an external capacitor between pins CT and V_{DD}, the outputs RESET and $\overline{\text{RESET}}$ are switched on. The same delay will be active when the supply voltage is increased again and exceeds the internal voltage reference, resulting in switching off the outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage with respect to V_{SS}	V_{DD}	–	8	V
Output voltage at pin 2 V_{DD} with respect to V_2	V_2	–	8	V
Output voltage at pin 5 (pin 4 at V_{SS}) V_{DD} with respect to V_5	V_5	–	8	V
Output voltage at pin 1 V_1 with respect to V_{SS}	V_1	–	8	V
Output voltage at pin 6 V_6 with respect to V_{SS}	V_6	–	8	V
Voltage at pin 7 (CT)	V_7	−0,5	V_{DD} + 0,5	V
Current at pin 7 (CT)	I_7	–	20	mA
Output currents at pins 1, 2, 5 and 6	$\|I_O\|$	–	25	mA
Total power dissipation	P_{tot}	–	150	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	1	–	6	V
Operating supply current V_{DD} = 6 V; all outputs open	I_{DD}	–	1	3	μA
Bandgap voltage reference; T_{amb} = 25 °C	V_{REF}	1,05	1,15	1,25	V
V_{REF} temperature coefficient	$\Delta V_{REF}/\Delta T$	–	−0,4	–	mV/K
Output current at pins 2 and 5 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; V_O = 0,4 V with respect to V_{SS}	I_O	1	2	–	mA
Output current at pins 1 and 6 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; $-V_O$ = 0,4 V with respect to V_{DD}	$-I_O$	1	2	–	mA

(1) For correct switching of the outputs the slew rate of the supply voltage should be less than 1 V/ms.

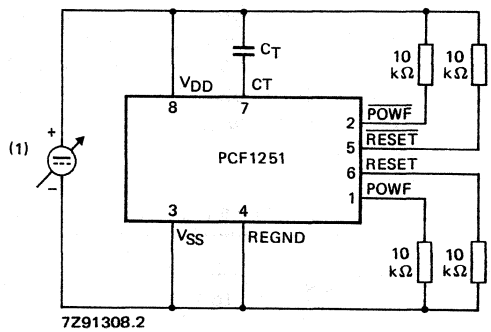


Fig. 3 Test circuit for timing measurements.

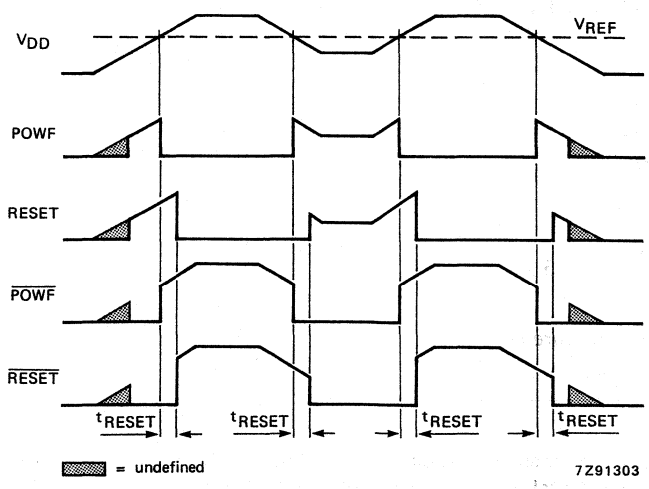


Fig. 4 Timing diagram for slow supply voltage changes.

(1) at $T_{amb} = 25\ ^{o}C$

a) $C_T < 0.1$ nF: $10\ \mu s < t_{RESET} < 750\ \mu s$

b) $C_T \geqslant 0.1$ nF: $t_{RESET} = \left[0{,}1 + 3{,}2\ ms \times C_T\left(\frac{nF}{nF}\right)\right]^{+75\%}_{-50\%}$

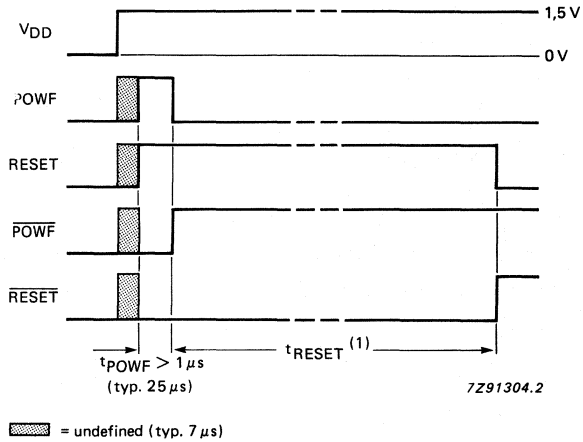


Fig. 5 Timing diagram for fast supply voltage switching on (non-repetitive).

APPLICATION INFORMATION

(1) The value of capacitor C is chosen to limit the slew rate of the supply voltage to less than 1 V/ms (e.g. the hysteresis voltage step on resistor R3).

(2) CT (pin 7) is a high-impedance connection for the capacitor C_T. This capacitor adds to the reset delay time provided by an internal current source (120 nA) and capacitor. Care must be taken to avoid external leakage current at this pin but the pin should not be left open circuit as stray capacitances to V_{SS} can then disturb the delay function.

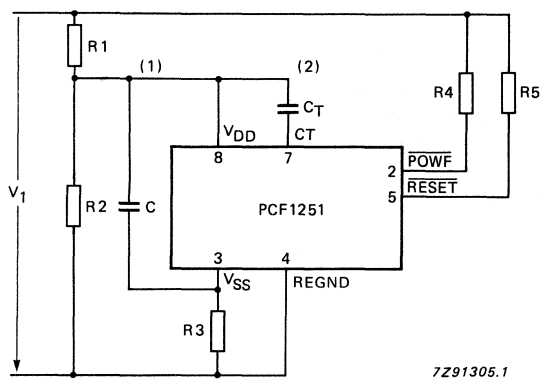
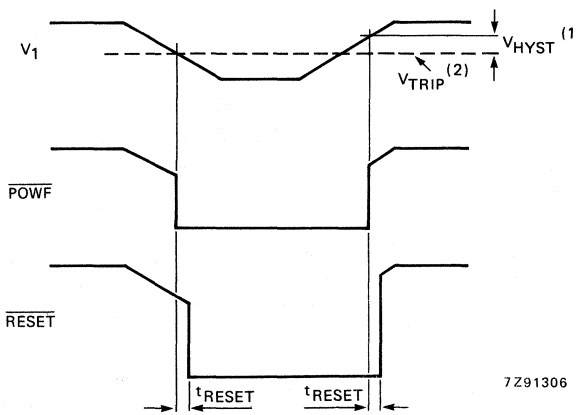


Fig. 6 Application circuit diagram.



(1) $V_{HYST} = V_{TRIP} \times \frac{R3}{R3 + R4}$; (0,2 V max.)

(2) $V_{TRIP} = V_{REF} \times \frac{R1 + R2}{R2}$

Fig. 7 Timing diagram for the circuit of Fig. 6.

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

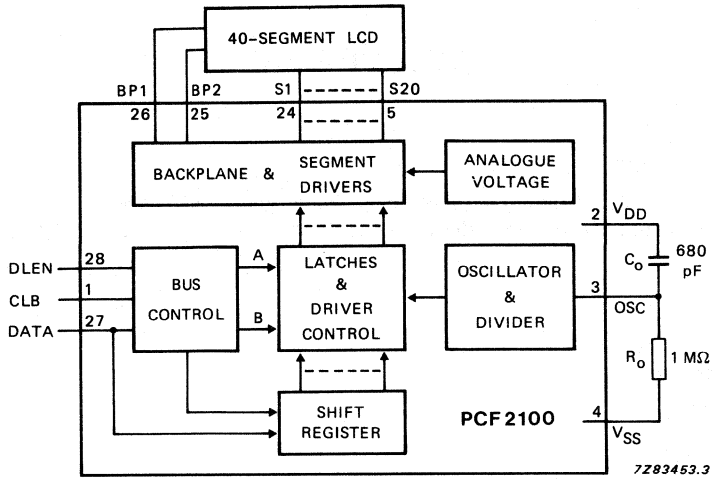


Fig. 1 Block diagram; PCF2100

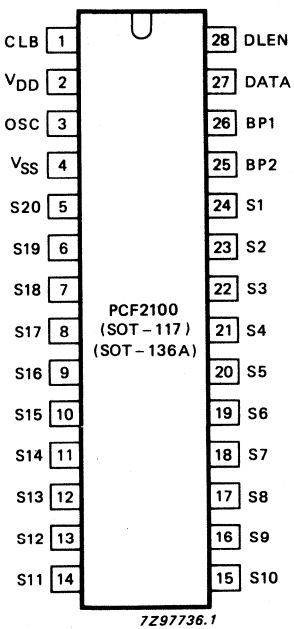


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
27	DATA	data line (CBUS)
28	DLEN	data line enable (CBUS)

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

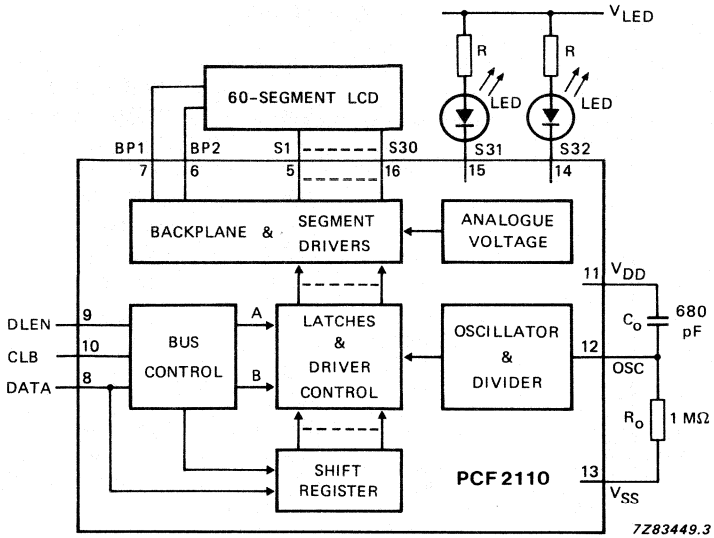


Fig. 3 Block diagram; PCF2110 (SOT-129).

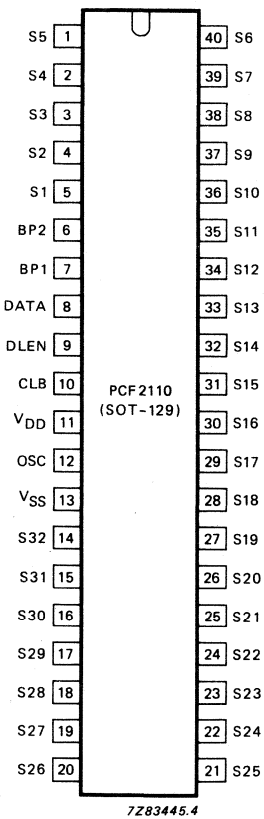


Fig. 4 Pinning diagram; PCF2110

DEVELOPMENT DATA

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

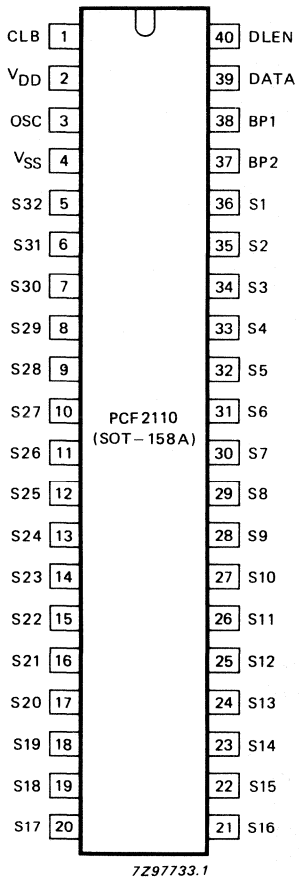


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

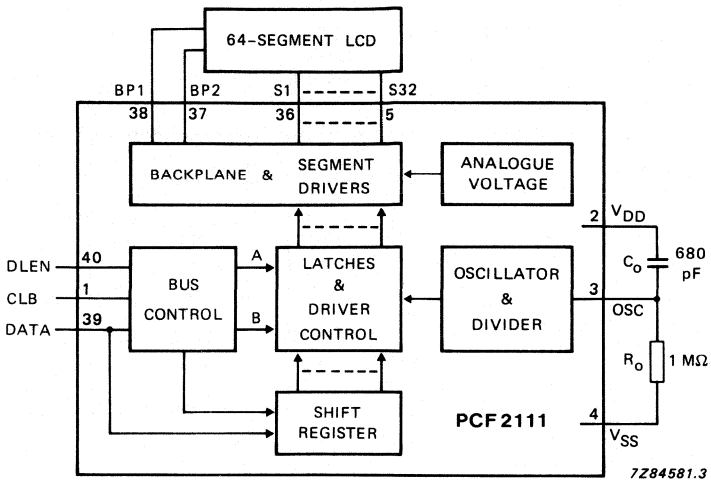


Fig. 6 Block diagram; PCF2111

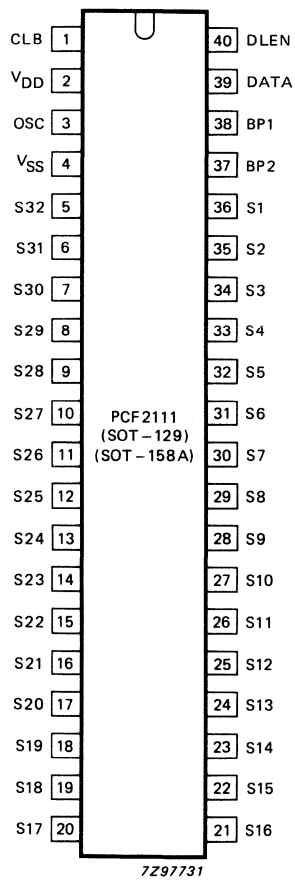


Fig. 7 Pinning diagram; PCF2111

DEVELOPMENT DATA

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line } CBUS
40	DLEN	data line enable } CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

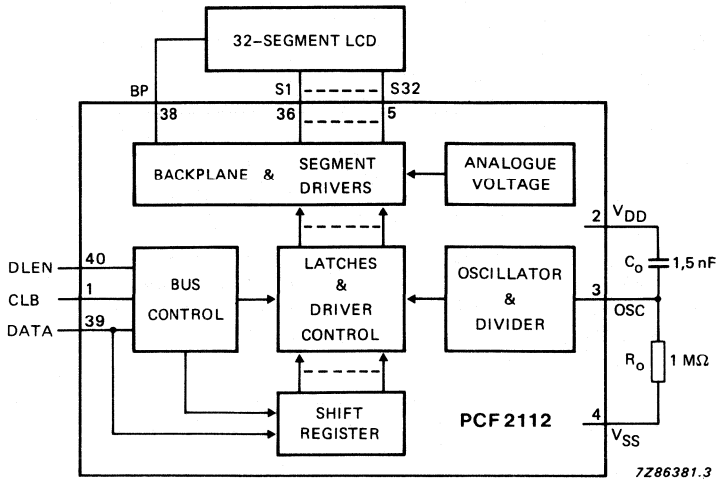


Fig. 8 Block diagram; PCF2112

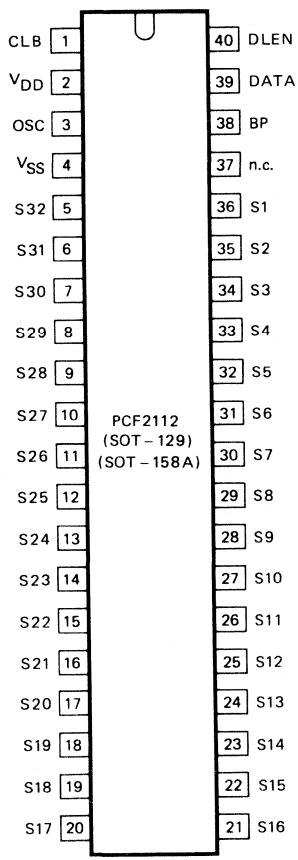


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

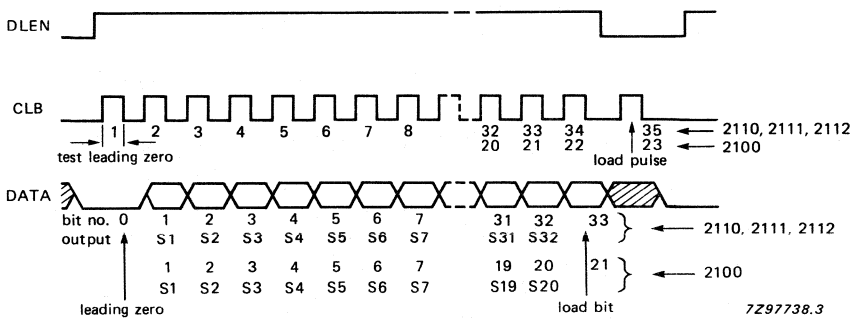


Fig. 10 CBUS data format.

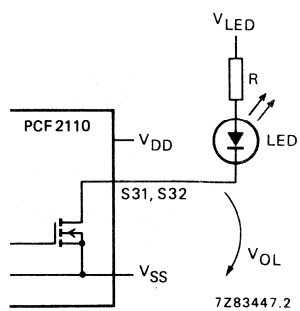


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

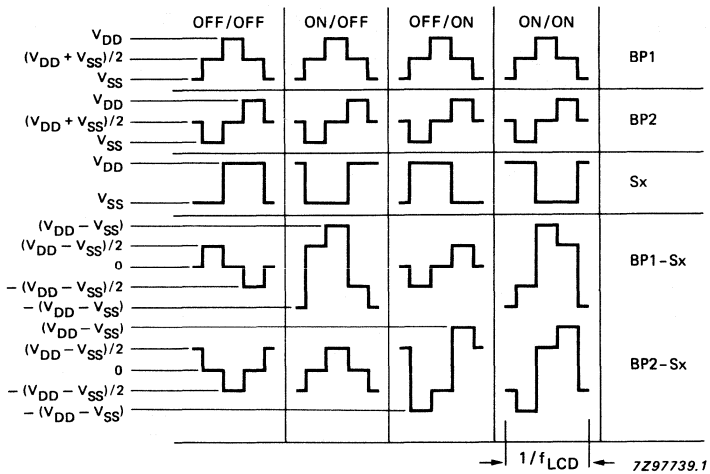


Fig. 12 Timing diagram (except PCF2112).

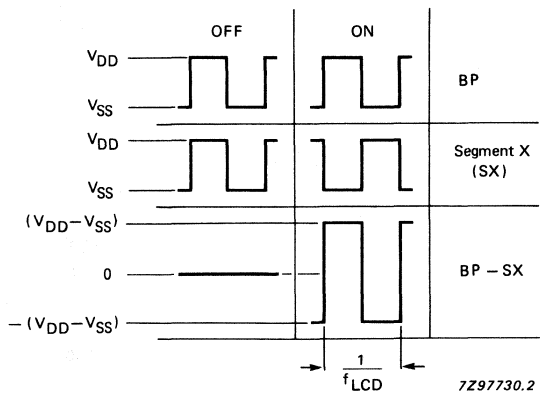


Fig. 13 Timing diagram for PCF2112.

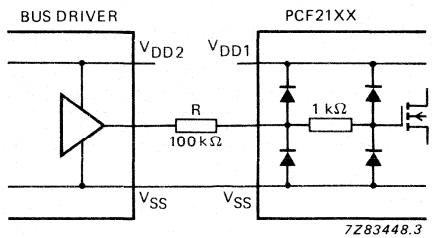
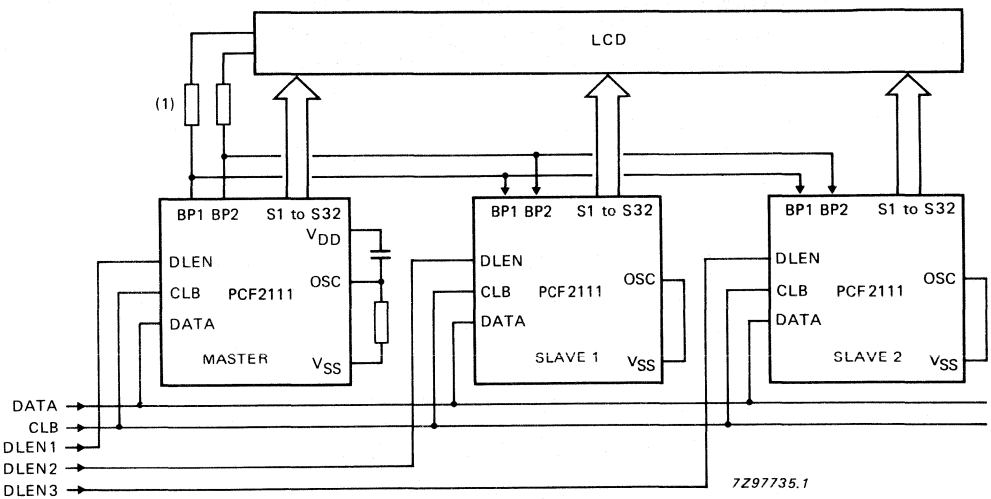


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be > 2,7 kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

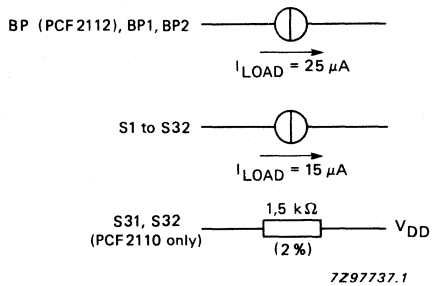


Fig. 16 Test loads.

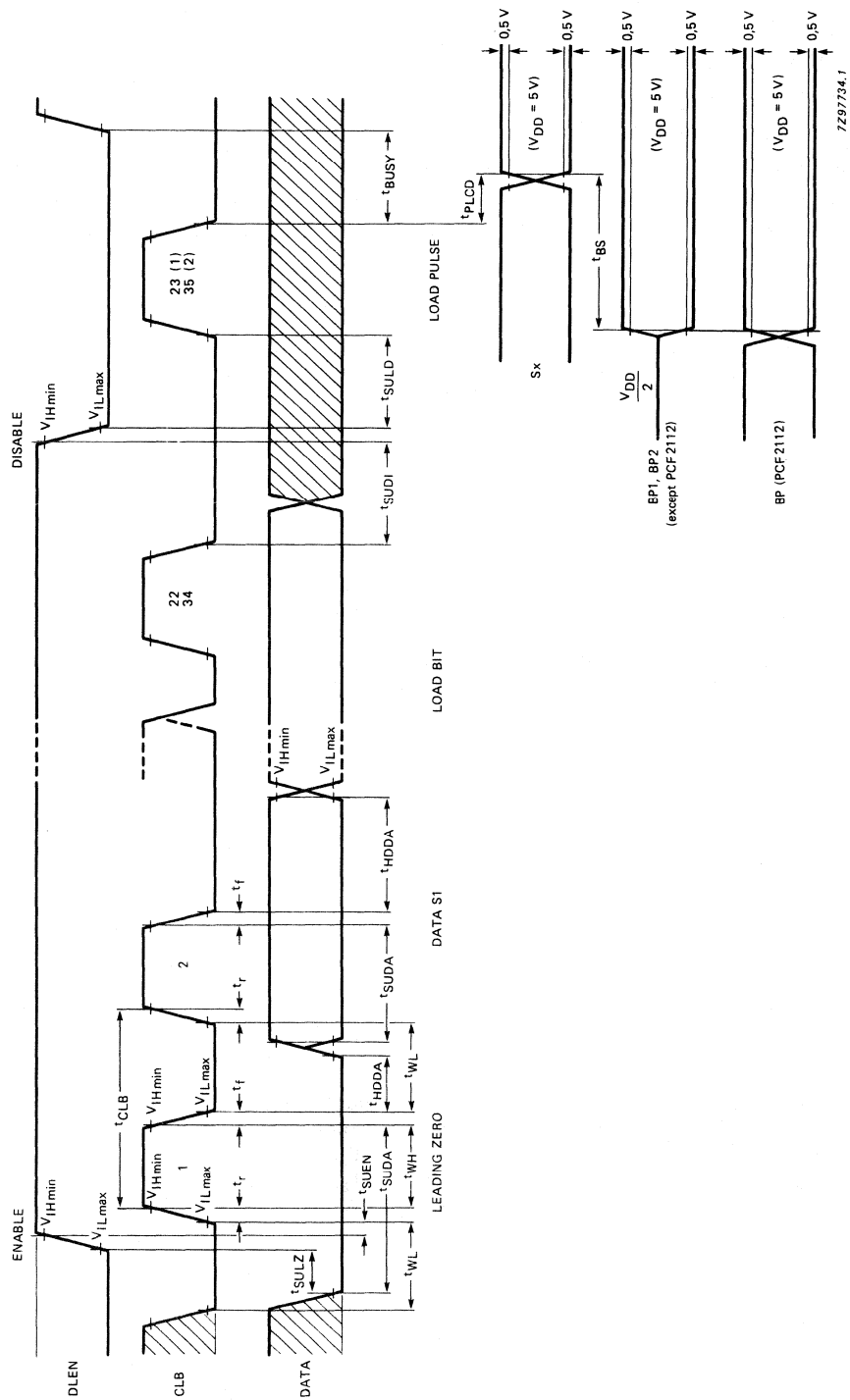


Fig. 17 CBUS timing.

(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

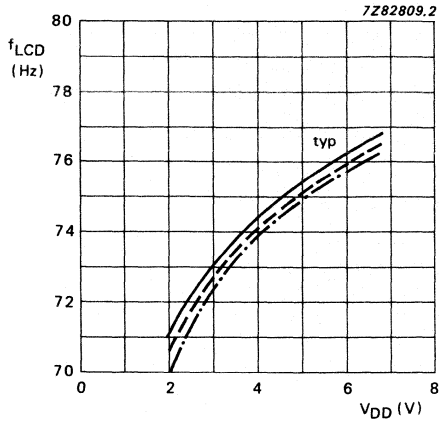


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

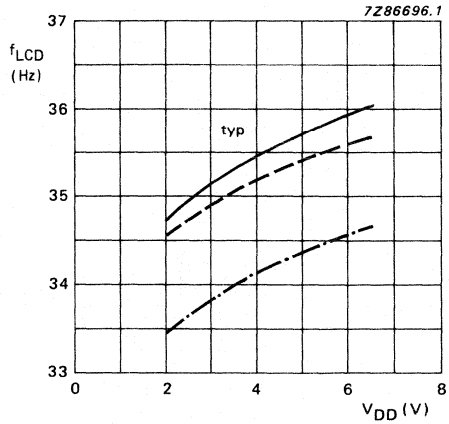


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

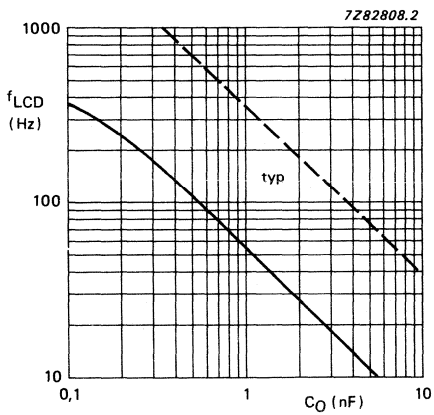


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

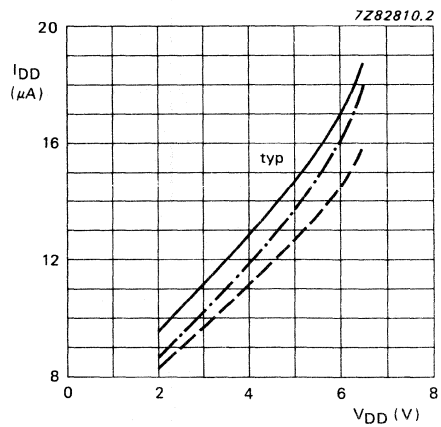


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

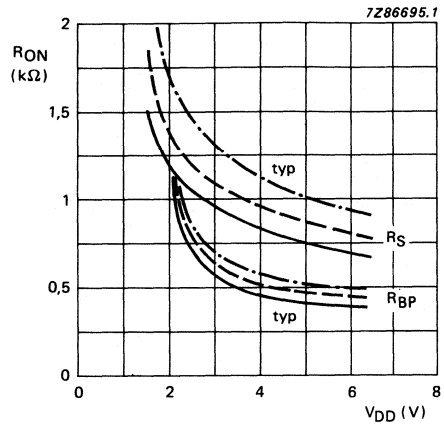


Fig. 22 Output resistance of backplane and segments.
——— $T_{amb} = -40\ ^{o}C$;
– – – – $T_{amb} = +25\ ^{o}C$;
– . – . – $T_{amb} = +85\ ^{o}C$.

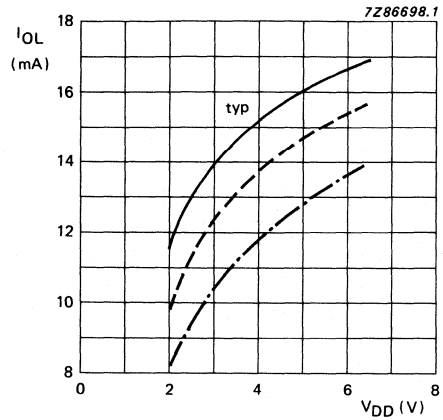


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— $T_{amb} = -40\ ^{o}C$;
– – – – $T_{amb} = +25\ ^{o}C$;
– . – . – $T_{amb} = +85\ ^{o}C$.

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I²C bus
- Software readable status word (parallel bus or I²C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	*	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

*Value to be fixed.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

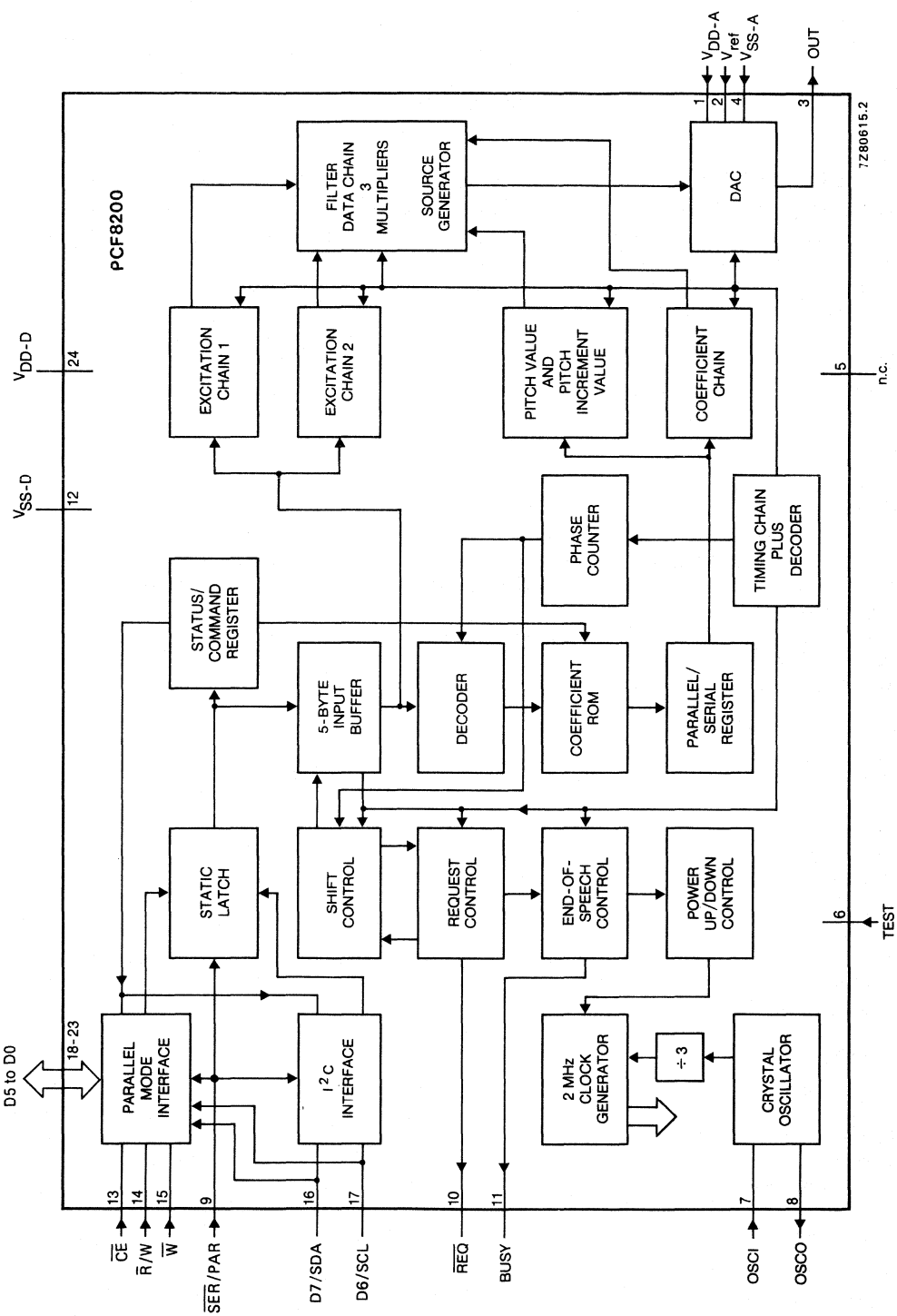


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

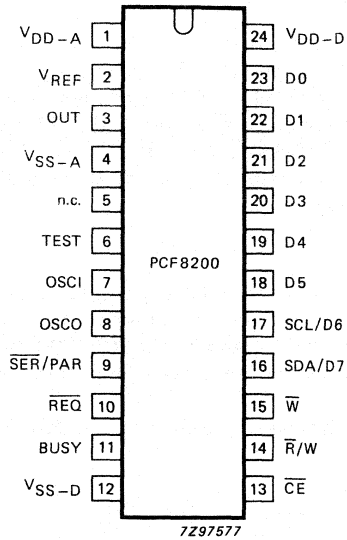


Fig. 2 Pinning diagram.

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	R/$\overline{W}$	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

	10	01	00	11	FS0, FS1
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms
FD1, FD0					

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

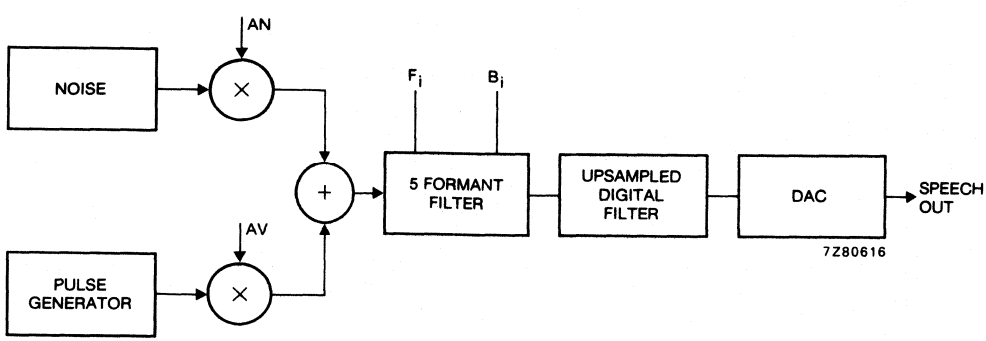


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

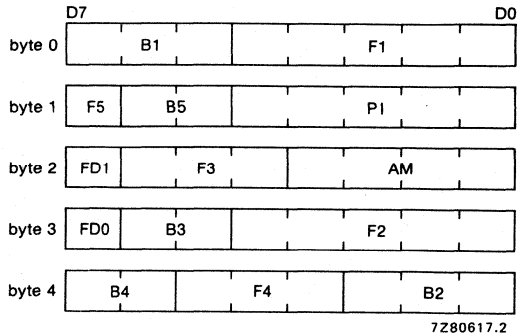
Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.

DEVELOPMENT DATA



It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

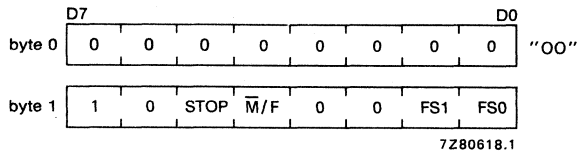


Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

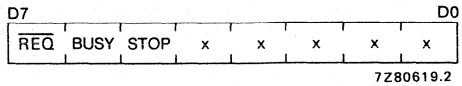


Fig. 6 Status read.

$\overline{REQ}$	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write. STOP = 1, BUSY = 0 stopped by the user. STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
$\overline{M}$/F	= 0	Male quantization table
STOP	= 0	
BUSY	= 0	Idle
$\overline{REQ}$	= 1	No data required

DEVELOPMENT DATA

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I²C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I²C ADDRESS

On chip there is a I²C slave receiver/transmitter with the address:

7 6 5 4 3 2 1 0
0 0 1 0 0 0 0 R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	−0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	−0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	−0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	−40	85	°C
Storage temperature range		T_{stg}	−55	125	°C

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, R/$\overline{W}$, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	* (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	*	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

* Values not yet available.

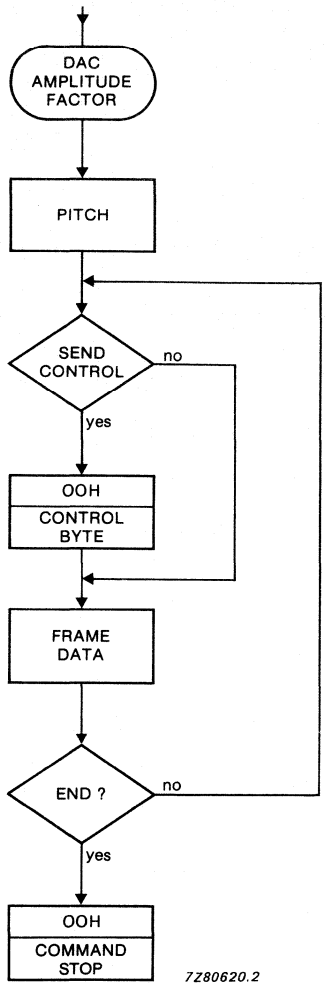
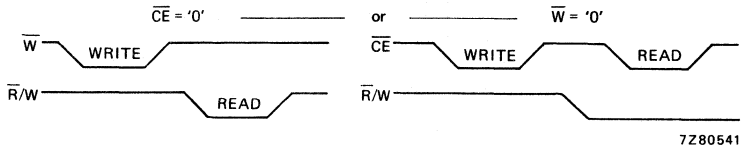


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

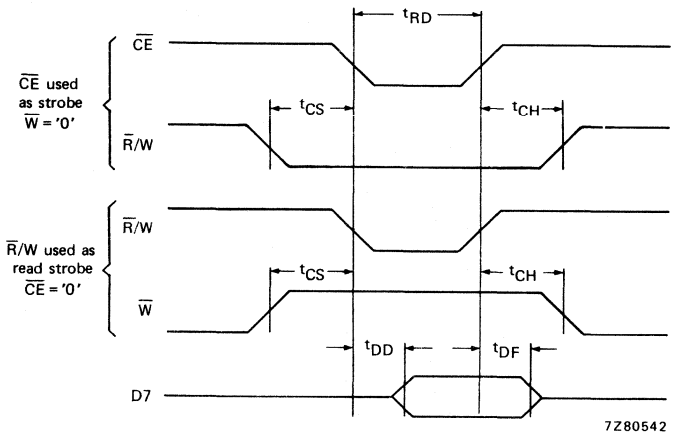


Fig. 8 Read timing.

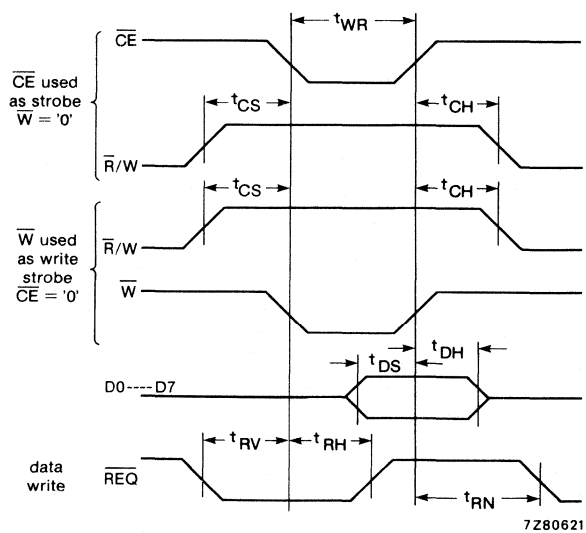


Fig. 9 Write timing.

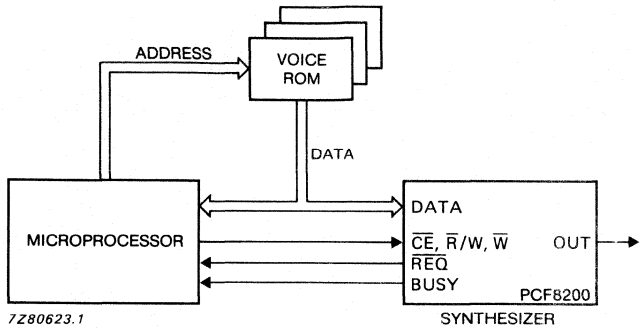


Fig. 10 Typical application configuration with parallel interface.

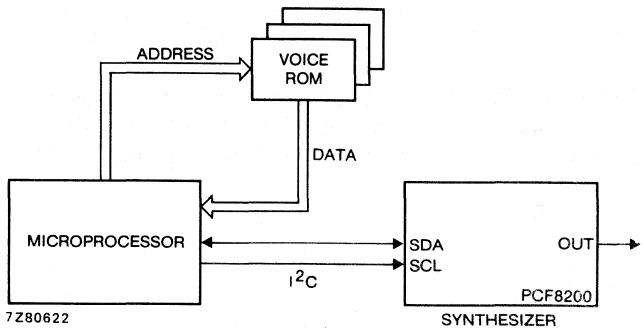


Fig. 11 Typical application configuration with series interface.

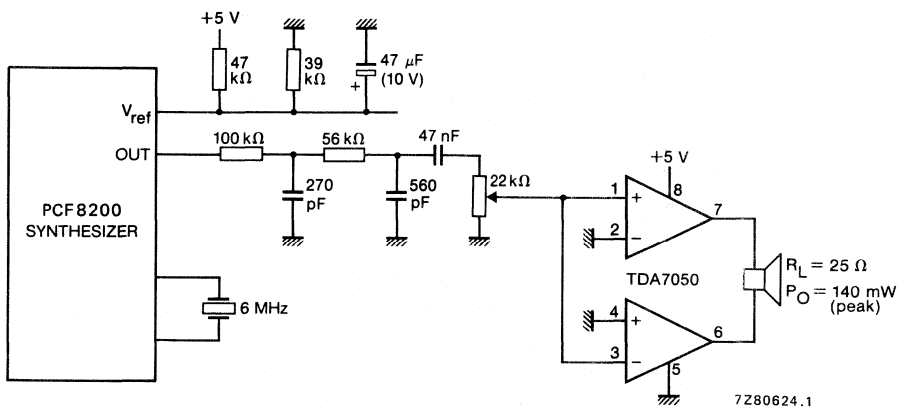


Fig. 12 An example of an output configuration.

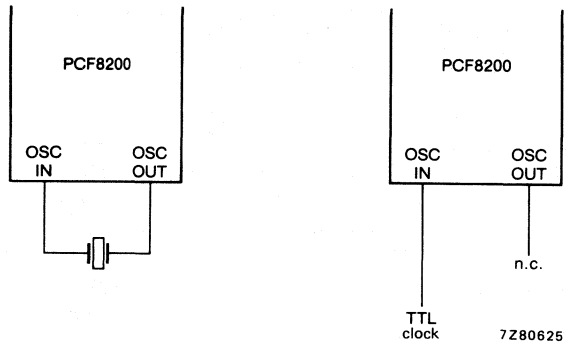


Fig. 13 Oscillator clock configurations.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the PCF84CXXX family. For detailed information, consult the PCF84CXXX data sheet.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: −40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

* See PCF84CXXX family Data Sheet.

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

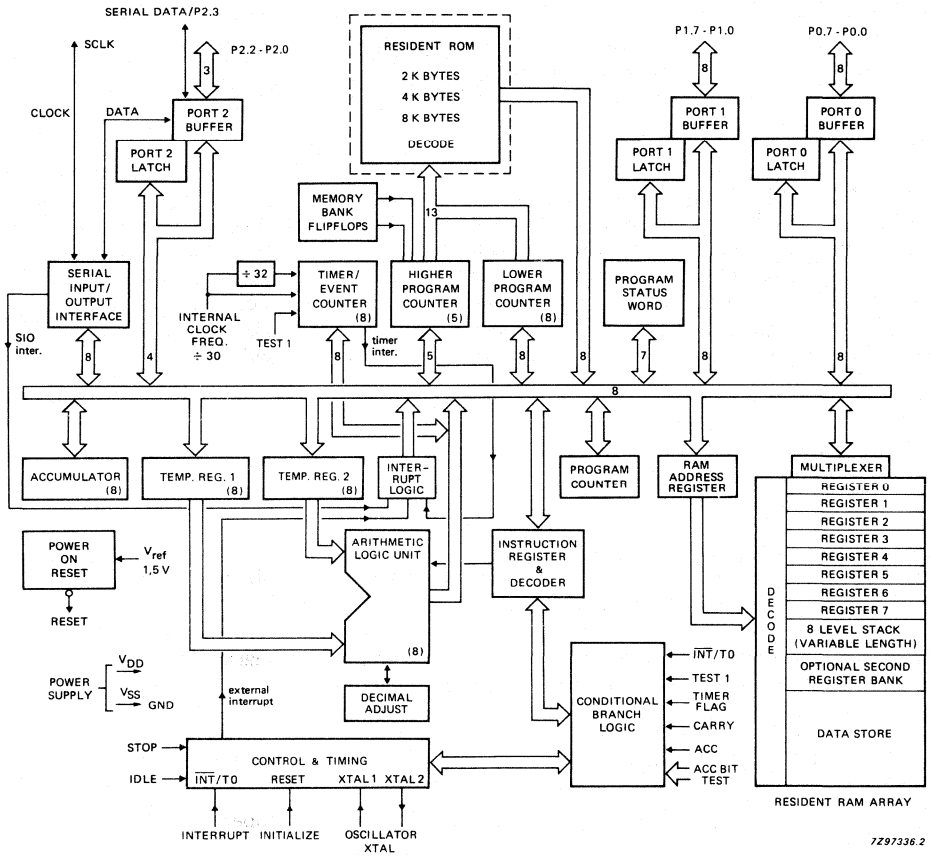


Fig. 1 Block diagram.

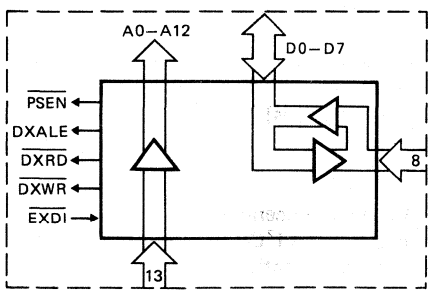


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

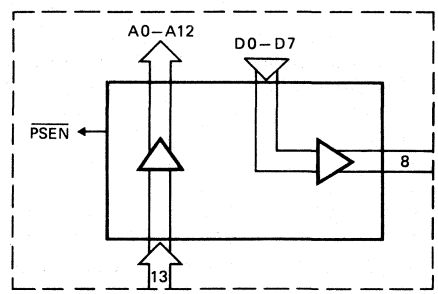


Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

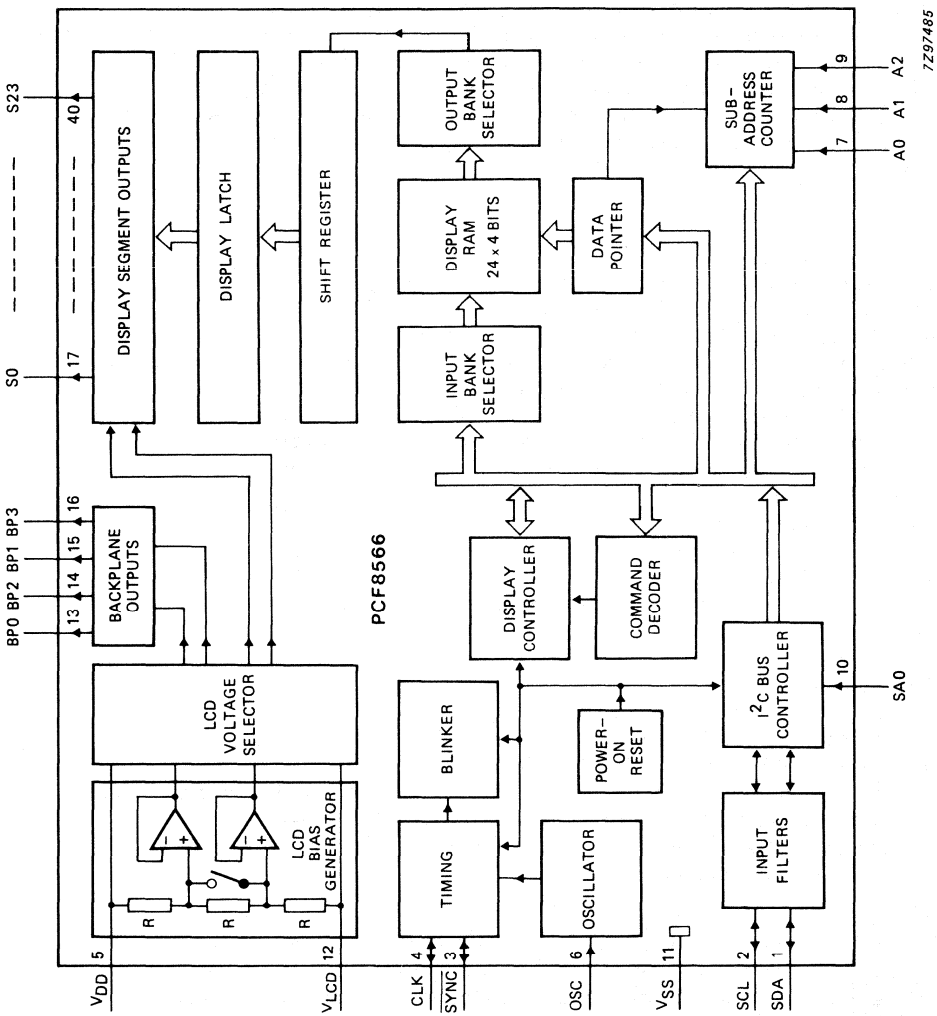


Fig. 1 Block diagram.

DEVELOPMENT DATA

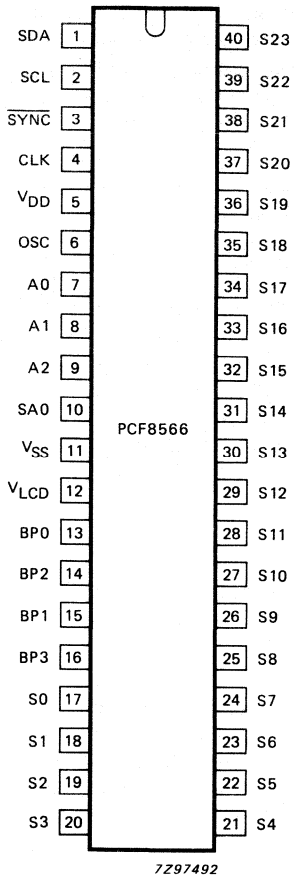


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 40	S0 to S23	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

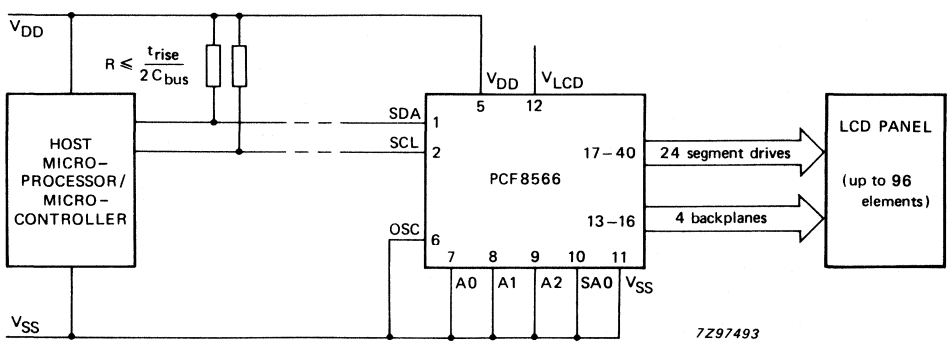


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

DEVELOPMENT DATA

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

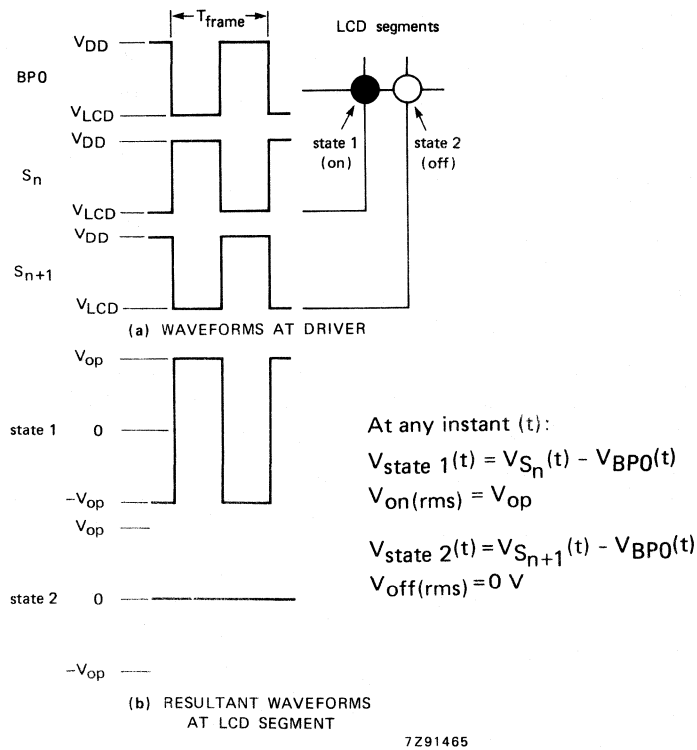


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

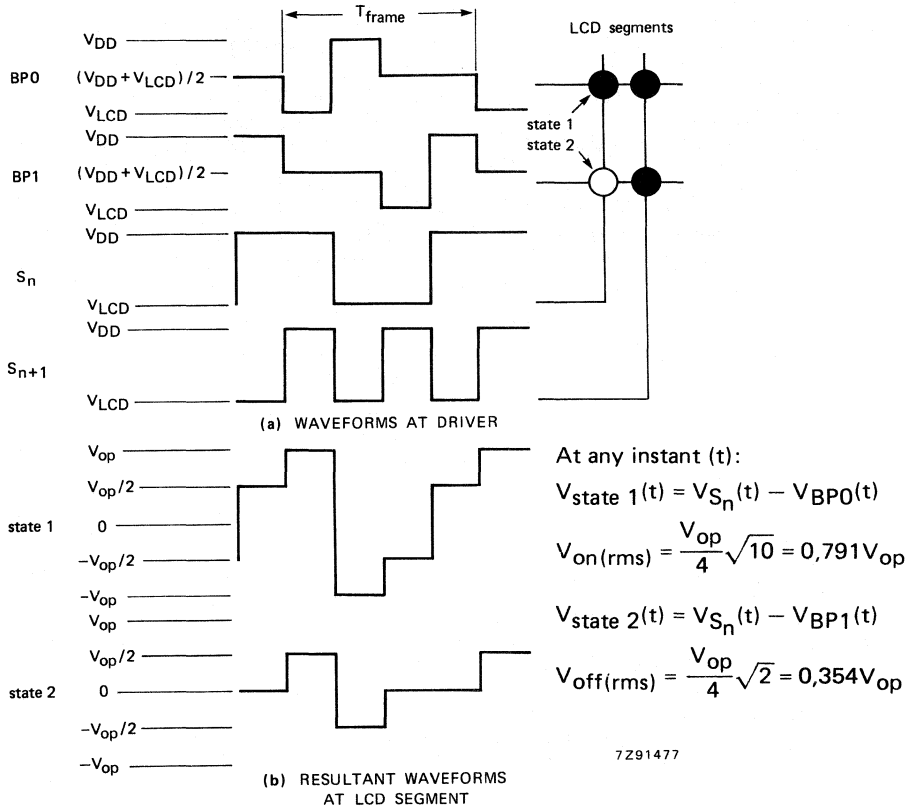


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

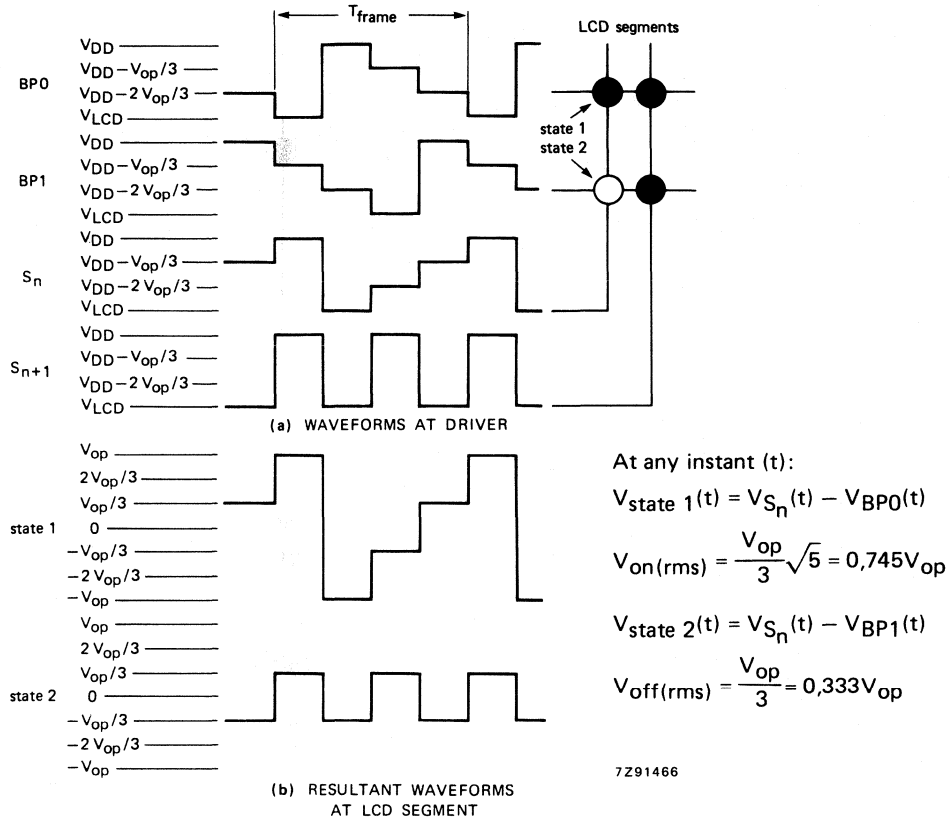


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

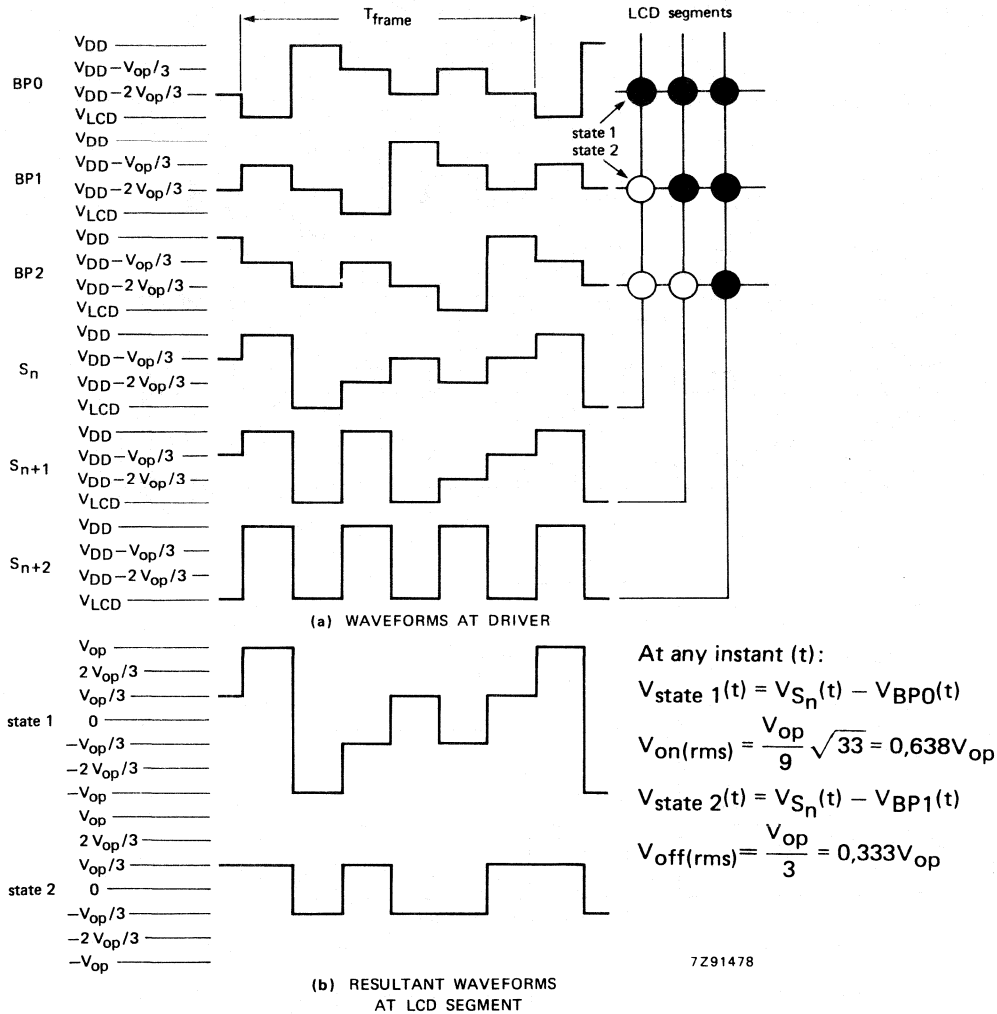


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

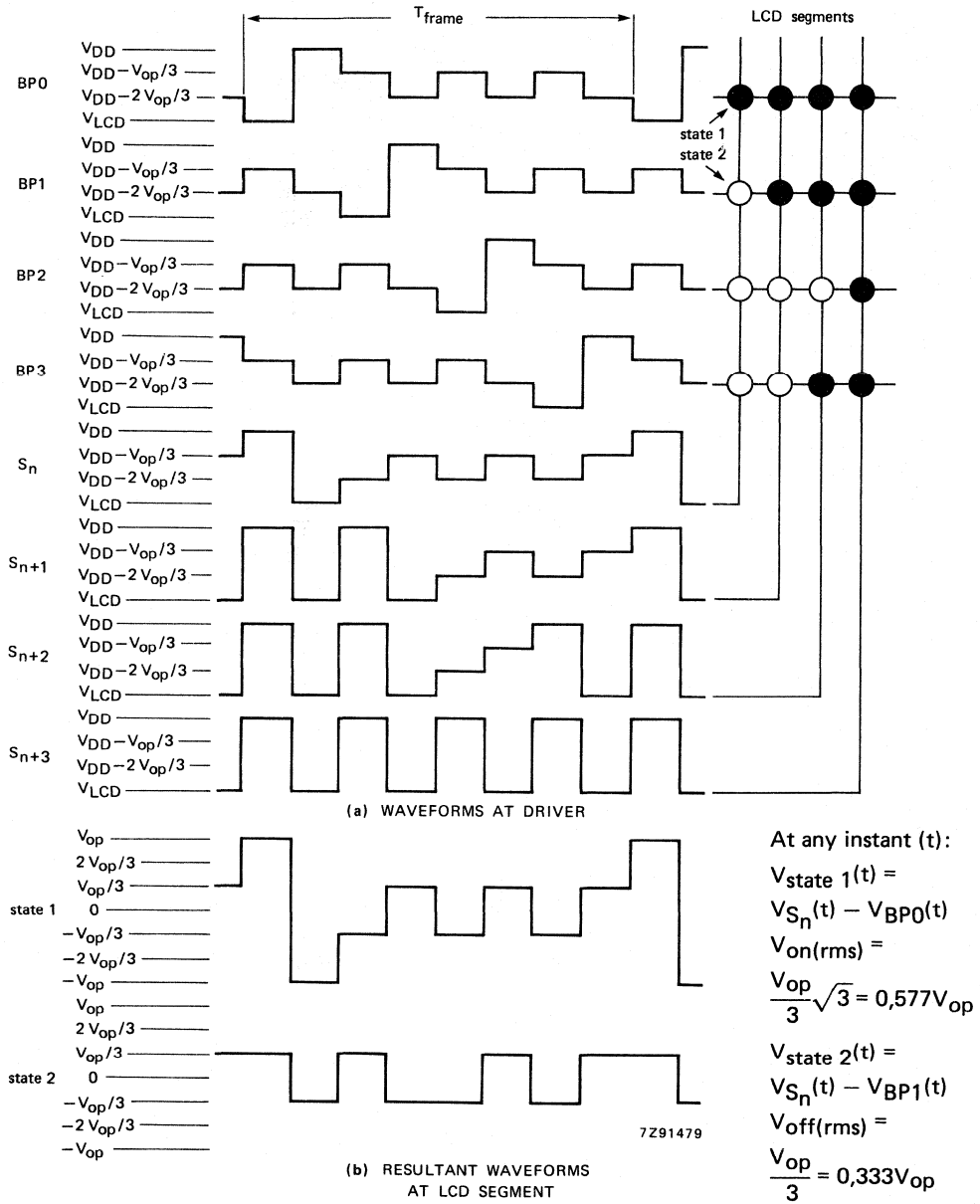


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

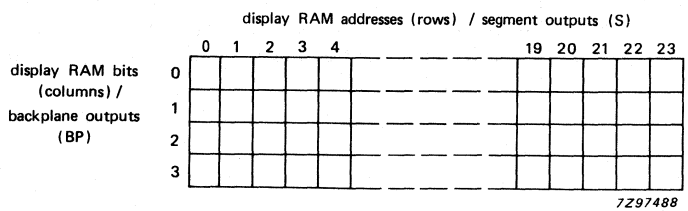


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

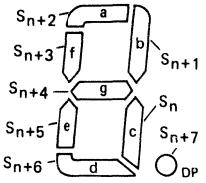
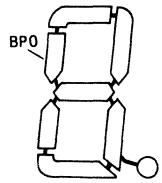
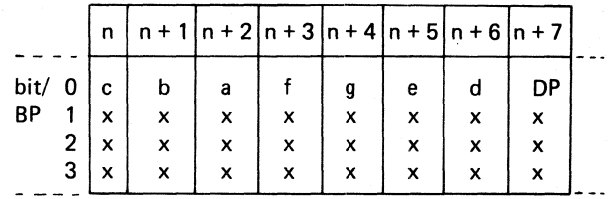
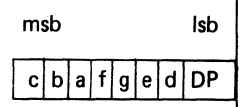
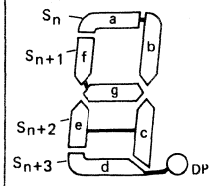
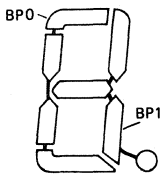
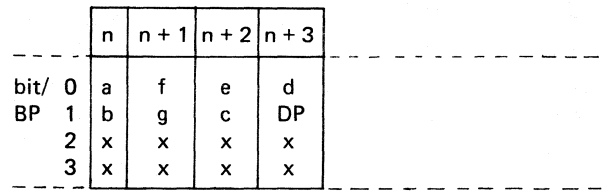
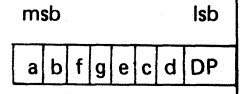
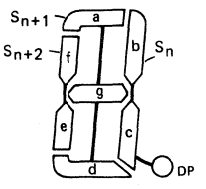
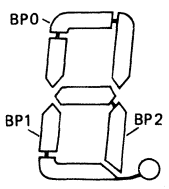
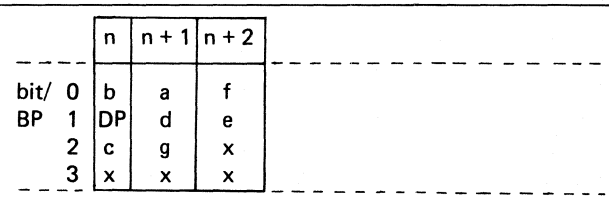
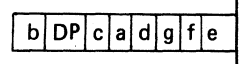
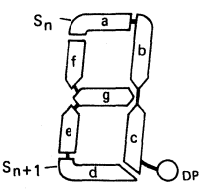
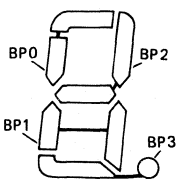
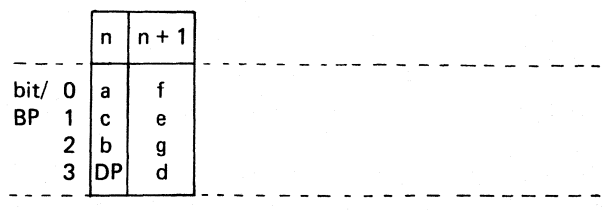
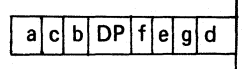
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

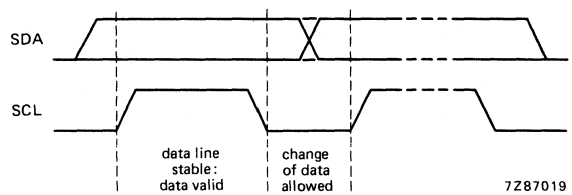


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

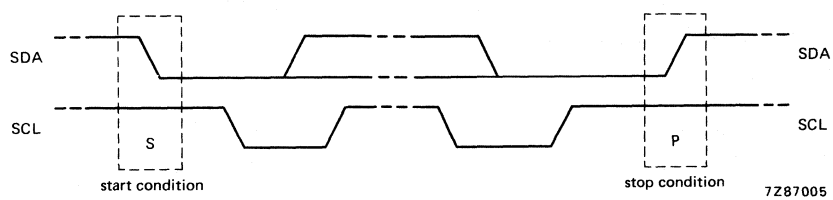


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

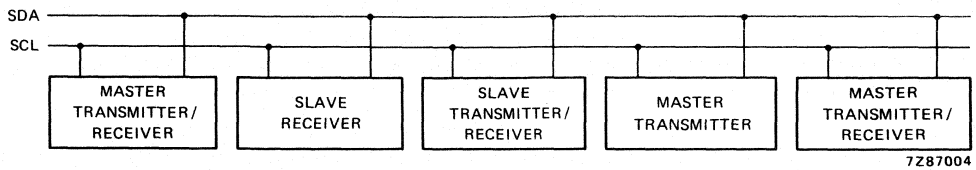


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

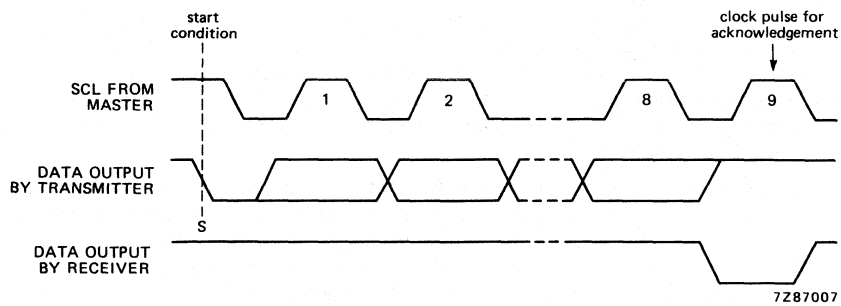


Fig. 14 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are available on request.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

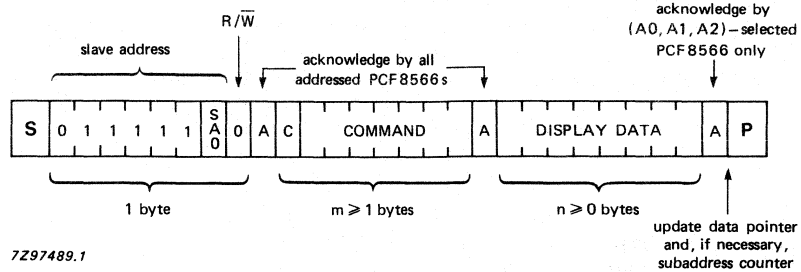


Fig. 15 I^2C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I^2C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

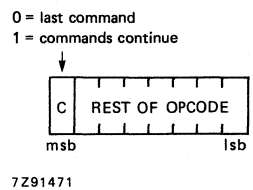


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td><table><tr><th>static</th><th>1 : 2 MUX</th><th>bit I</th></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table><table><tr><th>static</th><th>1 : 2 MUX</th><th>bit O</th></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table></td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td><table><tr><th>blink frequency</th><th>bits BF1</th><th>BF0</th></tr><tr><td>off</td><td>0</td><td>0</td></tr><tr><td>2 Hz</td><td>0</td><td>1</td></tr><tr><td>1 Hz</td><td>1</td><td>0</td></tr><tr><td>0,5 Hz</td><td>1</td><td>1</td></tr></table><table><tr><th>blink mode</th><th>bit A</th></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table></td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

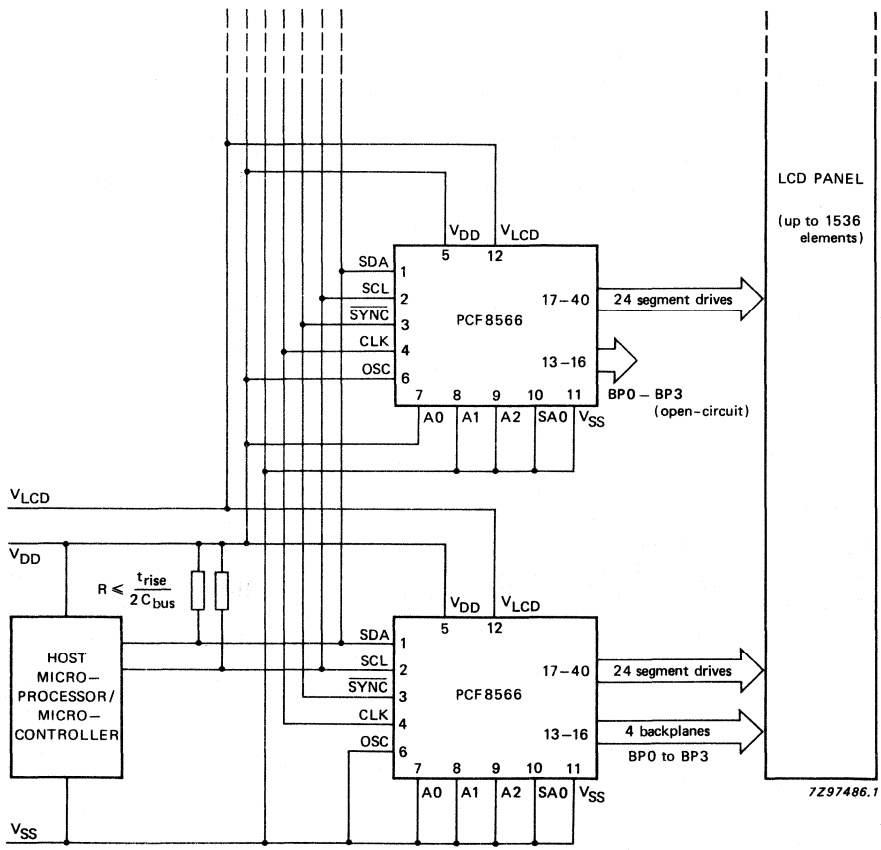


Fig. 17 Cascaded PCF8566 configuration.

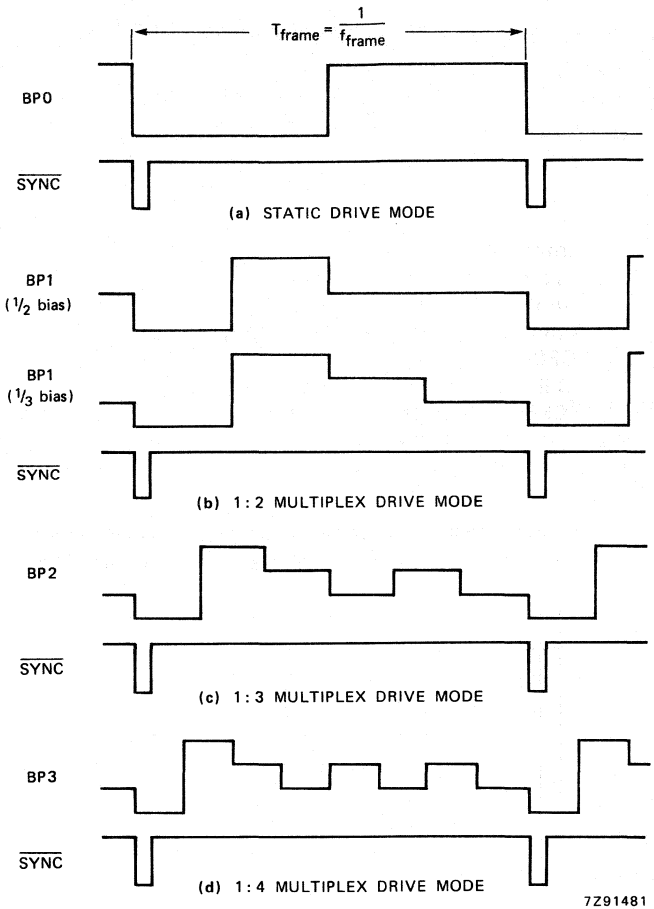


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}	$-0,5$ to $+7$	V
LCD supply voltage range	V_{LCD}	$V_{DD} -7$ to V_{DD}	V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I	$V_{SS} -0,5$ to $V_{DD} + 0,5$	V
Output voltage range (S0 to S23; BP0 to BP3)	V_O	$V_{LCD} -0,5$ to $V_{DD} + 0,5$	V
DC input current	$\pm I_I$	max. 20	mA
DC output current	$\pm I_O$	max. 25	mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max. 50	mA
Power dissipation per package	P_{tot}	max. 400	mW
Power dissipation per output	P_O	max. 100	mW
Storage temperature range	T_{stg}	-65 to $+150$	°C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

$V_{SS} = 0$ V; $V_{DD} = 2,5$ to 6 V; $V_{LCD} = V_{DD} -2,5$ to $V_{DD} -6$ V;

$T_{amb} = -40$ to $+85$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	$V_{DD} -6$	–	$V_{DD} -2,5$	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	3	7,0	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

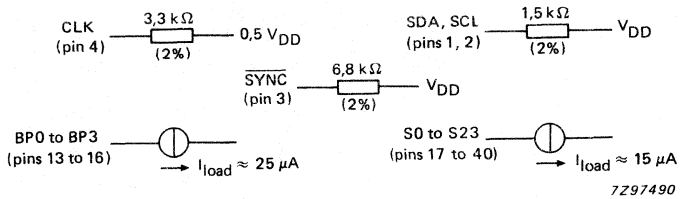


Fig. 19 Test loads.

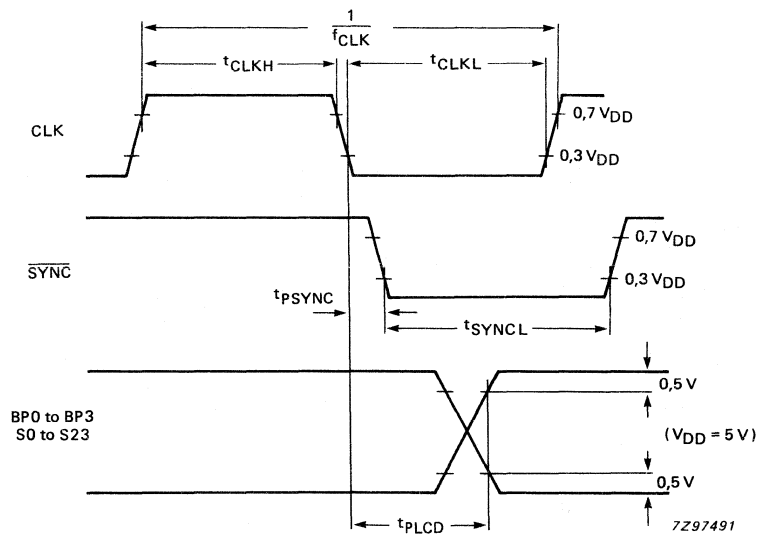


Fig. 20 Driver timing waveforms.

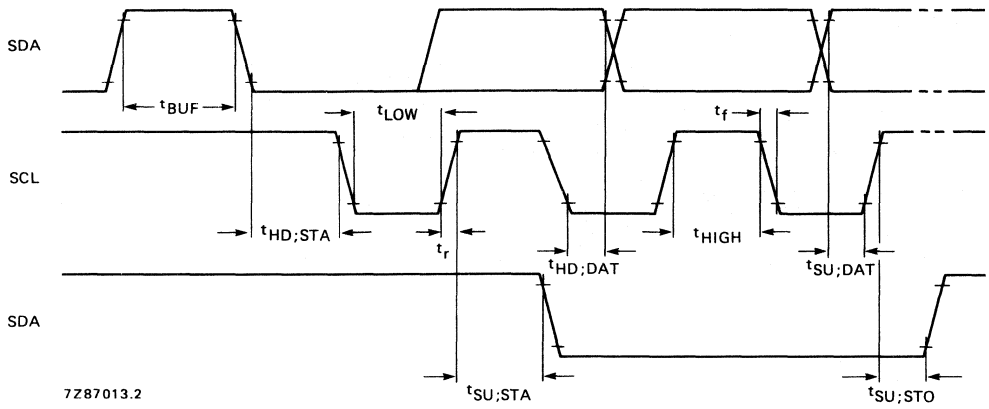
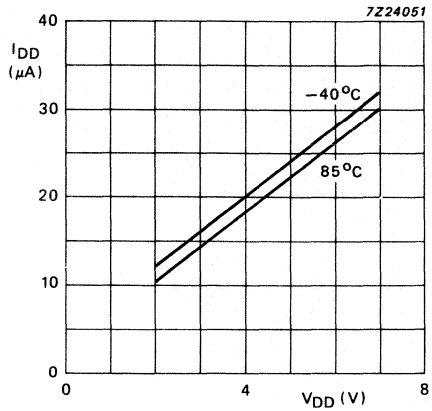
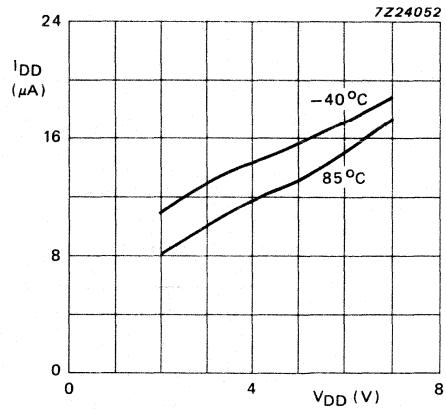


Fig. 21 I^2C bus timing waveforms.



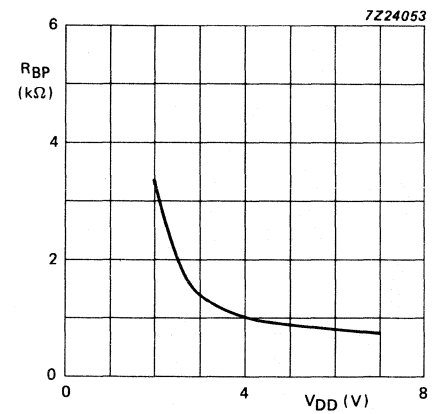
(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.



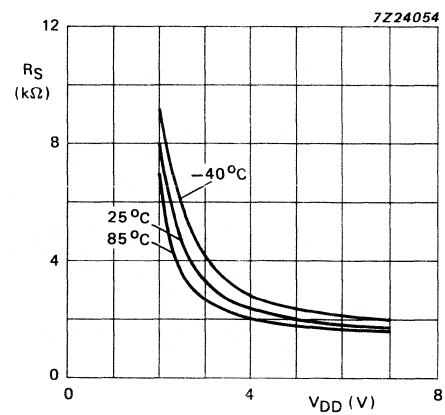
(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

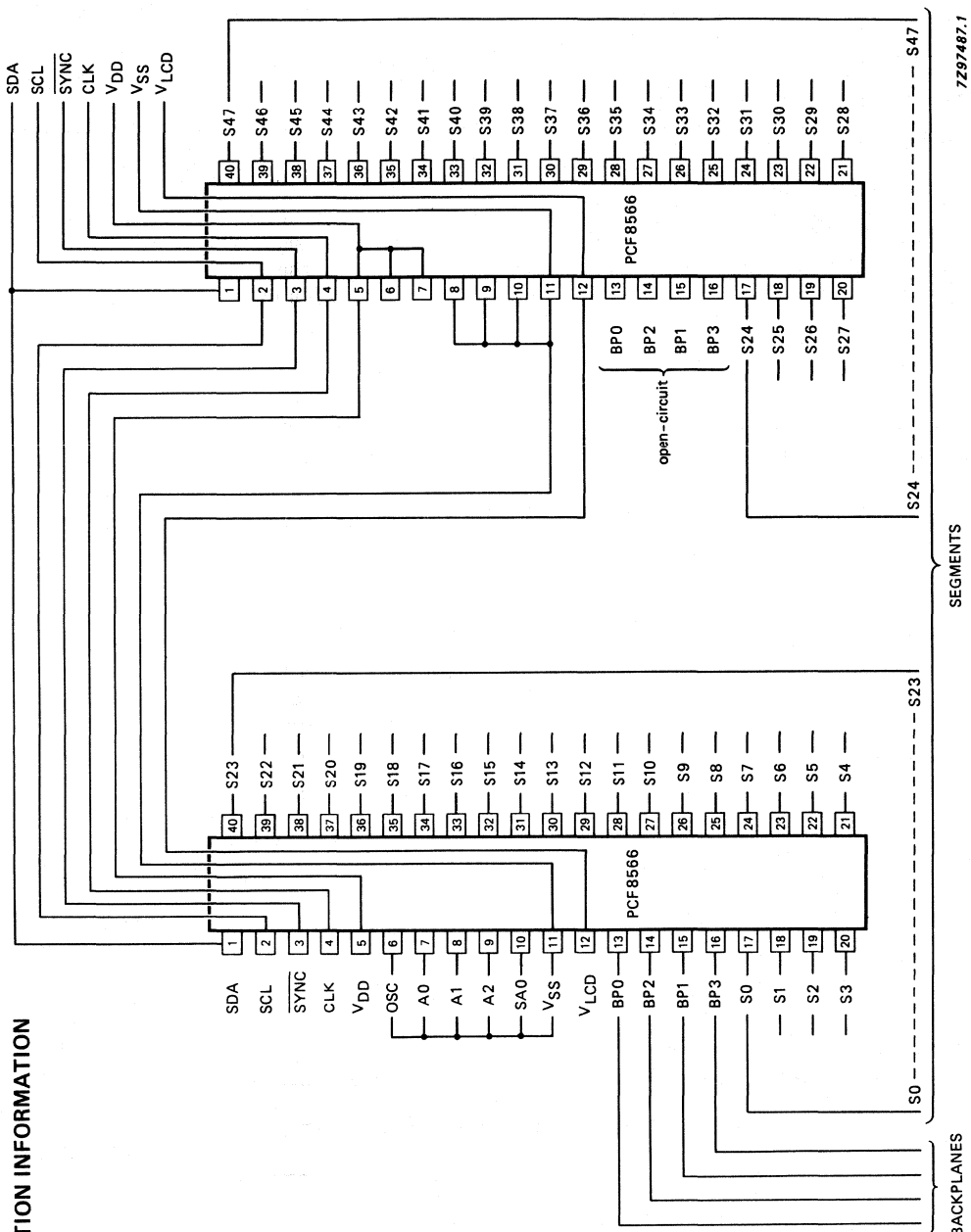


Fig. 24 Single plane wiring of packaged PCF8566s.

128 x 8 BIT/256 x 8 BIT STATIC RAMs WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

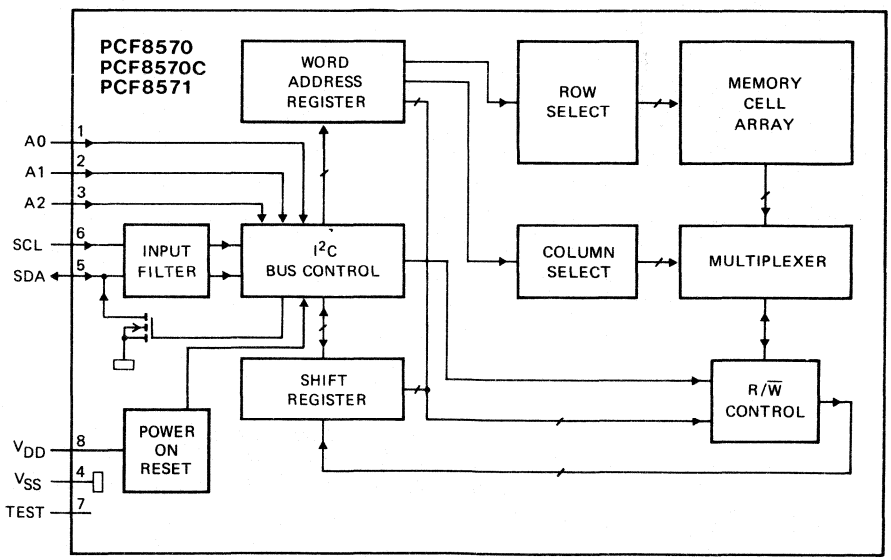


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

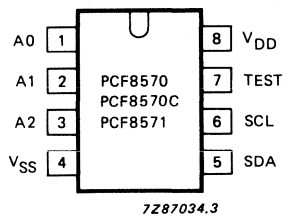


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
DC input current (any input)	$\pm I_I$	max.	10	mA
DC output current (any output)	$\pm I_O$	max.	10	mA
Supply current (pin 8 or pin 4)	$\pm I_{DD}$; I_{SS}	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD};					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 12 and 13)					
Supply current at T_{amb} = 25 °C; TEST = V_{DD};					
PCF8570/8570C	I_{DDR}	–	50	400	nA
PCF8571	I_{DDR}	–	50	200	nA
Recovery time	t_{HD2}	–	50	–	μs

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

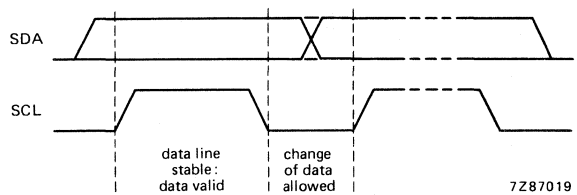


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

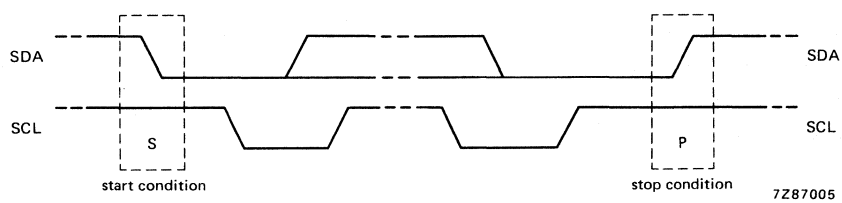


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

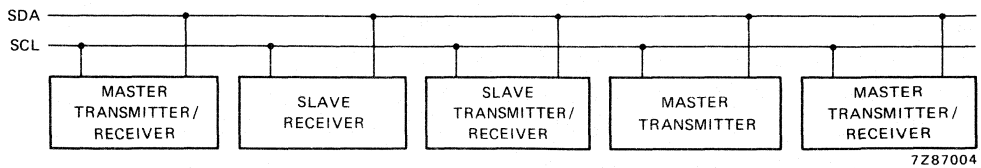


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

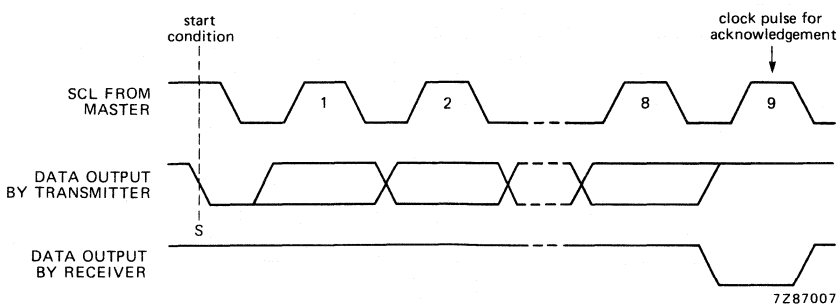


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

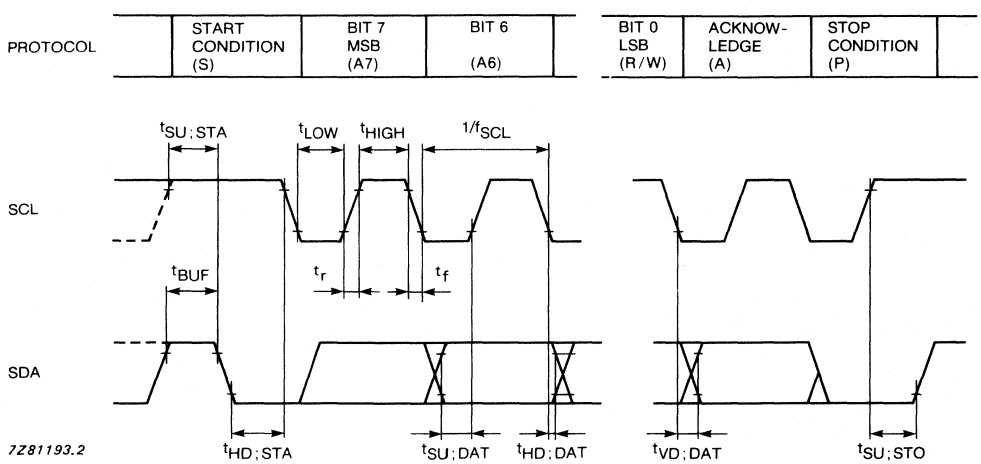


Fig. 7 I²C bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig. 8.

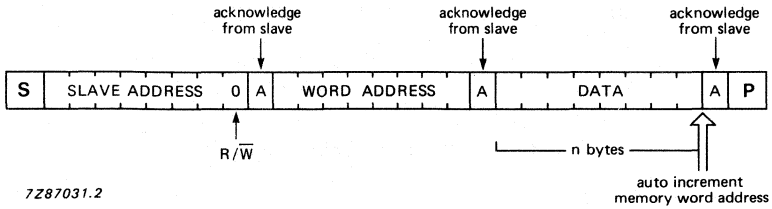


Fig. 8(a) Master transmits to slave receiver (WRITE mode).

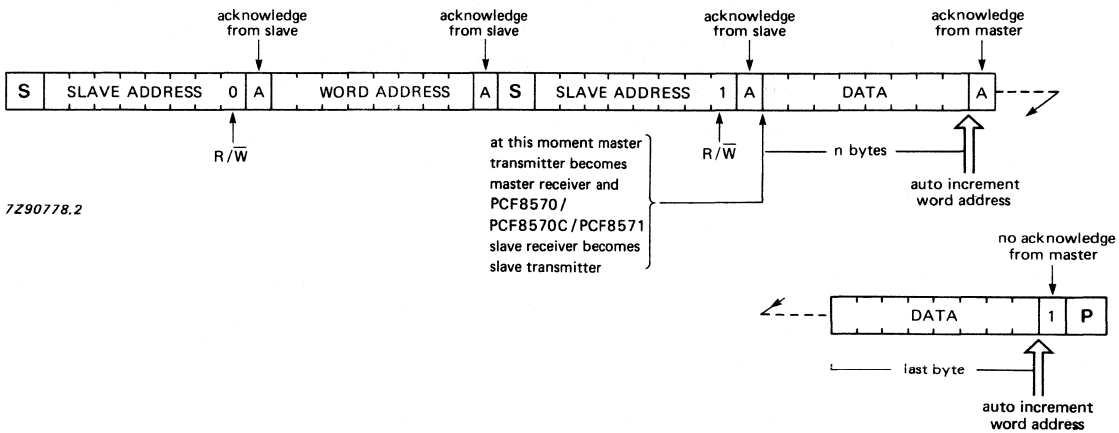


Fig. 8(b) Master reads after setting word address (WRITE word address; READ data).

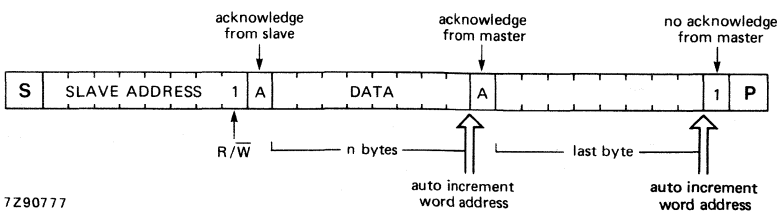


Fig. 8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig. 10).

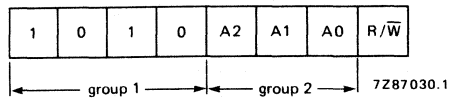


Fig. 9 PCF8570 and PCF8571 address.

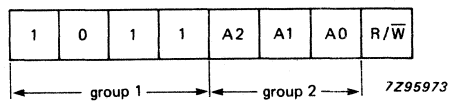


Fig. 10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

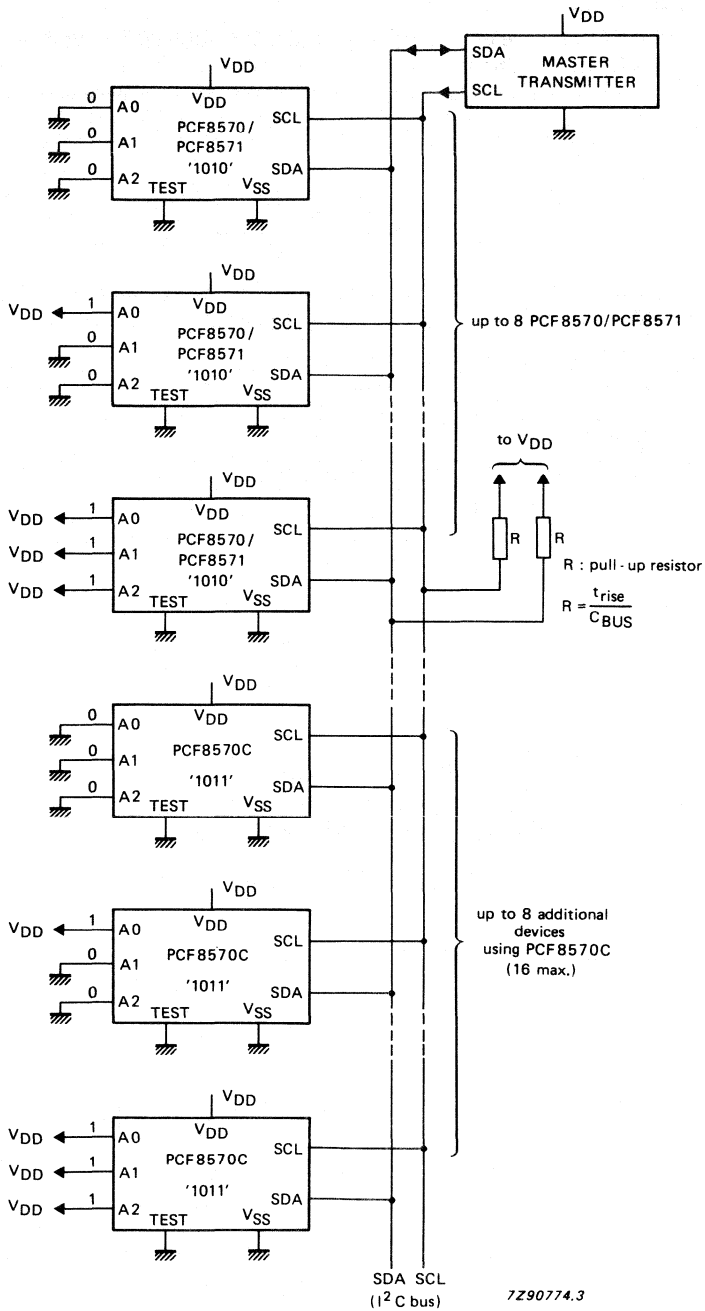
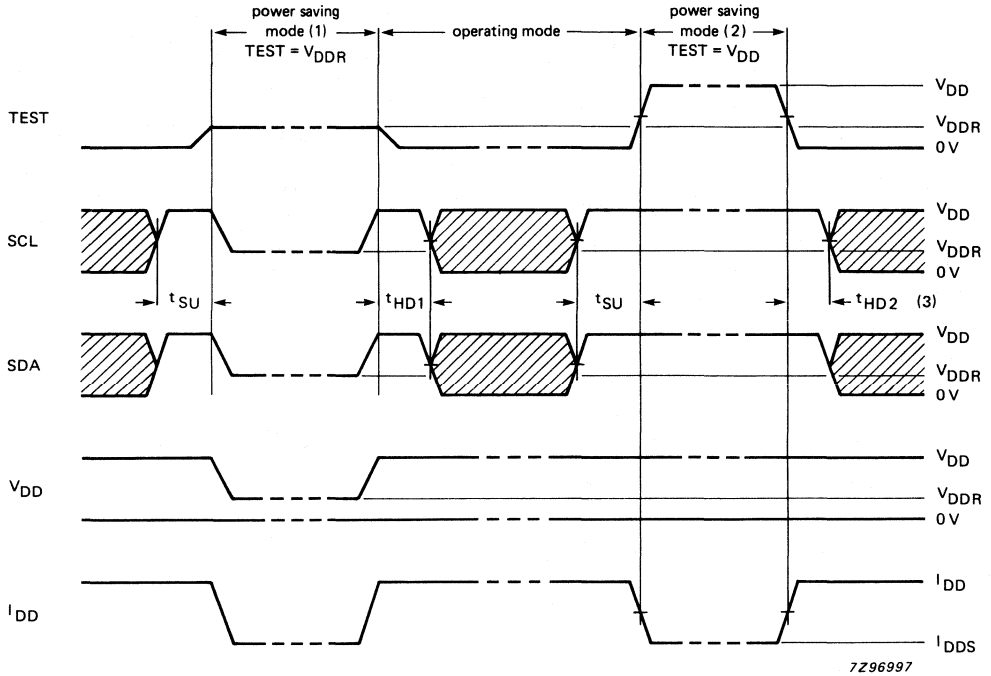


Fig. 11 Application diagram.

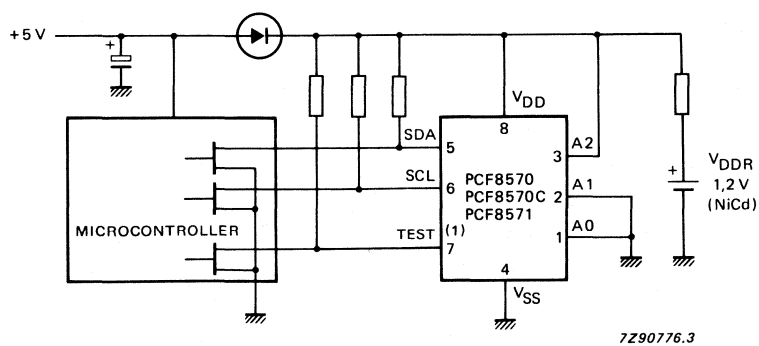
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig. 12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

Fig. 13 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS peripheral circuit that functions as a real time clock/calendar with an Inter IC (I^2C) bus interface.
The device incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA are also available. Information is transferred via a serial, two-line bidirectional bus (I^2C). Back-up for the clock during supply interruption is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	–	6,0	V
Supply voltage (I^2C interface)		$V_{DD}-V_{SS2}$	2,5	–	6,0	V
Crystal oscillator		f_{osc}	–	32,768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

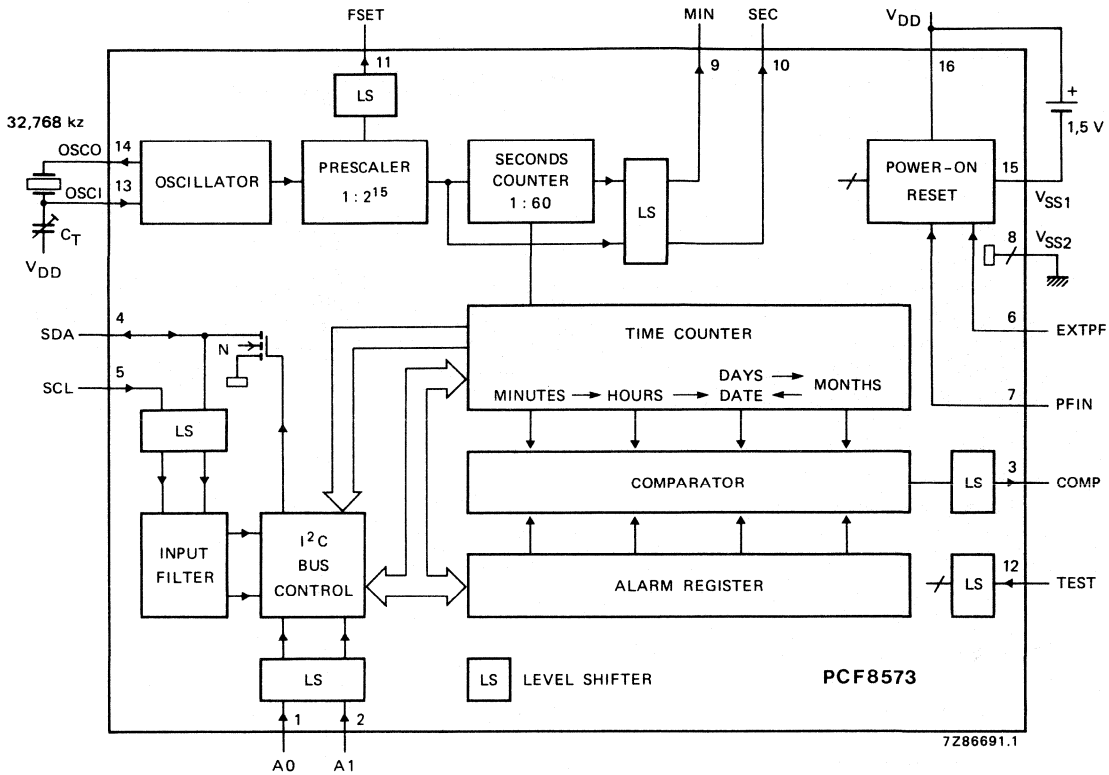


Fig. 1 Block diagram.

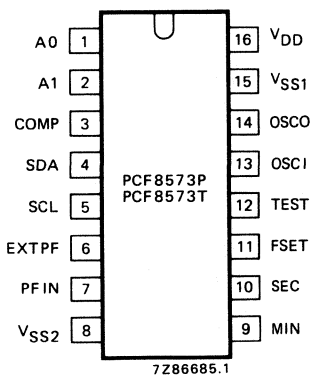


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

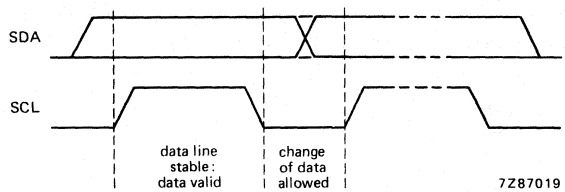


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

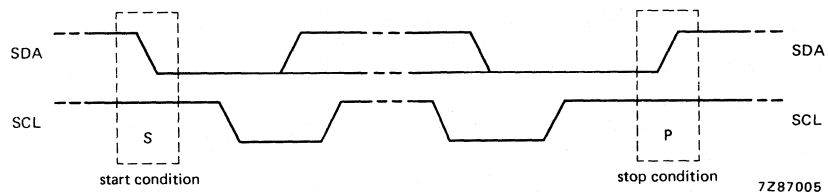


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

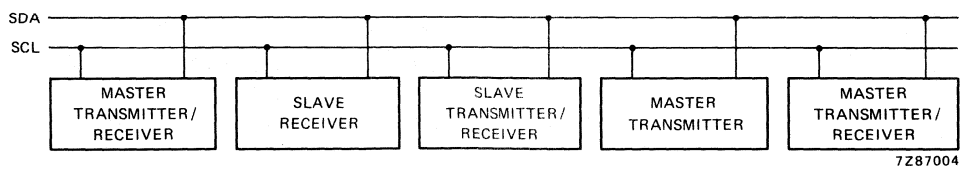


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 11 and Fig. 12.)

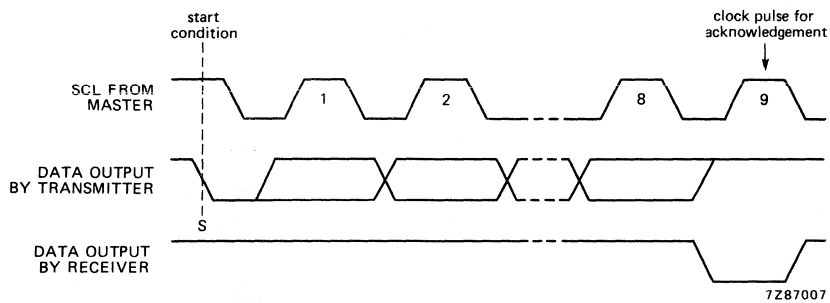


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

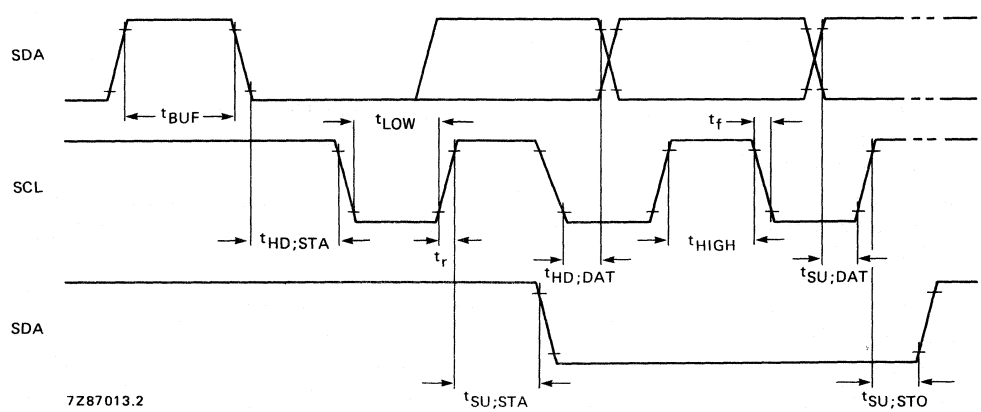


Fig. 7 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

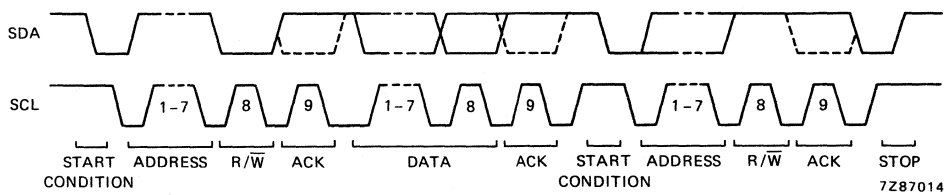


Fig. 8 Complete data transfer.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 9.

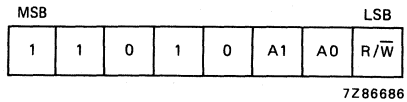


Fig. 9 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 10 and Fig. 11.

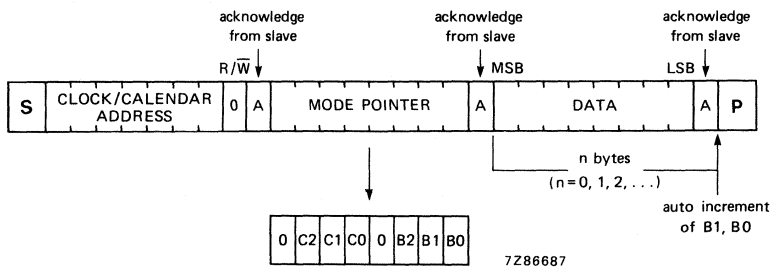


Fig. 10 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

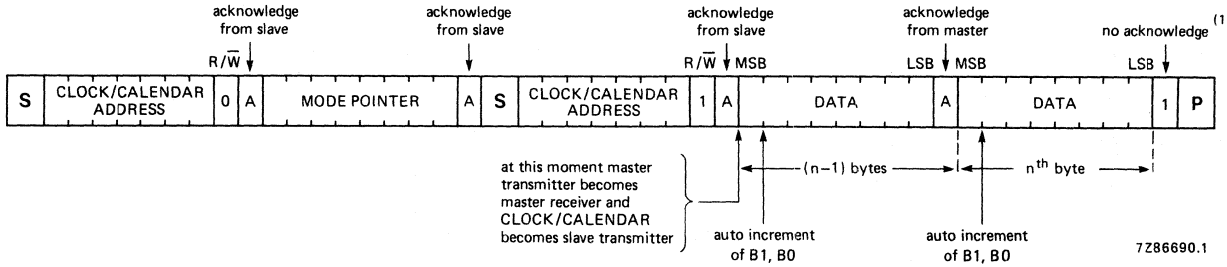
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

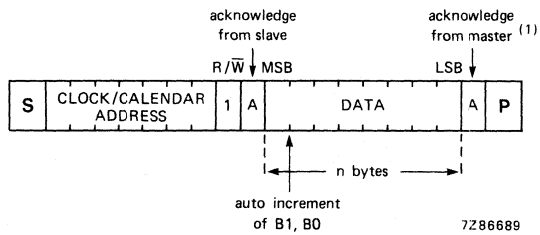
"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 11 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 12 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit.

* = minutes.

** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage ranges		$V_{DD}-V_{SS1}$	−0,3	8	V
		$V_{DD}-V_{SS2}$	−0,3	8	V
Voltage input (pins 4; 5)		V_I	$V_{SS2}-0,8$	$V_{DD}+0,8$	V*
Voltage input (pins 6; 7; 13, 14)		V_I	$V_{SS1}-0,6$	$V_{DD}+0,6$	V
Voltage on any other pin		V_I	$V_{SS2}-0,6$	$V_{DD}+0,6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage I^2C interface		$V_{DD}-V_{SS2}$	2,5	5,0	6,0	V
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	1,5	$V_{DD}-V_{SS2}$	V
Supply current V_{SS1}	$V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}	$V_{DD}-V_{SS2}$ = 5 V; (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current	$V_I = V_{SS2}$ to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN						
Input voltage HIGH		$V_{IH}-V_{SS1}$	0,7 x $V_{DD}-V_{SS1}$	–	–	V
Input voltage LOW		$V_{IL}-V_{SS1}$	0	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD} T_{amb} = 25 °C;	$\pm I_I$	–	–	1,0	μA
	$V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	0,1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1,2	1,4	V
Power "ON" reset	$V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0,3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency at SCL	$V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (Fig. 7)		t_{LOW}	4,7	–	–	μs
Pulse width HIGH (Fig. 7)		t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input		T_I	0,25	1	2,5	μs
Input capacitance (SDA; SCL)		C_I	–	–	7	pF
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters	f = 32,768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	9	–	pF
Trimmer capacitance		C_T	5	–	25	pF

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

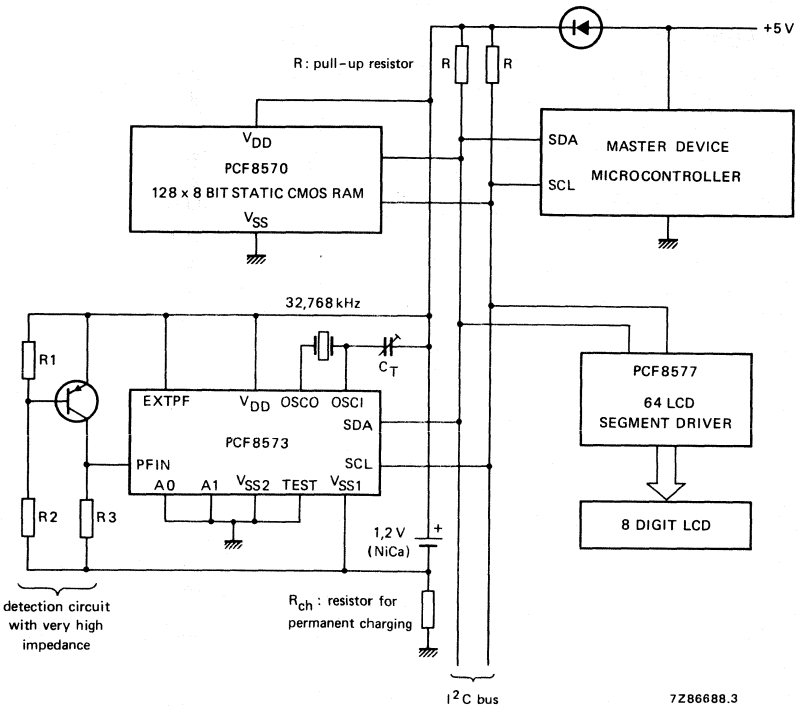


Fig. 13 Application example of the PCF8573 clock/calendar.

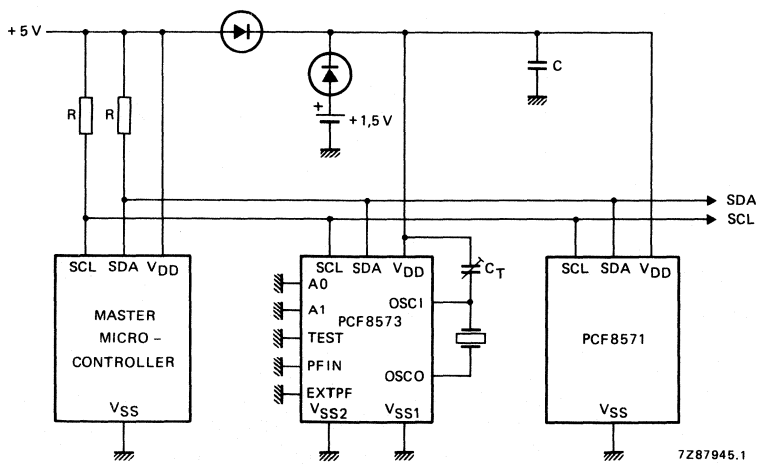


Fig. 14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O EXPANDER FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig. 10.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

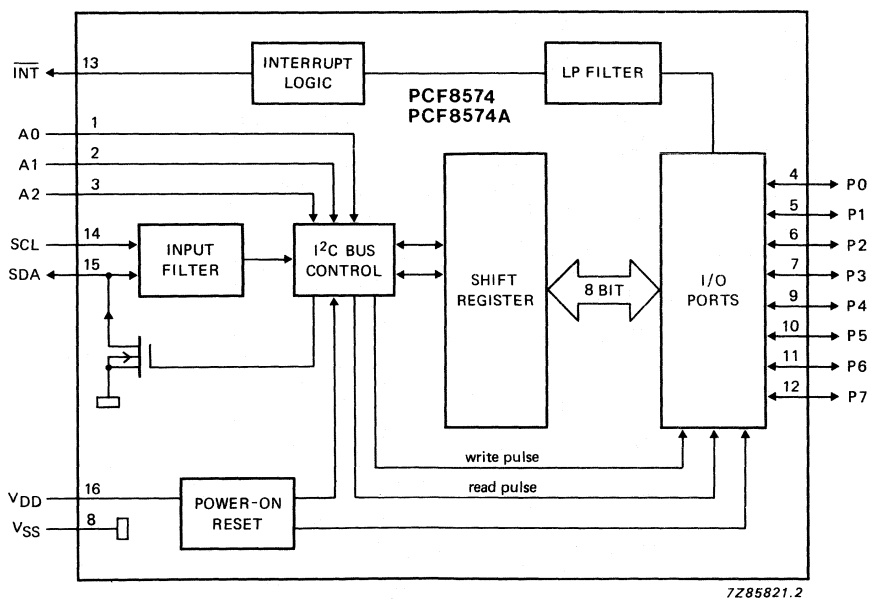


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

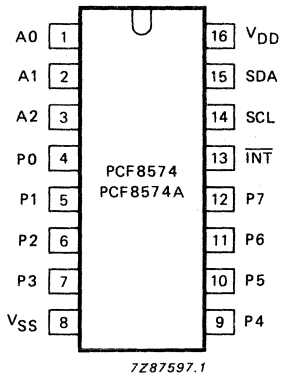


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

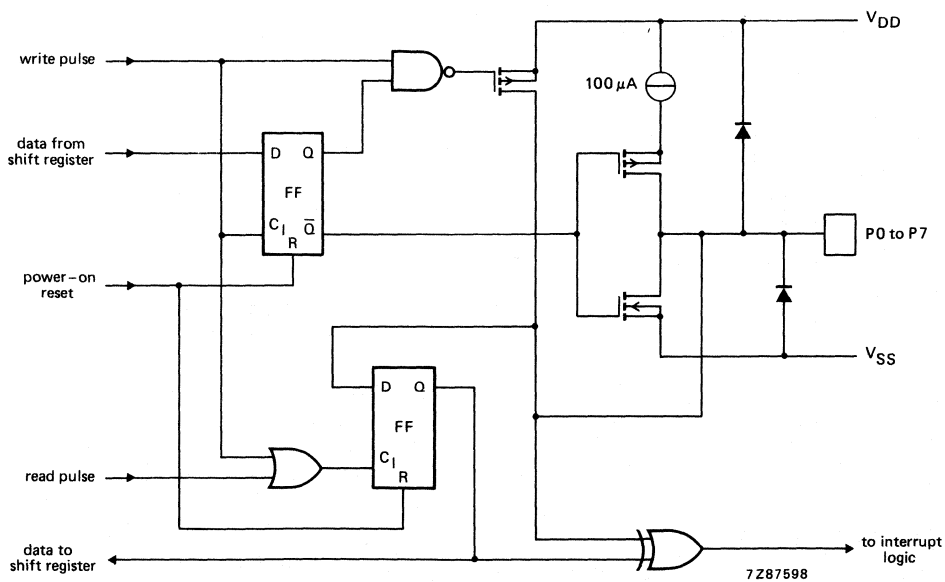


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

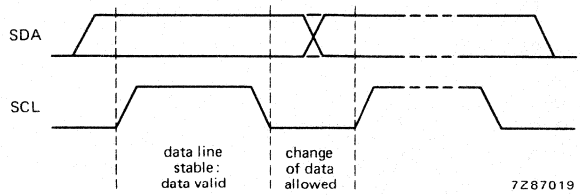


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

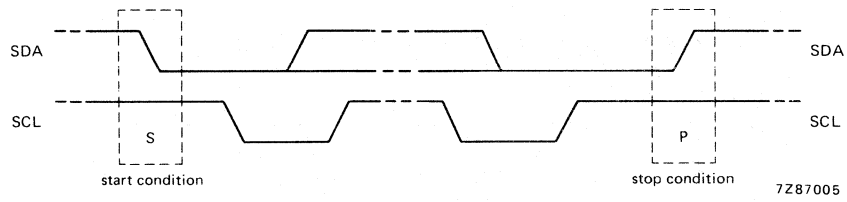


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

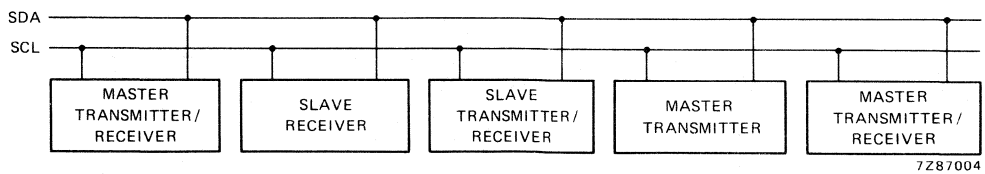


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

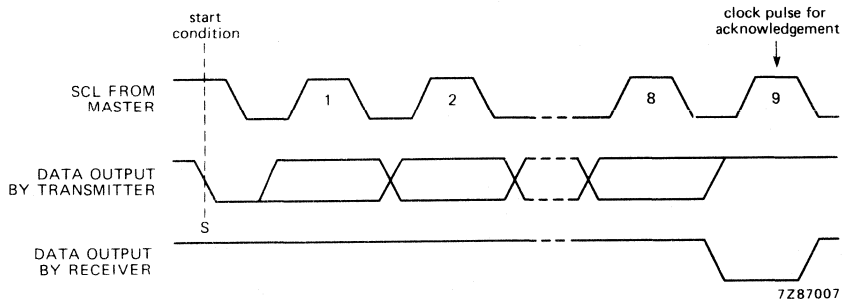


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

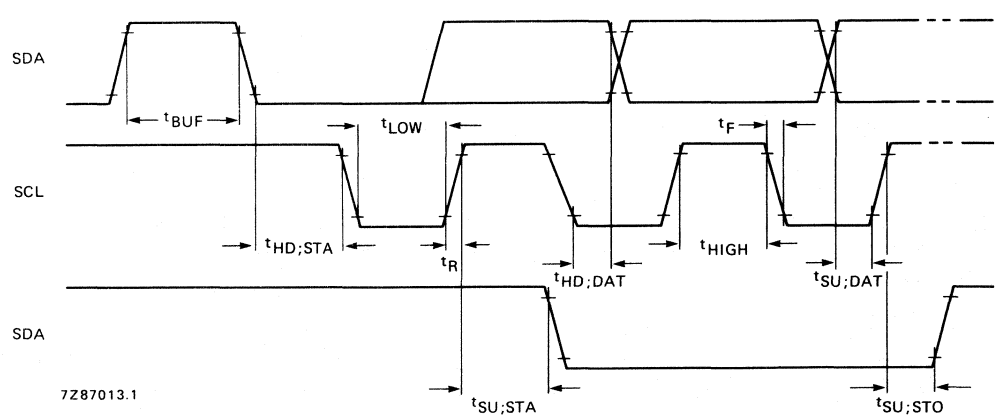


Fig. 8 I²C bus timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

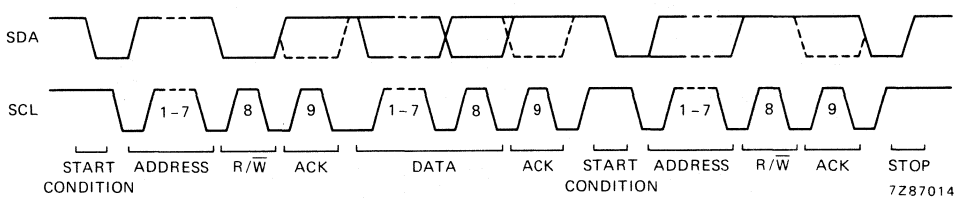


Fig. 9 Complete data transfer.

Where:

Clock t_{LOWmin} 4,7 μs

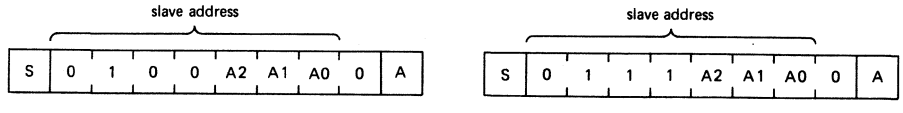
$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

FUNCTIONAL DESCRIPTION

Addressing (see Figs 10, 11 and 12)



(a) PCF8574. (b) PCF8574A.

Fig. 10 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

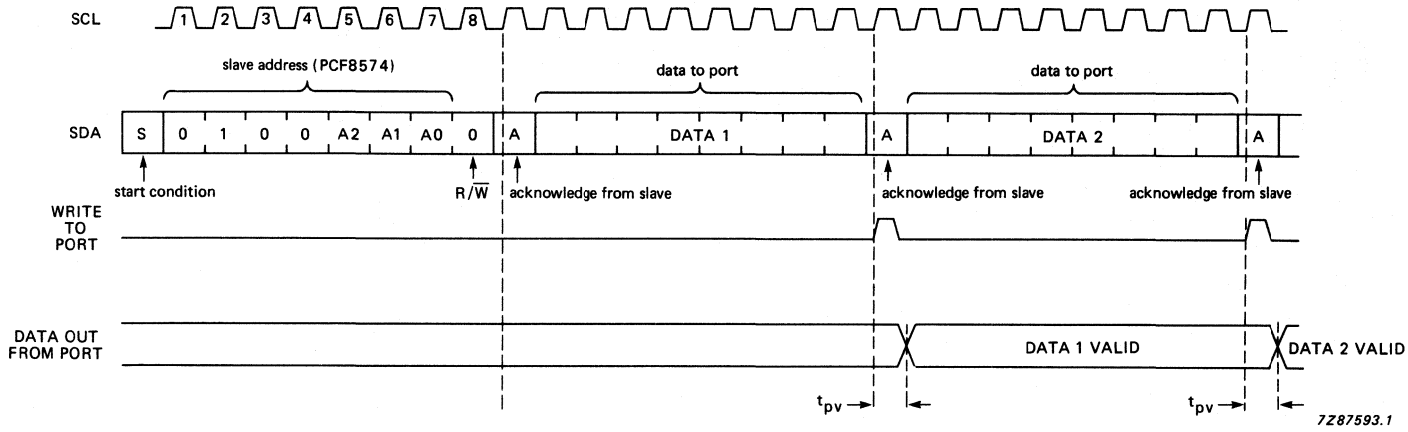


Fig. 11 WRITE mode (output port).

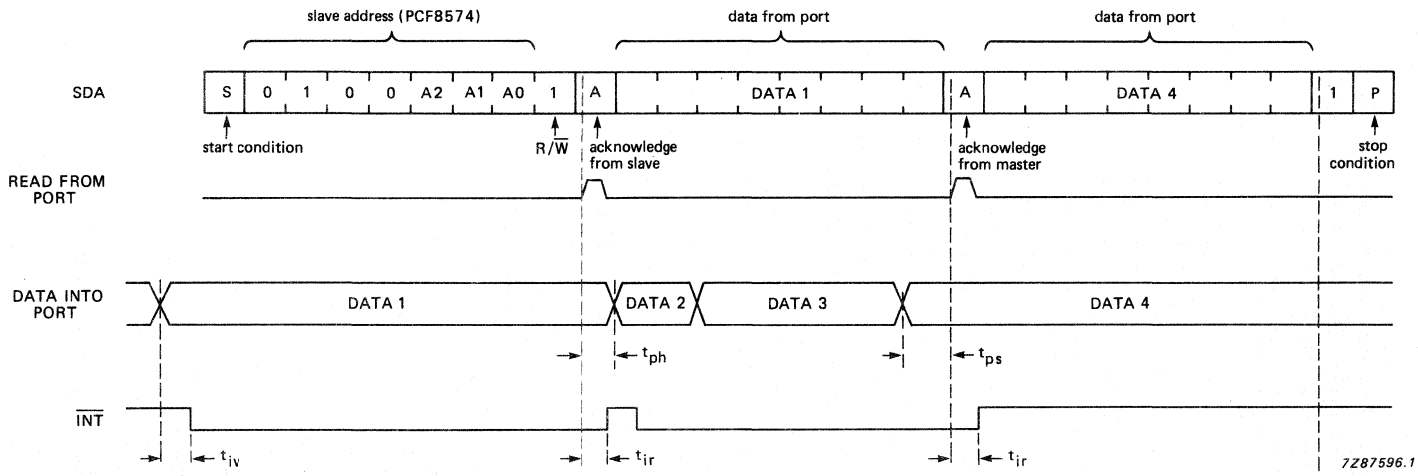


Fig. 12 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 13 and 14)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

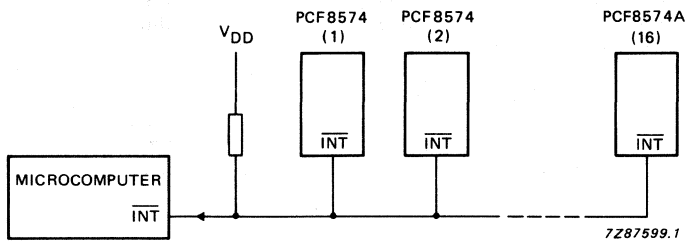


Fig. 13 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

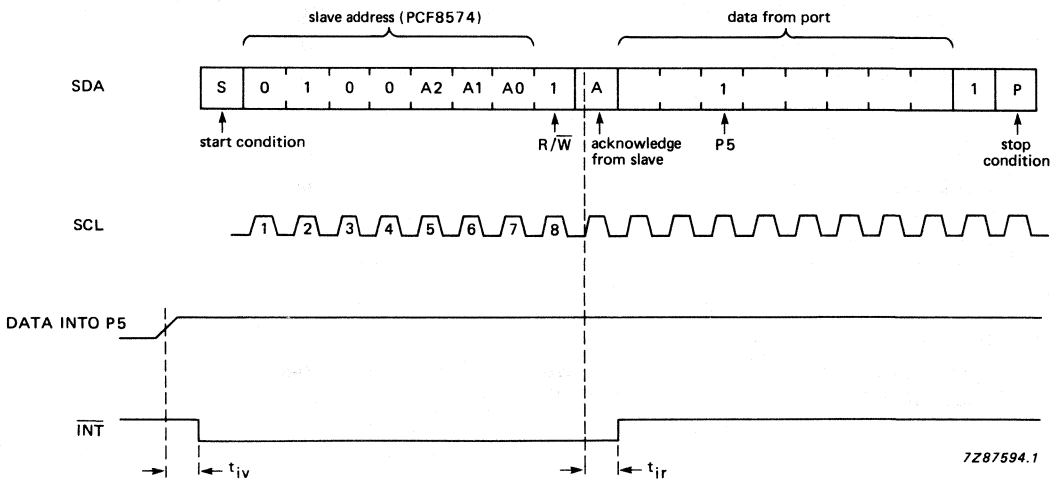


Fig. 14 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 15)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

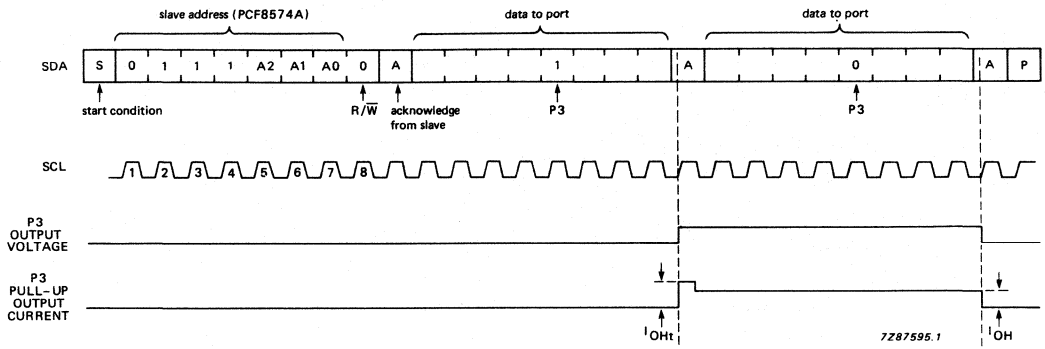


Fig. 15 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7 V
Input voltage range (any pin)	V_I	V_{SS}−0,5 to V_{DD} + 0,5	V
D.C. current into any input	$\pm I_I$	max.	20 mA
D.C. current into any output	$\pm I_O$	max.	25 mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100 mA
Total power dissipation	P_{tot}	max.	400 mW
Power dissipation per output	P_o	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	1	μA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at $V_{OH} = V_{SS}$ (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH during acknowledge (see Fig. 16)					
at $V_{OH} = V_{SS}$	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	1	μA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24 segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

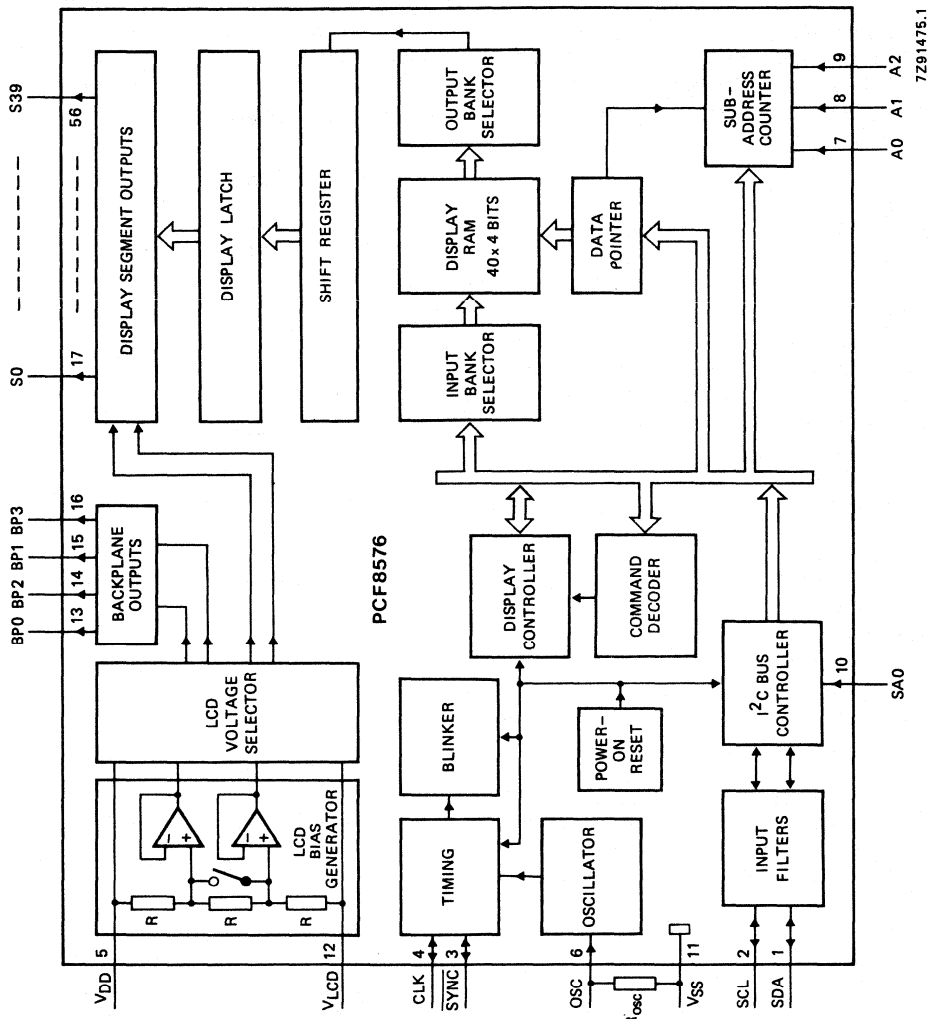


Fig. 1 Block diagram.

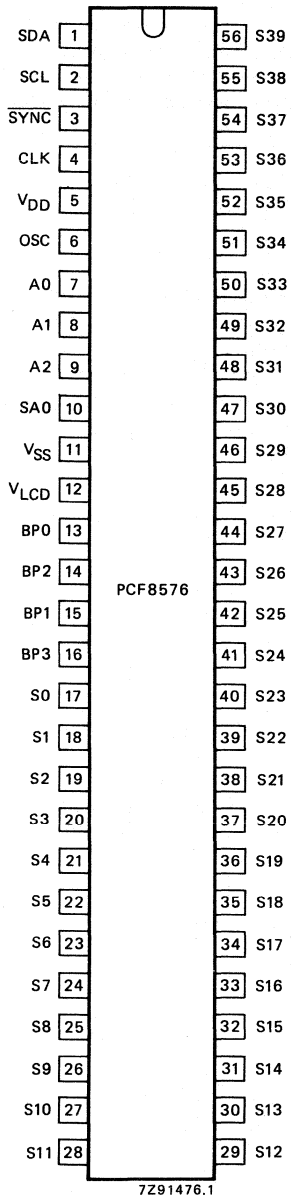


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropiate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

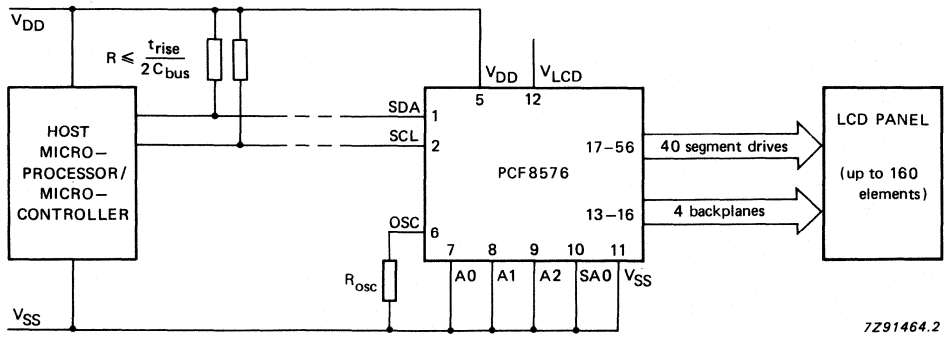


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\,V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

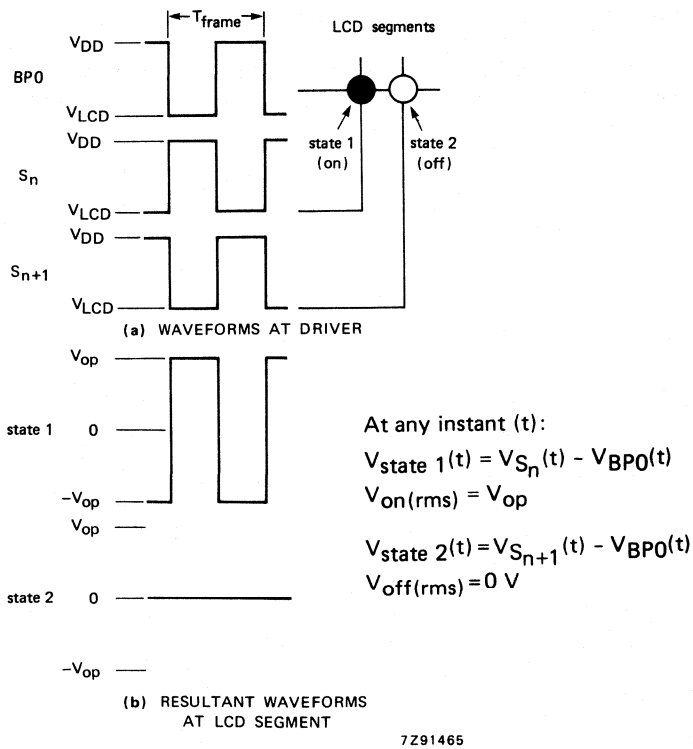


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

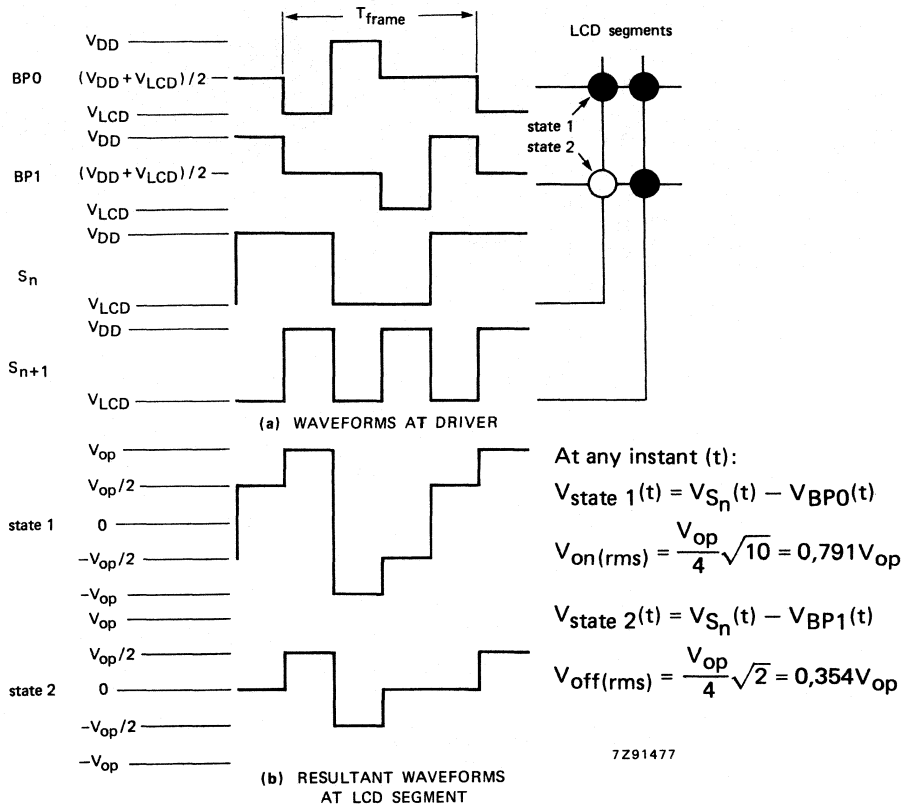


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

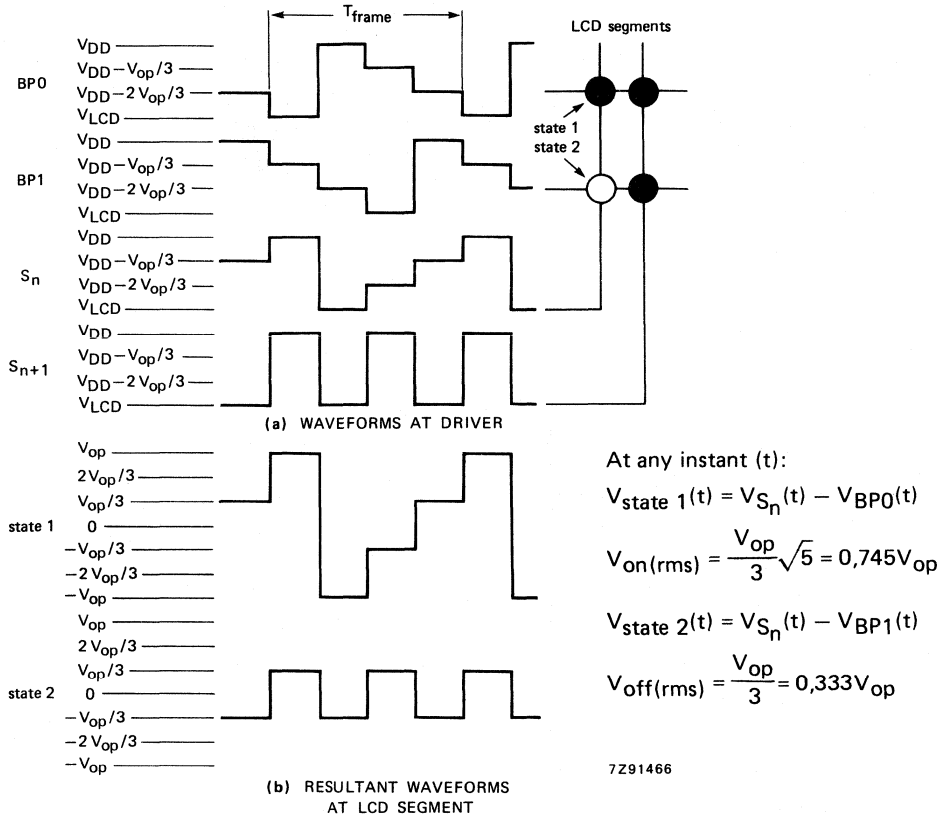


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

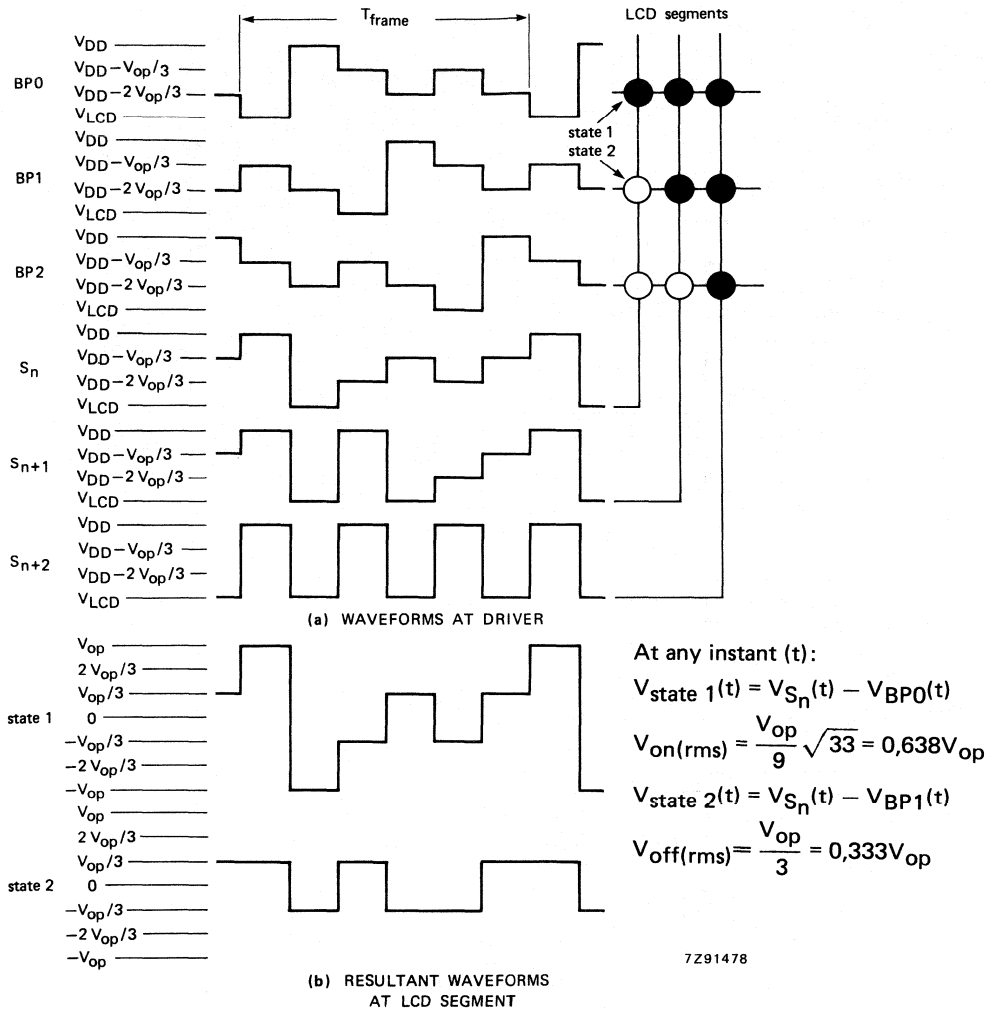


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

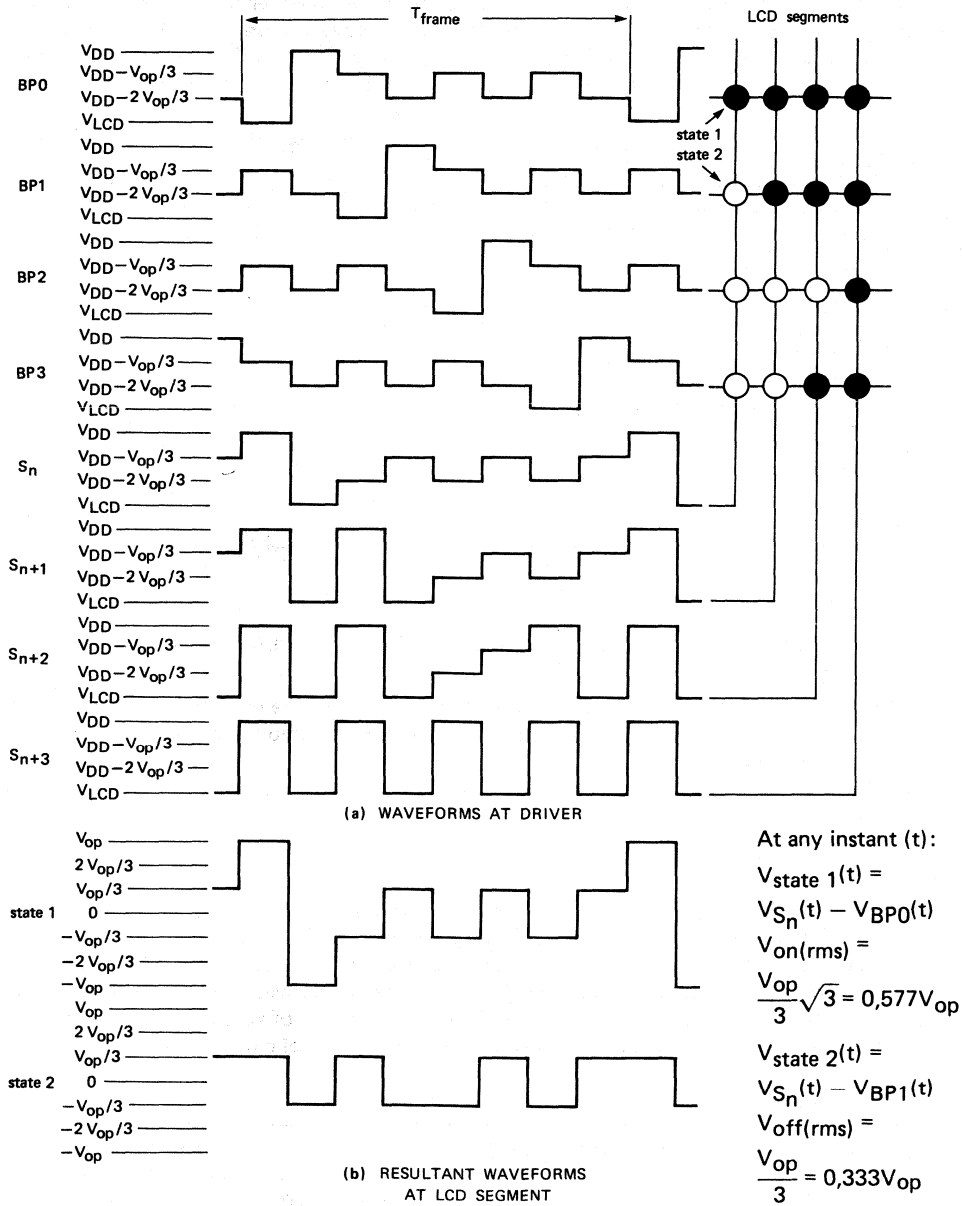


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

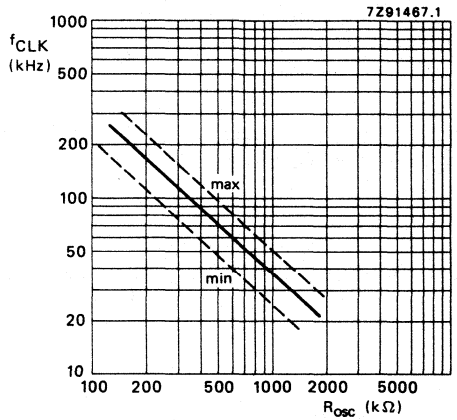


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed back-plane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multi-plex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

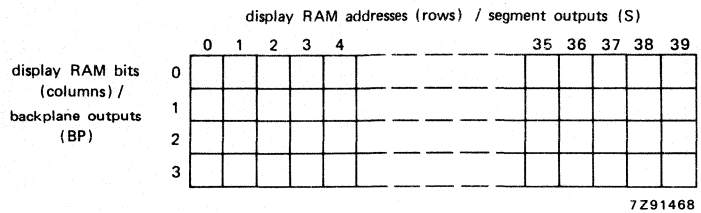


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

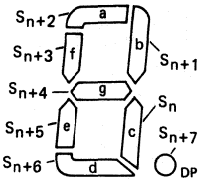
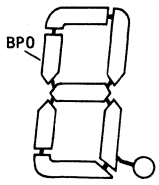
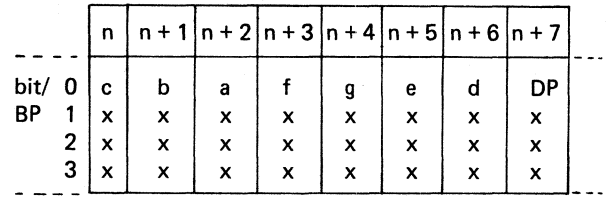
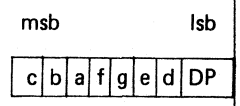
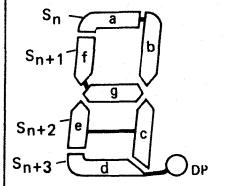
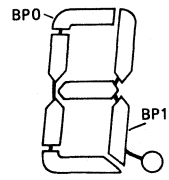
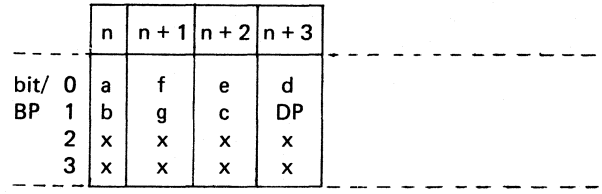
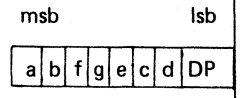
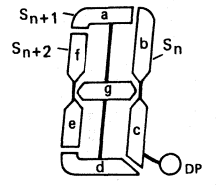
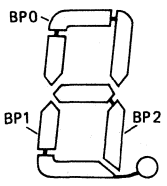
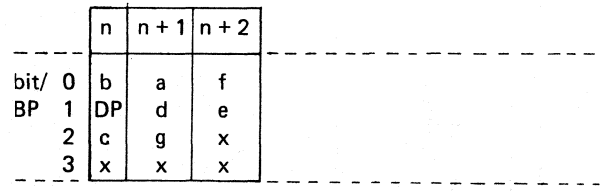
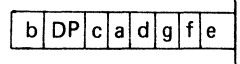
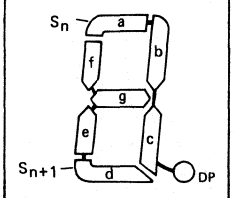
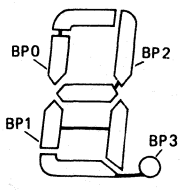
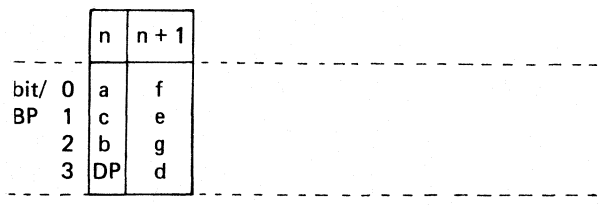
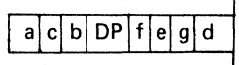
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

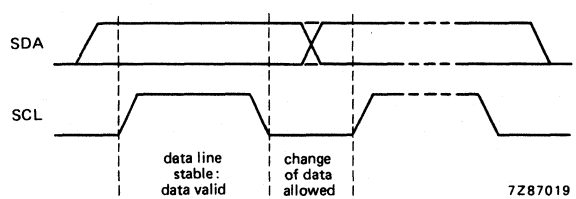


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

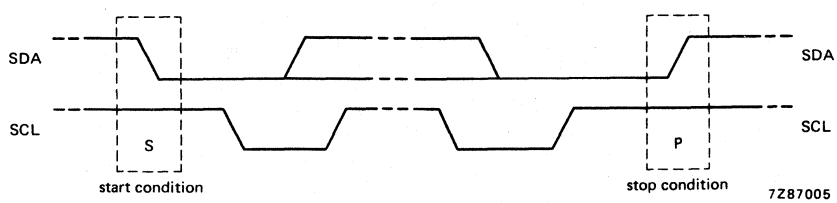


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

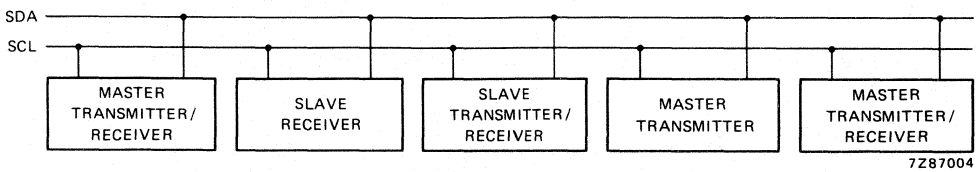


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

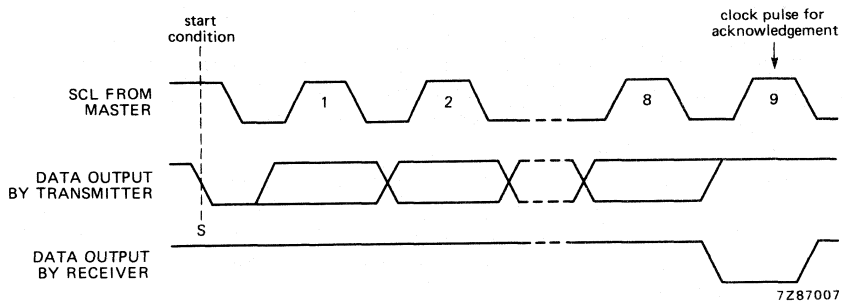


Fig. 15 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

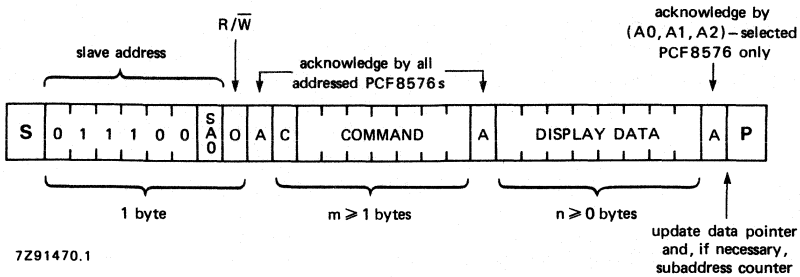


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

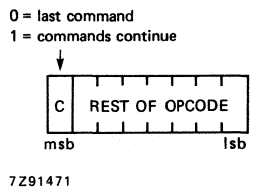


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table><table><tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table></td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td><table><tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr><tr><td>off</td><td>0</td><td>0</td></tr><tr><td>2 Hz</td><td>0</td><td>1</td></tr><tr><td>1 Hz</td><td>1</td><td>0</td></tr><tr><td>0,5 Hz</td><td>1</td><td>1</td></tr></table><table><tr><td>blink mode</td><td>bit A</td></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table></td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

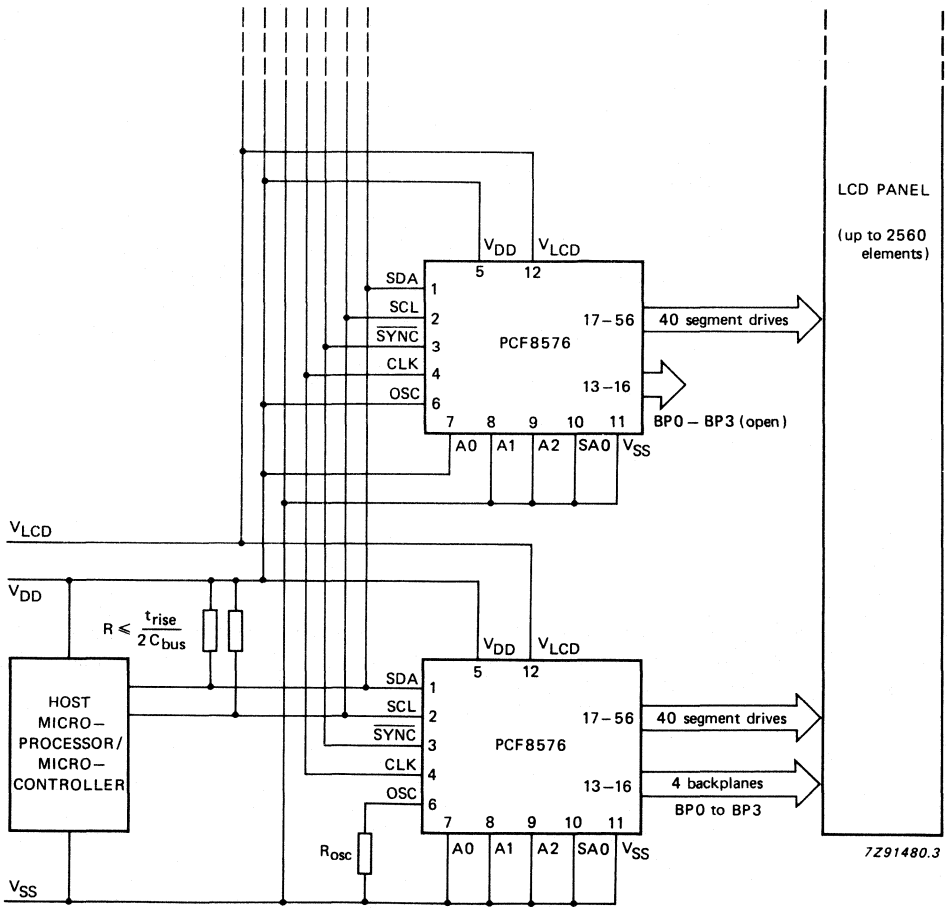
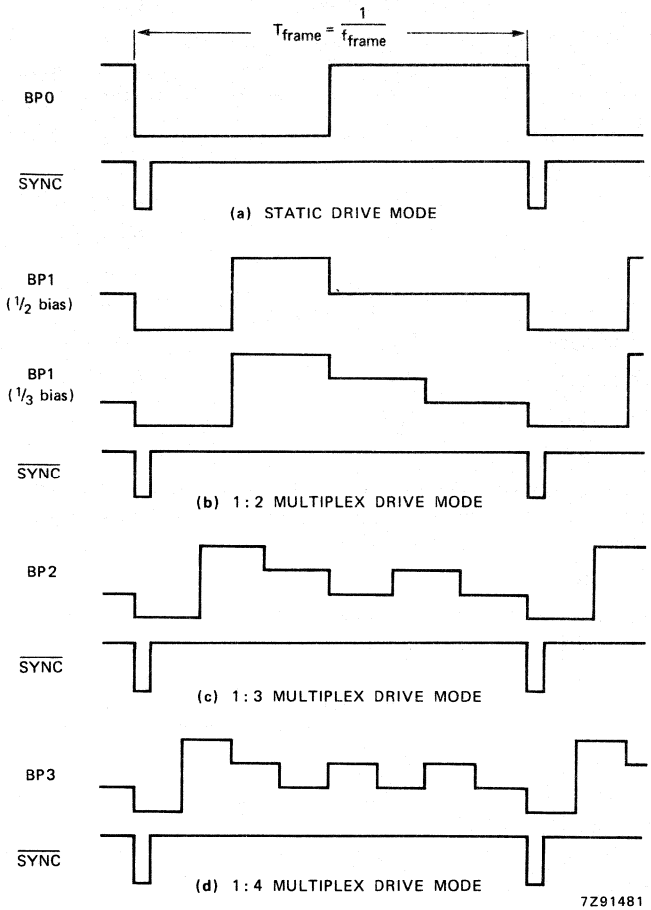


Fig. 18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

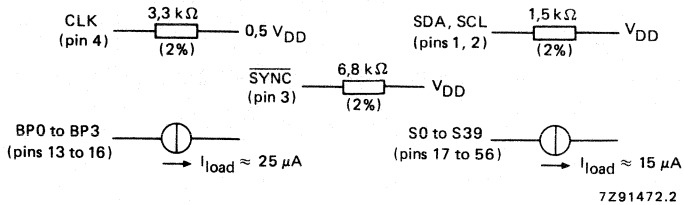


Fig. 20 Test loads.

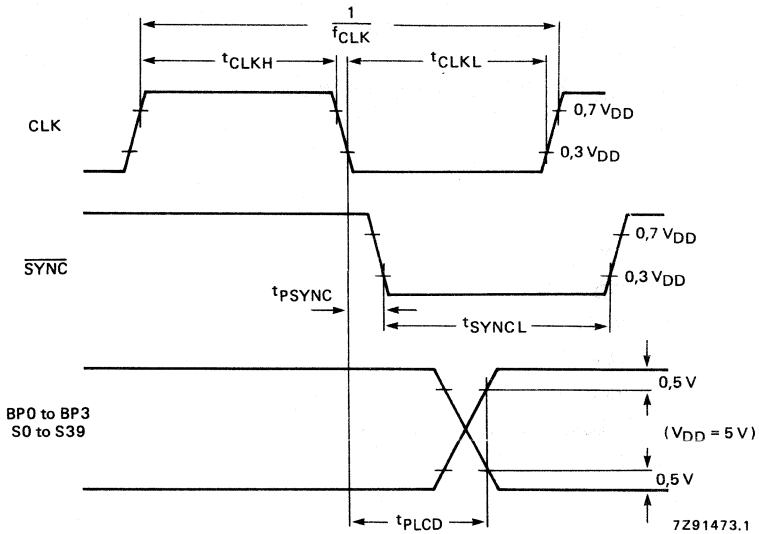


Fig. 21 Driver timing waveforms.

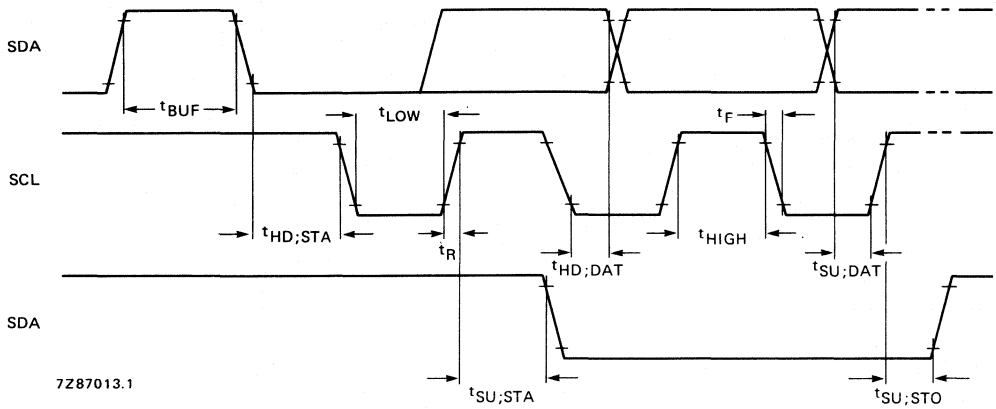
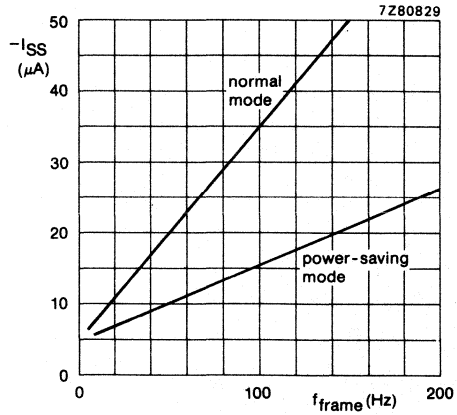
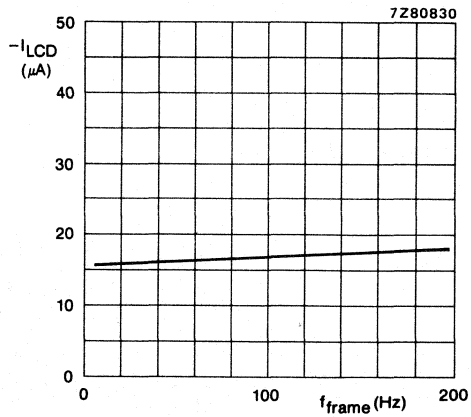


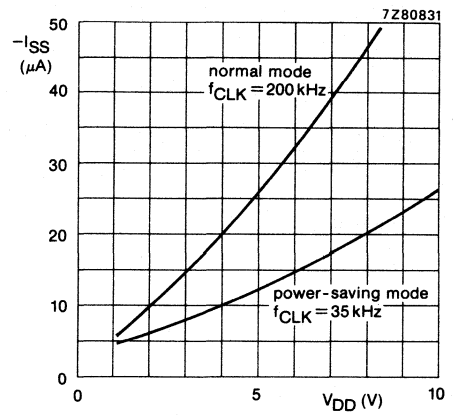
Fig. 22 I²C bus timing waveforms.



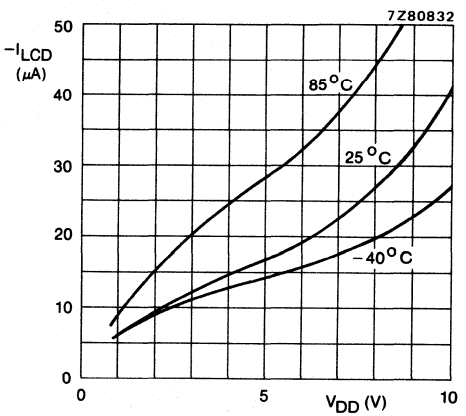
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

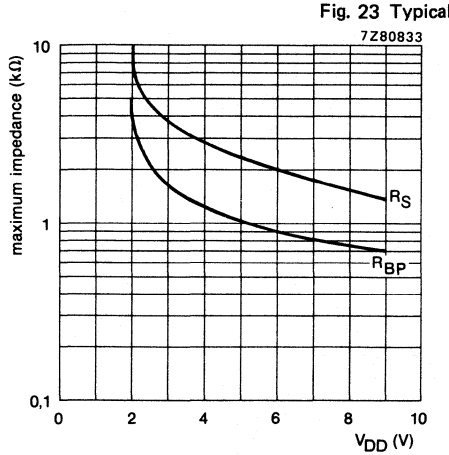


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

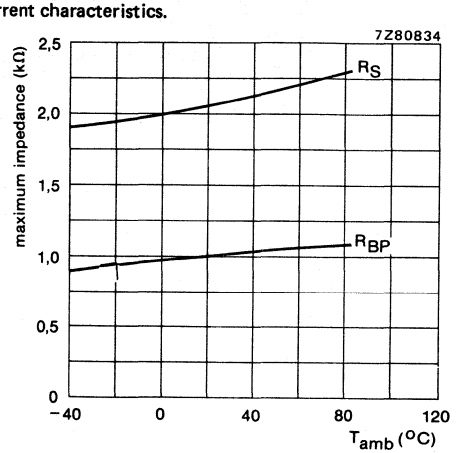


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

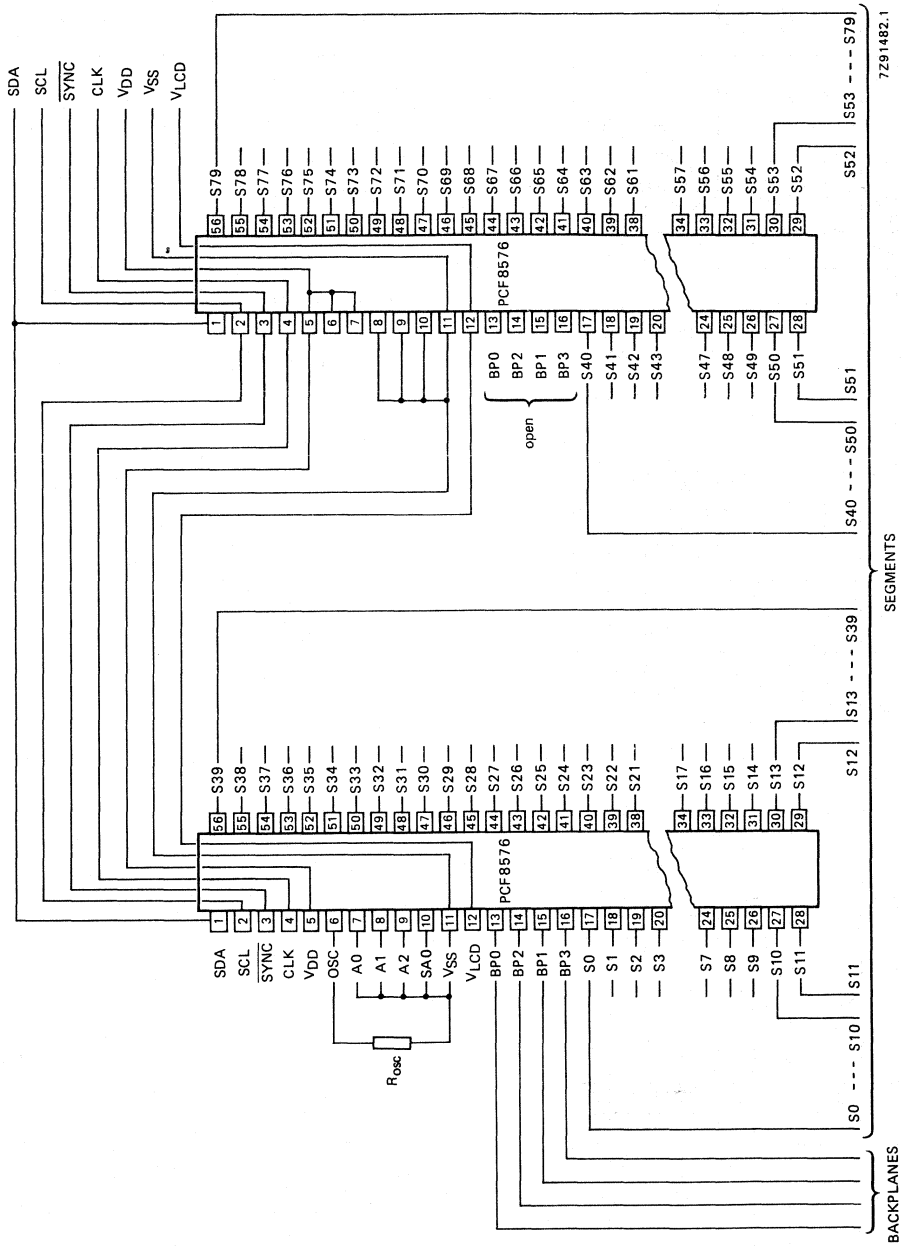


Fig. 25 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

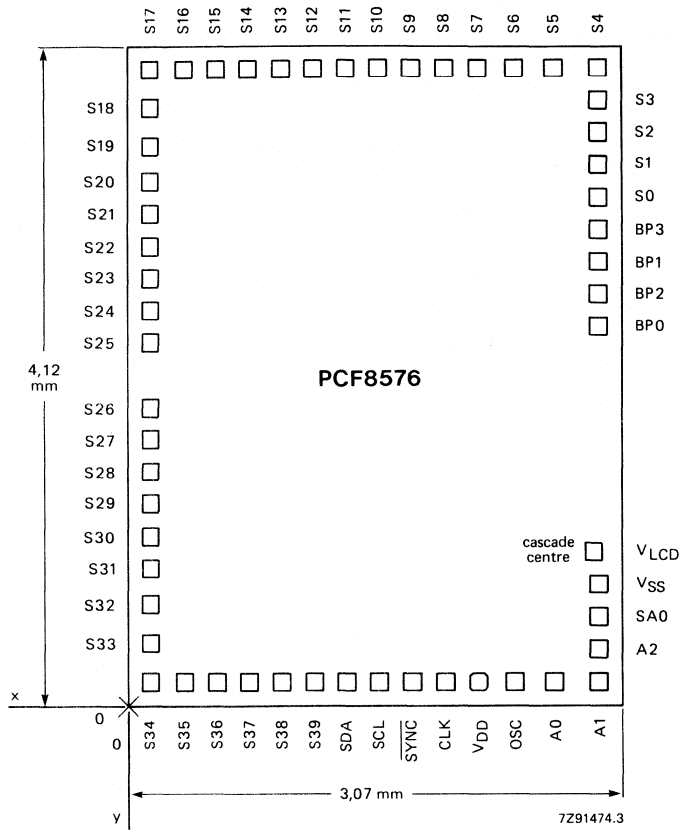


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380	↑	↑
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380	↑	↑
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32	↑	640	↑
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0	↕	560	↑
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2	↑	2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

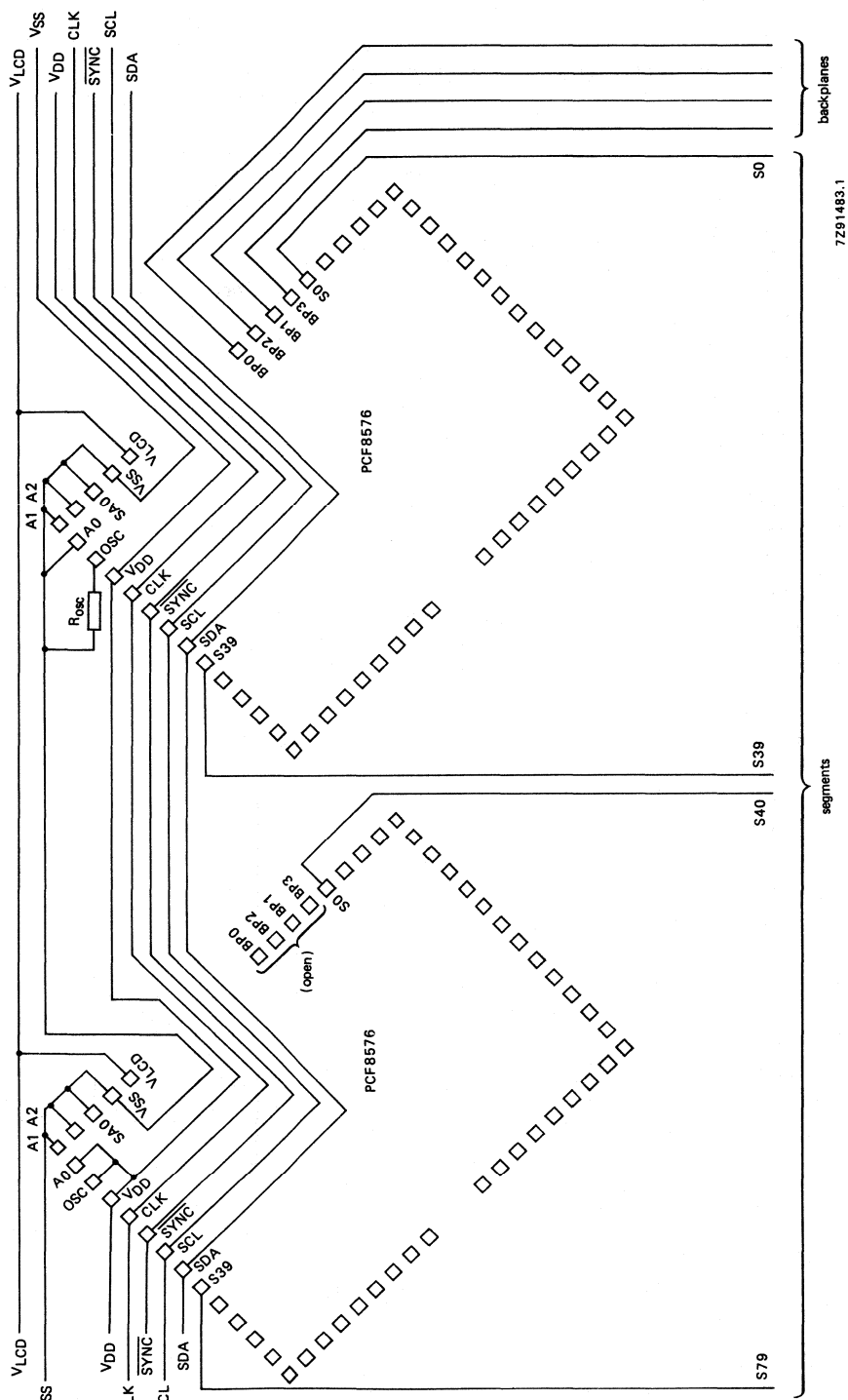


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

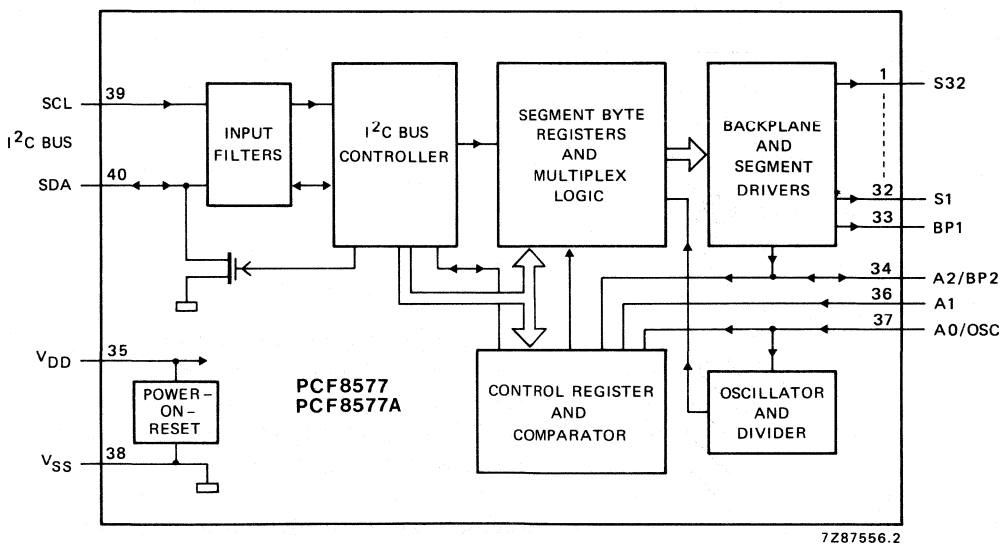


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO40; SOT158A).

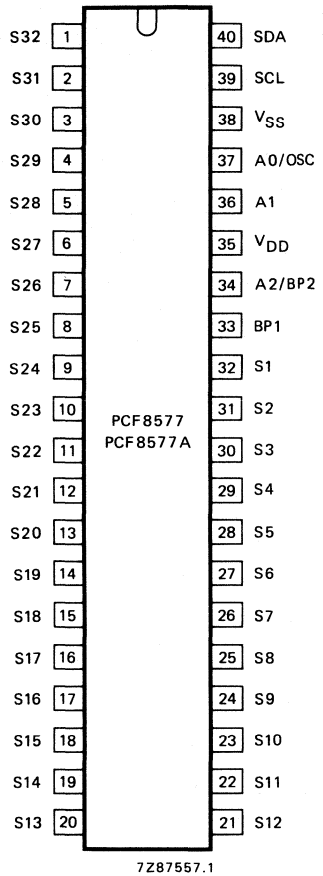


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

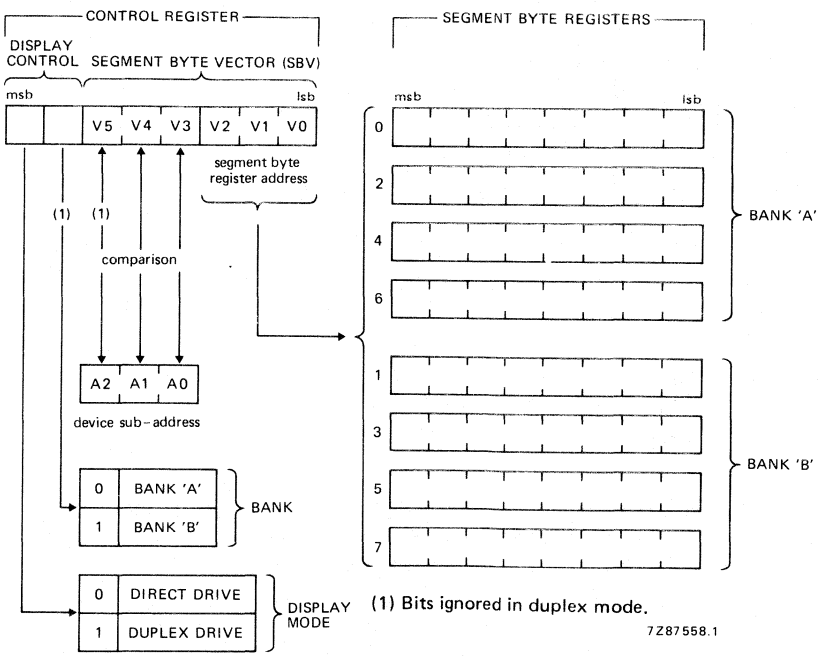


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.

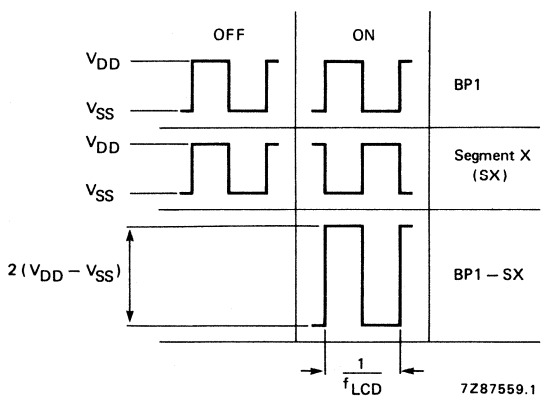


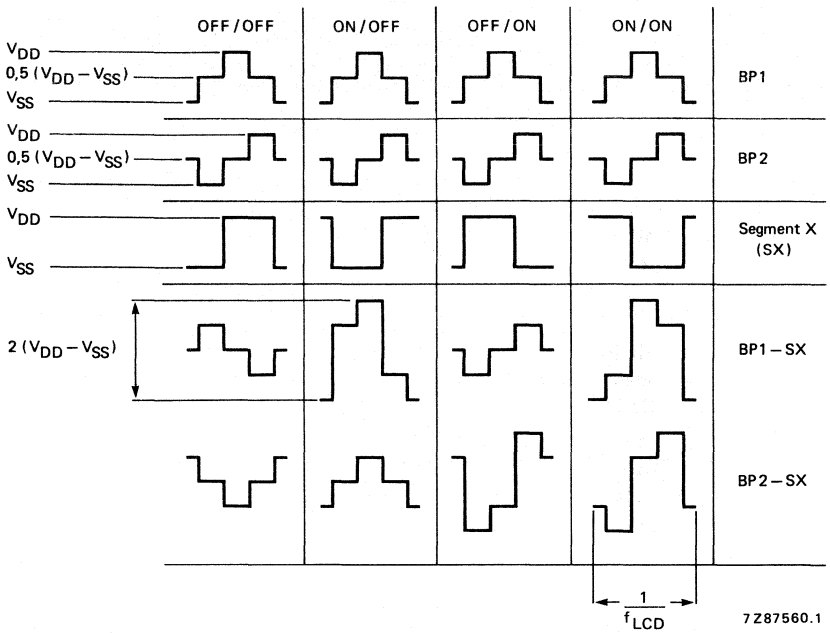
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2{,}26$

Fig. 5 Duplex mode display output waveforms.

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

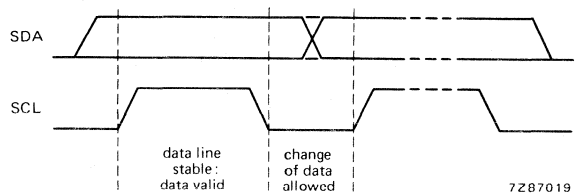


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

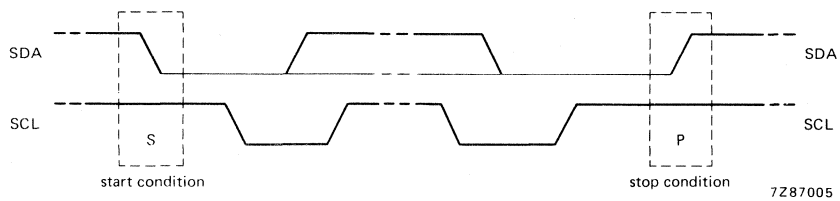


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

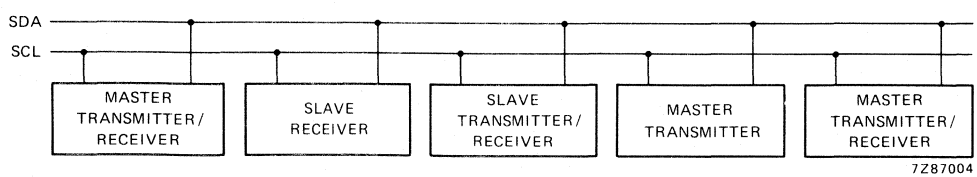


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

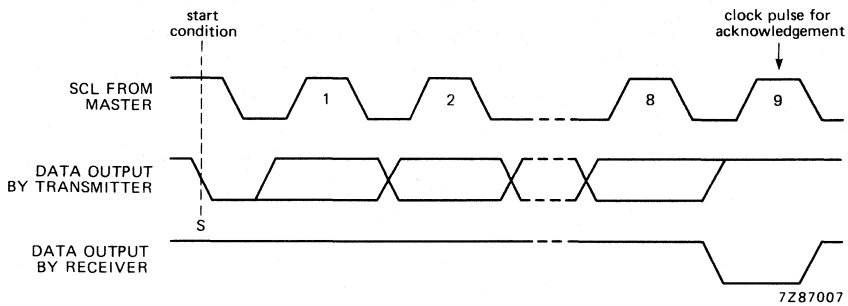


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

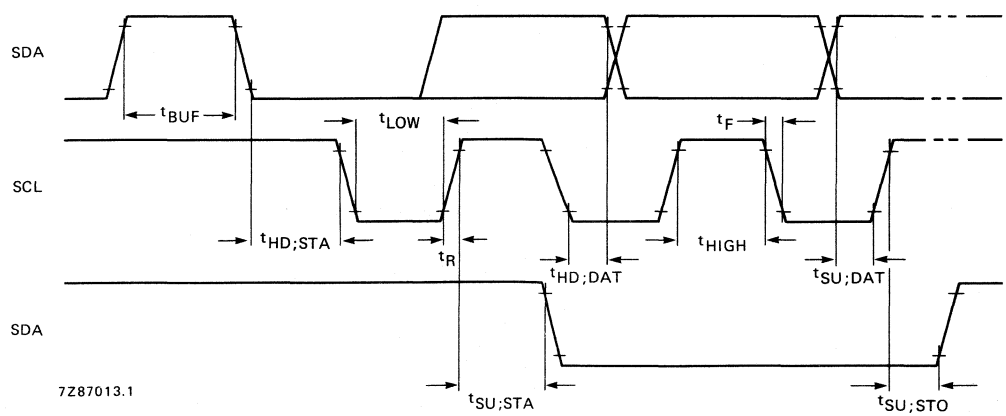


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

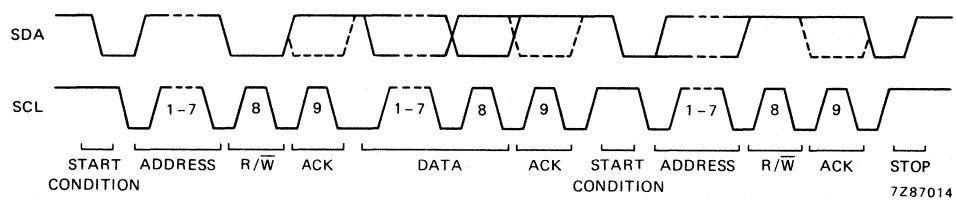


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

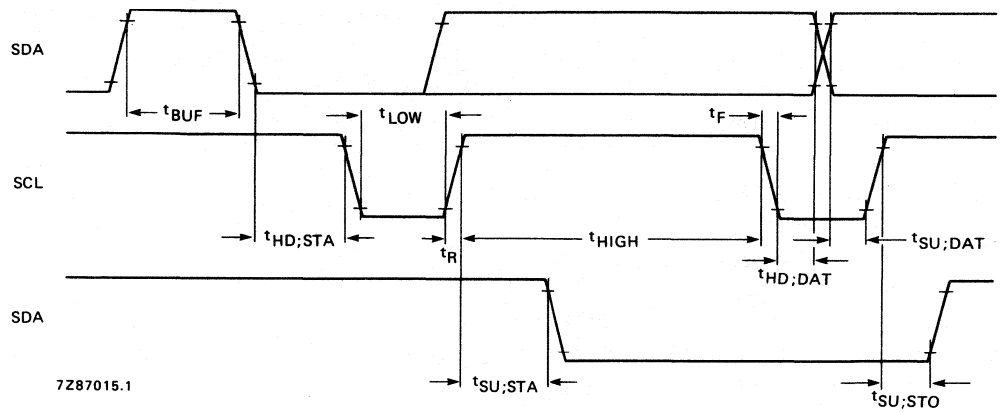


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

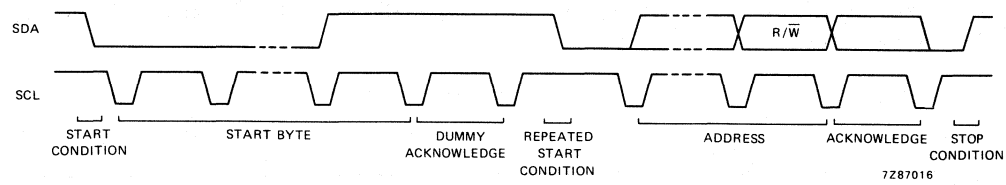


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

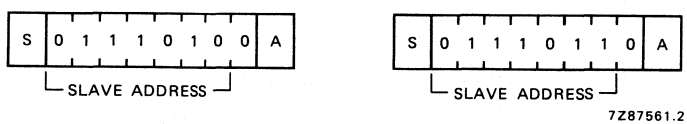
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave addresses for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577. (b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

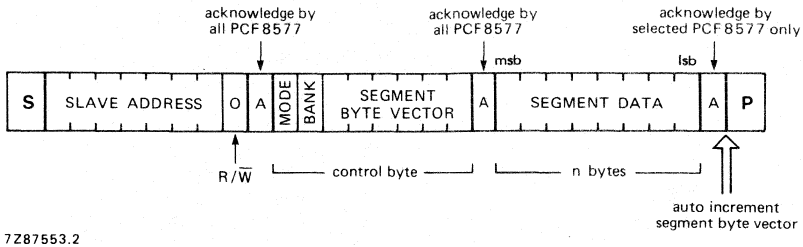


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	**BP1**
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	**BP2**
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	**BP1**
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	**BP2**
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	**BP1**
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	**BP2**
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	**BP1**
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	**BP2**

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

DEVELOPMENT DATA

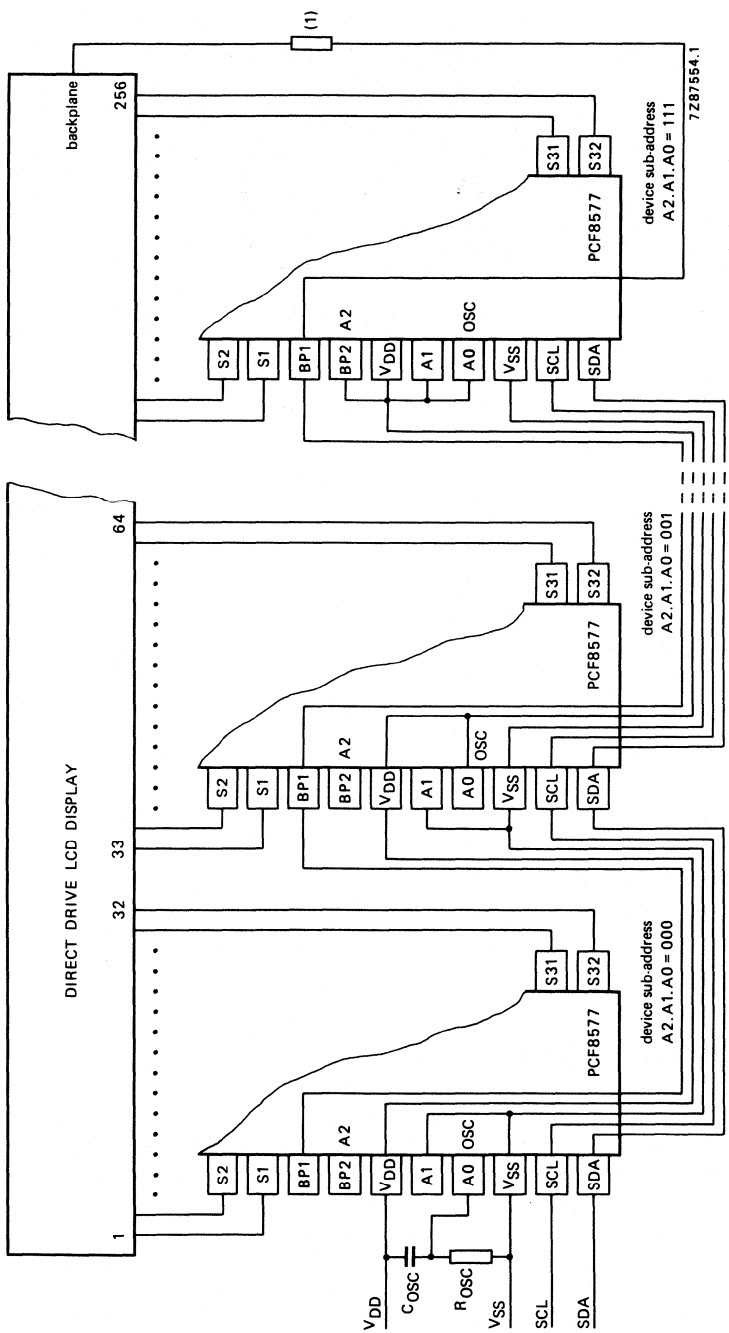
CHARACTERISTICS

V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	50	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at V_I = V_{SS}	C_I	–	–	7	pF
A1 input leakage current at V_I = V_{SS} or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at V_I = V_{DD}	I_I	–	2,0	–	μA
A0/OSC input current at V_I = V_{SS} or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current at V_{OH} = V_{DD} − 0,4 V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times (V_{BP} − V_{SX}) at maximum load	t_r, t_f	–	–	200	μs
Display frequency at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

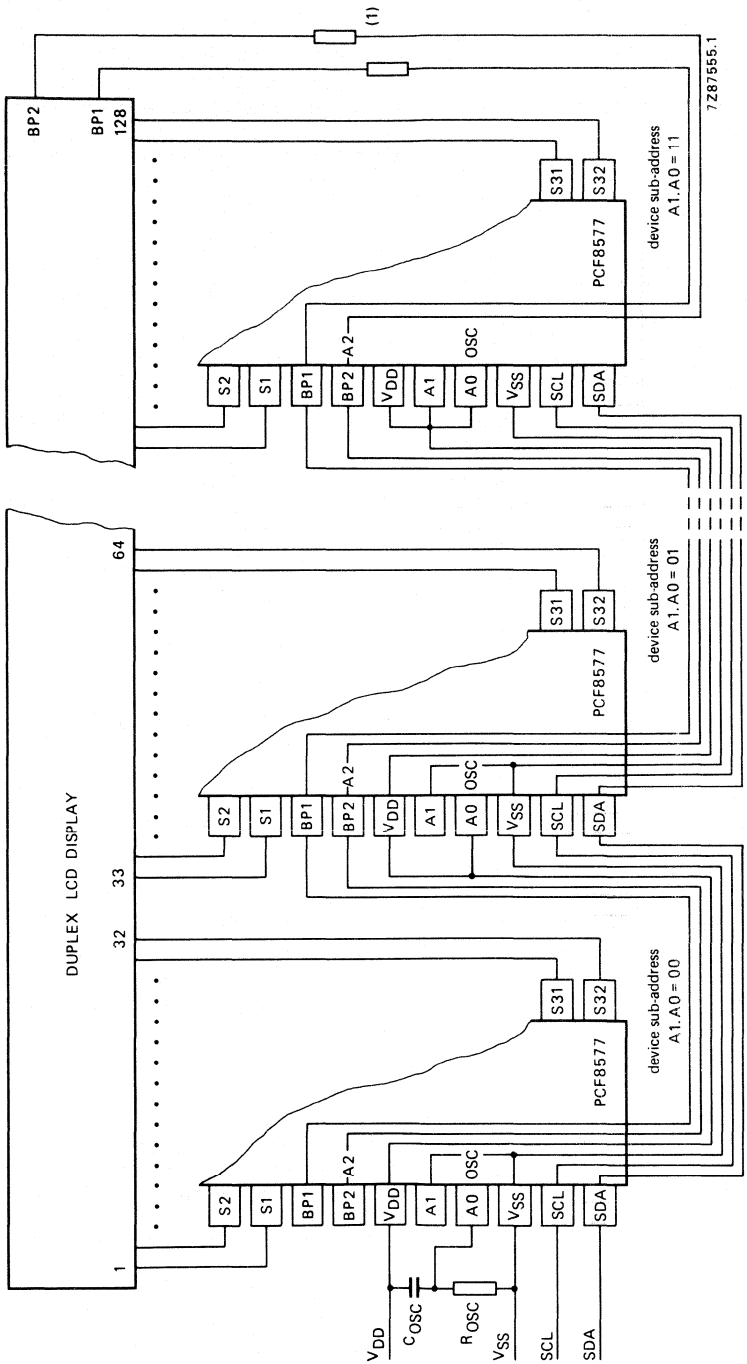
** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.



(1) The series resistance of the display backplane must be greater than 1 Ω.

Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.

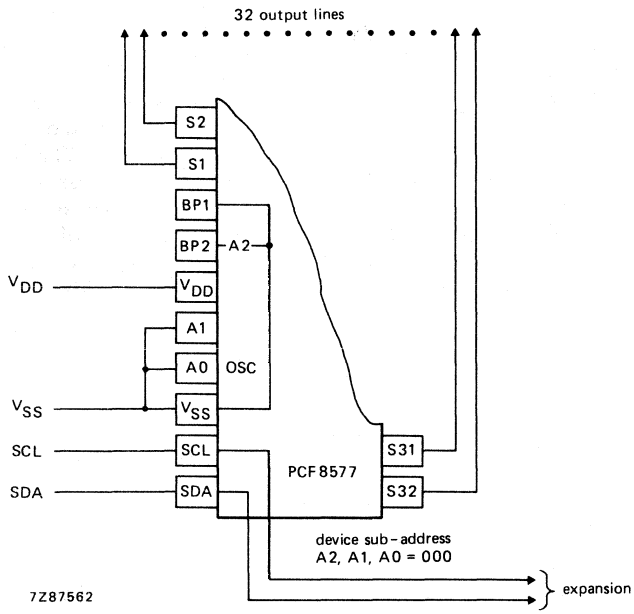
DEVELOPMENT DATA



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I²C bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or, for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots.
The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (possible 40,960 dots)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578U: uncased chip-in-tray.

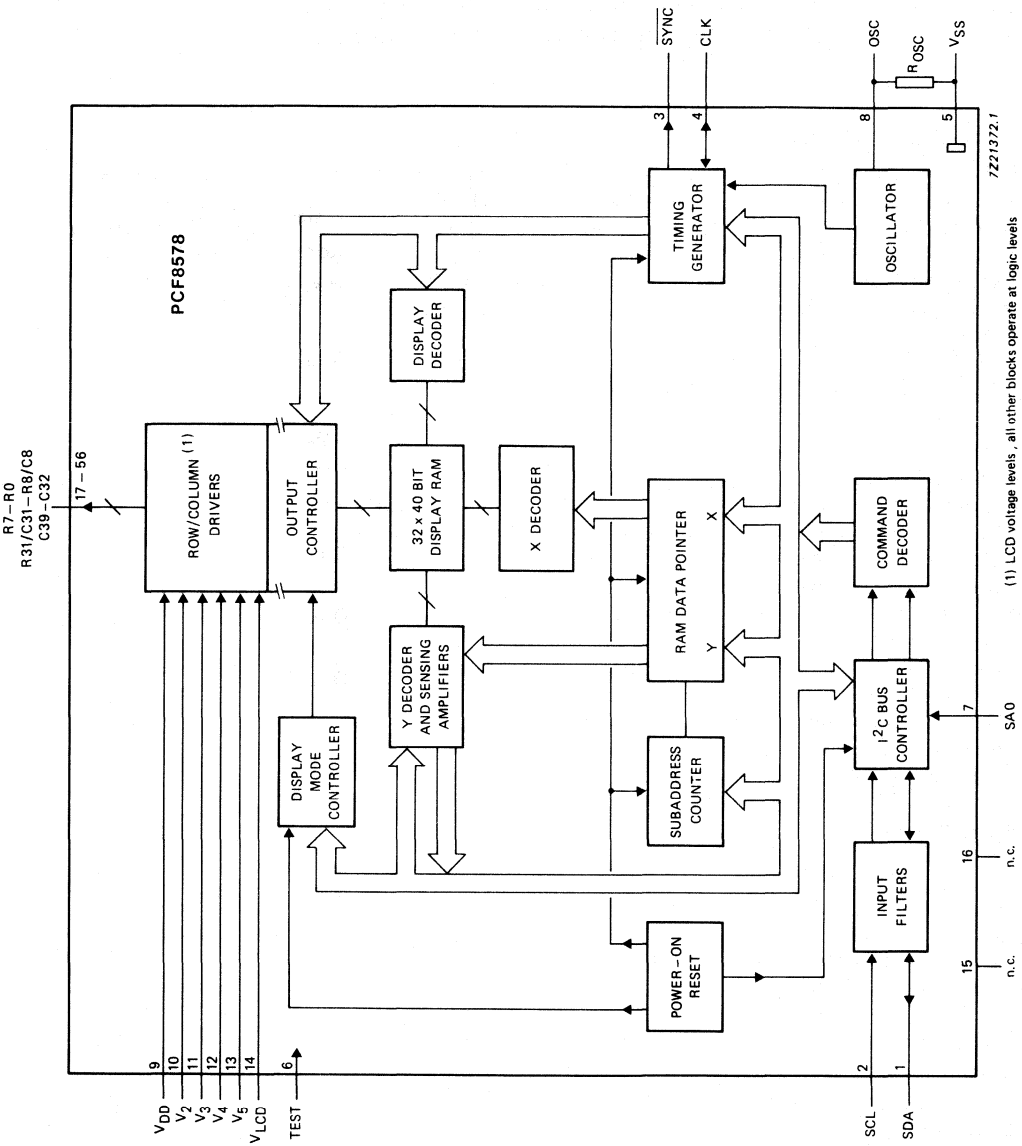


Fig. 1 Block diagram.

DEVELOPMENT DATA

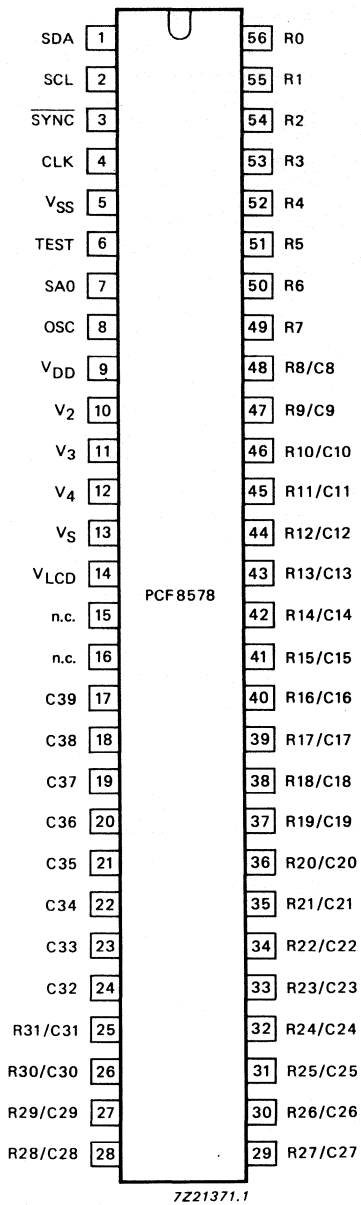


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output ⎫ I²C bus
2	SCL	Clock input ⎭
3	$\overline{\text{SYNC}}$	Cascade synchronization output
4	CLK	External clock input/output
5	V_{SS}	Ground (logic)
6	TEST	Test pin (connect to V_{SS})
7	SA0	I²C bus slave address input (bit 0)
8	OSC	Oscillator input
9	V_{DD}	Positive supply voltage
10	V_2	⎫ LCD bias voltage inputs
11	V_3	⎪
12	V_4	⎪
13	V_5	⎭
14	V_{LCD}	LCD supply voltage
15	n.c.	Not connected
16	n.c.	Not connected
17 to 24	C39 to C32	⎫ LCD column driver outputs ⎭
25 to 48	R31/C31 to R8/C8	⎫ LCD row/column driver outputs ⎭
49 to 56	R7 to R0	⎫ LCD row driver outputs ⎭

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications or for larger displays with up to 15 PCF8579s (31 when two slave addresses are used). See Table 1 for common display configurations.

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Common display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1 : 8	8	32	–	–	small digital or alphanumeric displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
with PCF8579	1 : 8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1 : 16	16	624	16 x 2	640	
	1 : 24	24	616	24	640	
	1 : 32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays bias sources with high driver capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig. 3 (a stand-alone system would be identical but without PCF8579).

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

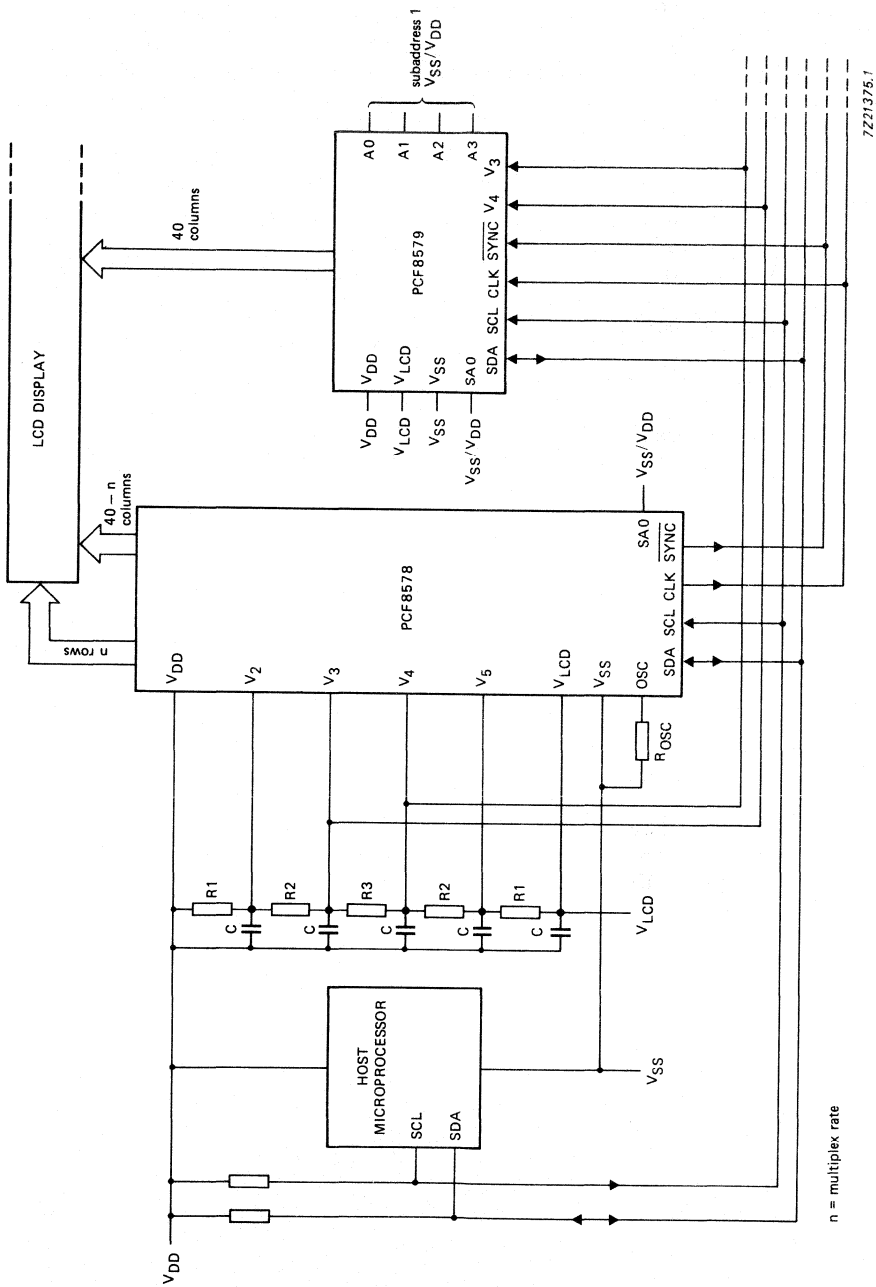


Fig. 3 Typical mixed mode configuration.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. The device is optimized for use with the PCF8578 LCD row/column driver. Up to 32 PCF8579s can be cascaded and used on the same I^2C bus (using the two slave addresses). Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579U: uncased chip-in-tray.

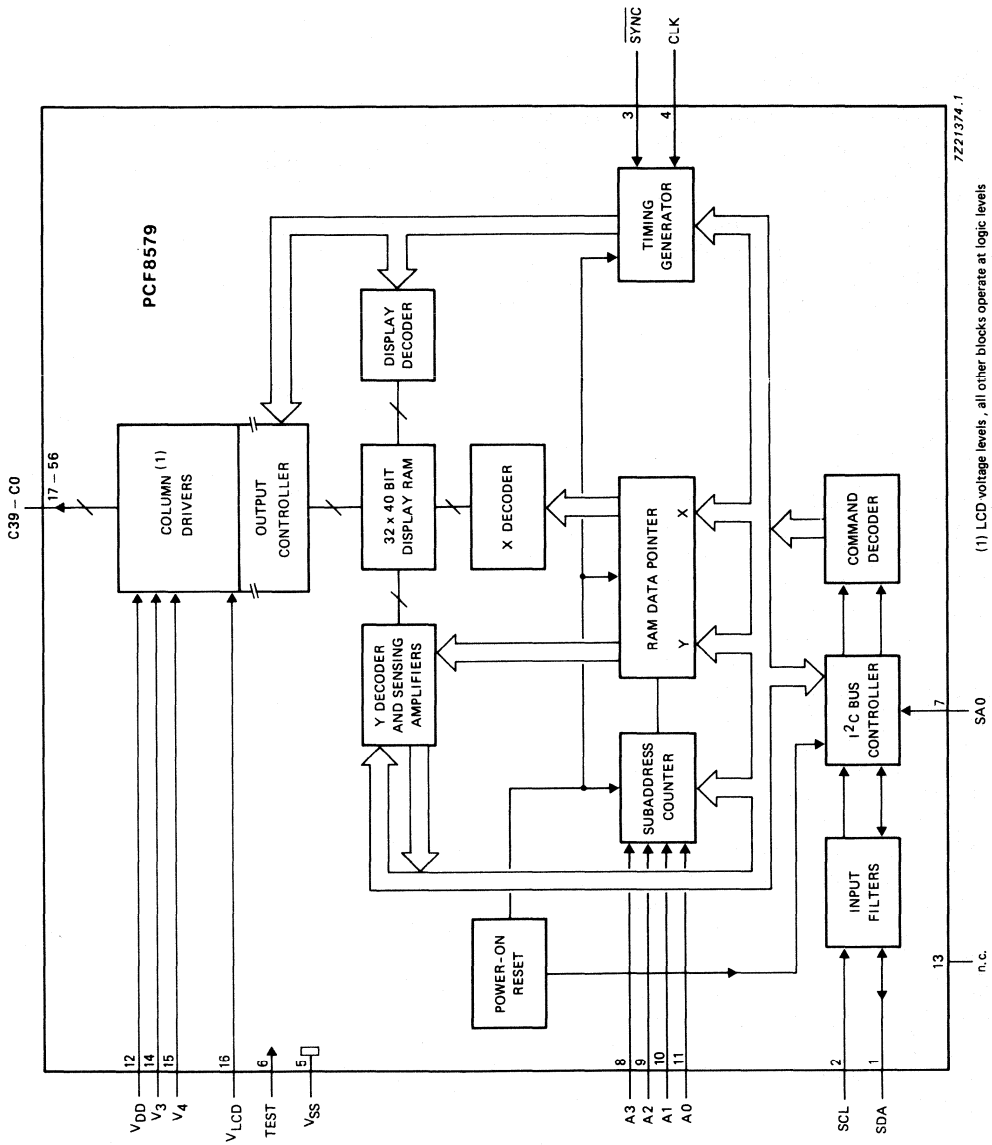


Fig. 1 Block diagram.

DEVELOPMENT DATA

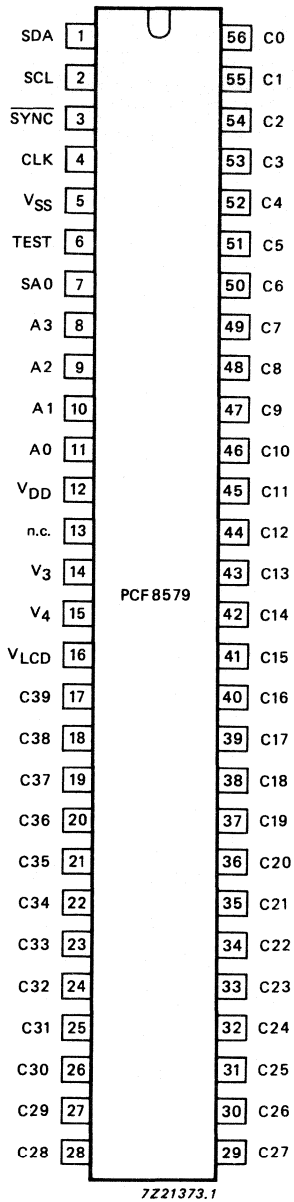


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output	I²C bus
2	SCL	Clock input	I²C bus
3	$\overline{SYNC}$	Cascade synchronization input	
4	CLK	External clock input	
5	V_{SS}	Ground (logic)	
6	TEST	Test pin (connect to V_{SS})	
7	SA0	I²C bus slave address input (bit 0)	
8	A3	I²C bus subaddress inputs	
9	A2	I²C bus subaddress inputs	
10	A1	I²C bus subaddress inputs	
11	A0	I²C bus subaddress inputs	
12	V_{DD}	Positive supply voltage	
13	n.c.	Not connected	
14	V_3	LCD bias voltage inputs	
15	V_4	LCD bias voltage inputs	
16	V_{LCD}	LCD supply voltage	
17 to 56	C39 to C0	LCD column driver outputs	

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

The PCF8578 typically operates with up to 16 PCF8579s. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s. This is achieved by setting the LSB of the I^2C bus slave address to 1 (V_{DD}) or 0 (V_{SS}) using input SA0.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. 1 : 32 multiplex rate
2. Display bank 0
3. Data pointer is set to X, Y address 0
4. Character mode
5. Subaddress counter is cleared
6. I^2C bus interface is initialized
7. Display blanked (by PCF8578)

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the threshold voltage (V_{th}). V_{th} is typically defined as the r.m.s. voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

multiplex rate	$\frac{V_1}{V_{op}}$	$\frac{V_2}{V_{op}}$	$\frac{V_3}{V_{op}}$	$\frac{V_4}{V_{op}}$	$\frac{V_{off}}{V_{op}}$	$\frac{V_{on}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	$\frac{V_{op}}{V_{th}}$
1 : 8	0,739	0,522	0,478	0,261	0,297	0,430	1,477	3,37
1 : 16	0,800	0,600	0,400	0,200	0,245	0,316	1,291	4,08
1 : 24	0,830	0,661	0,339	0,170	0,214	0,263	1,230	4,68
1 : 32	0,850	0,700	0,300	0,150	0,193	0,230	1,196	5,19

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leq 9$	$n \geq 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

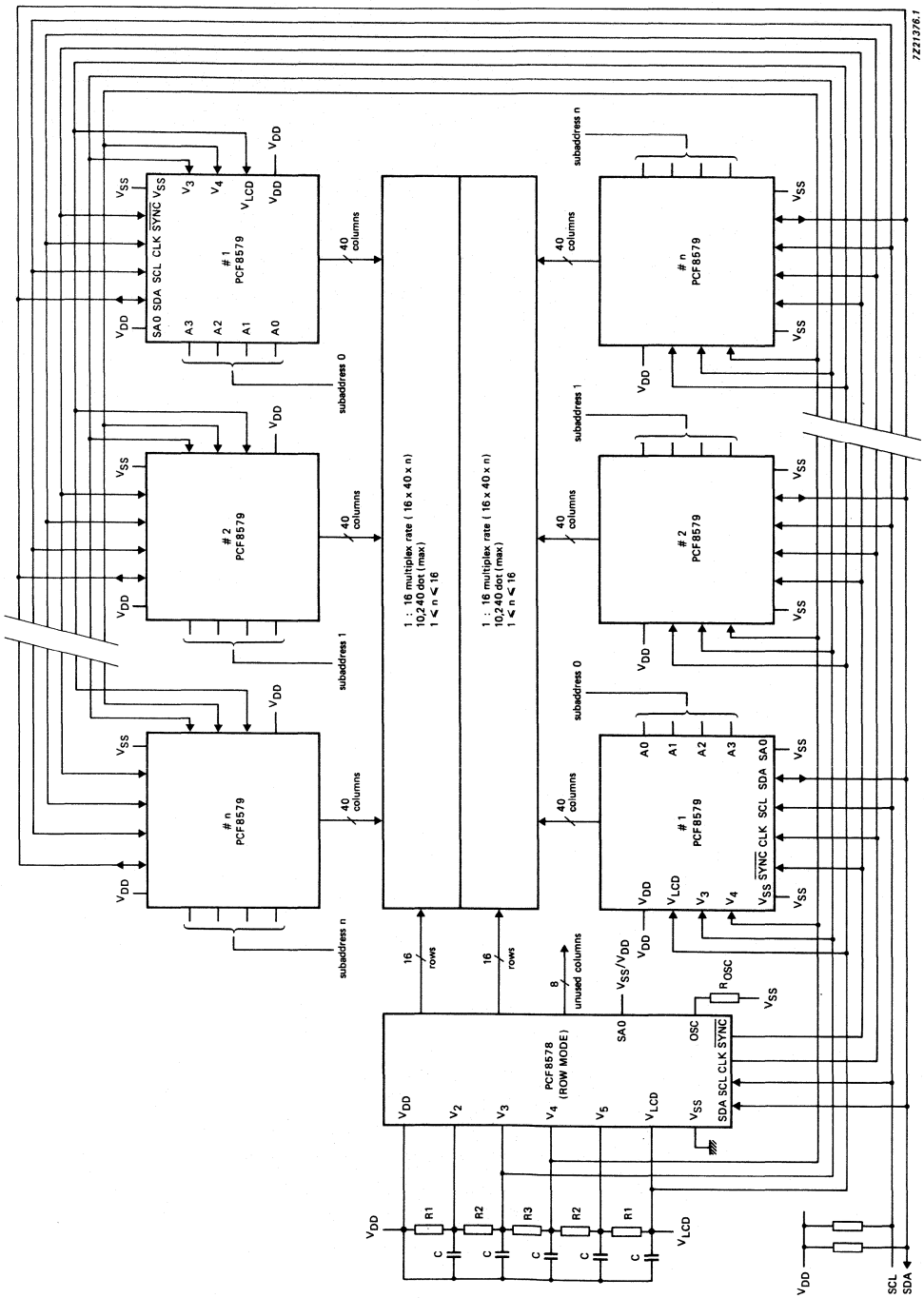


Fig. 3 Example of split screen application with 1 : 16 multiplex rate for improved contrast.

256 × 8-bit STATIC CMOS EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator. If the latter is used an RC time constant must be connected to pin 7 or 13.

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

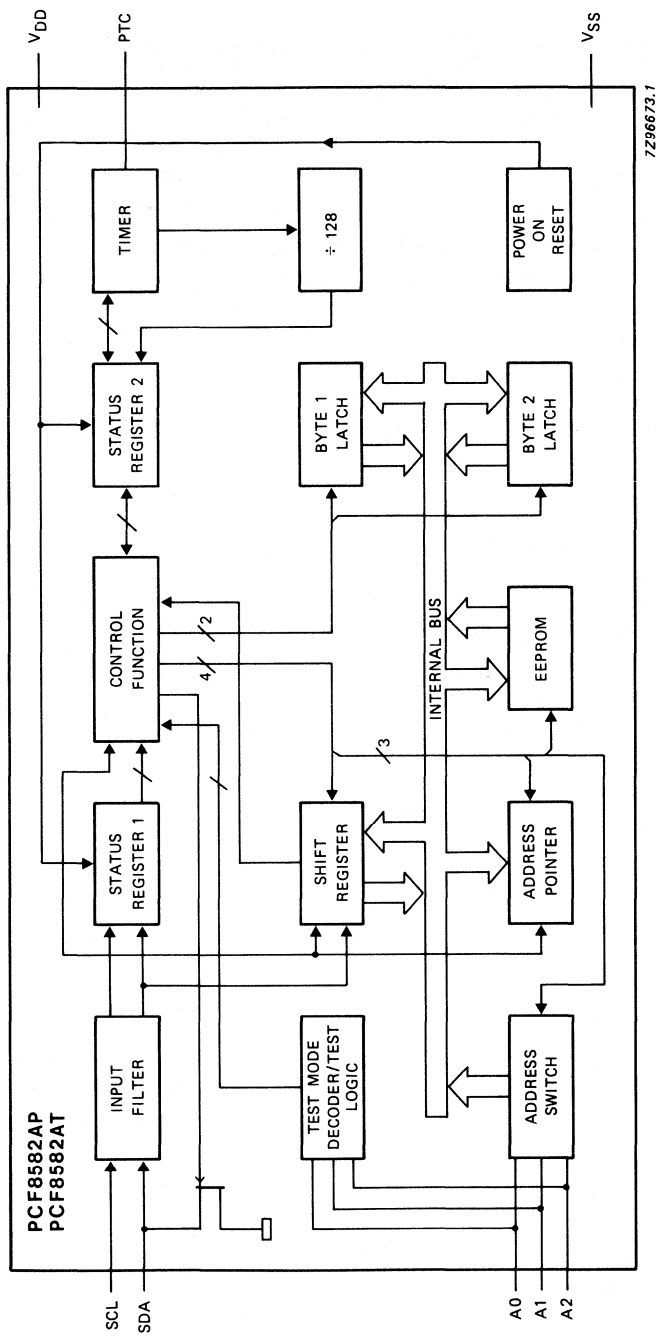
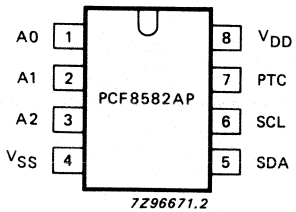
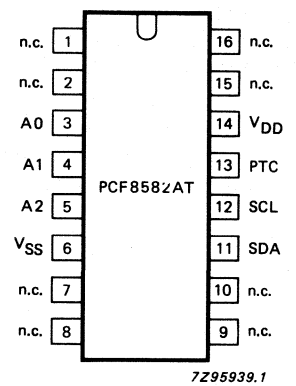


Fig. 1 Block diagram.



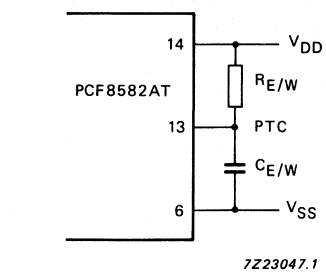
1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^2C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

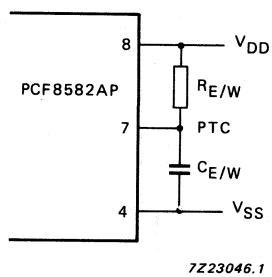
Fig. 2 (a) Pinning diagram.



1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^2C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.





Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW,
while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

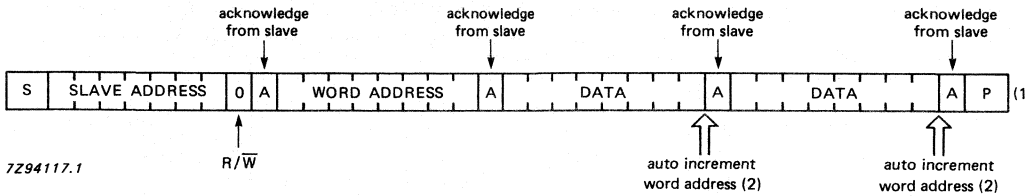
Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I²C-bus are available on request.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

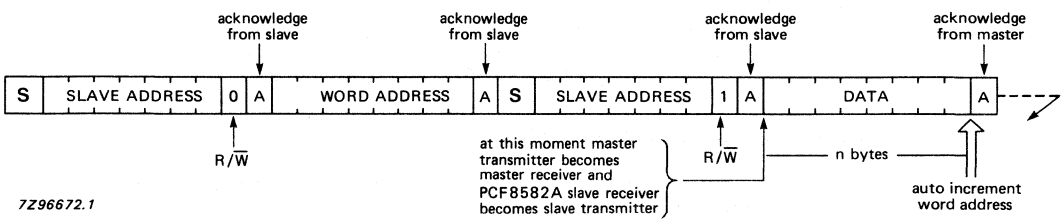
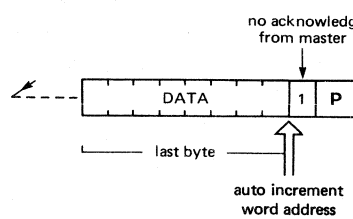


Fig. 4(b) Master reads PCF 8582A slave after setting word address (write word address; READ data).



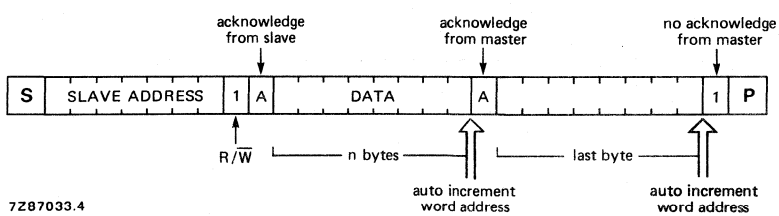


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

* The device can be used as read only without the programming clock.

I²C-bus timing

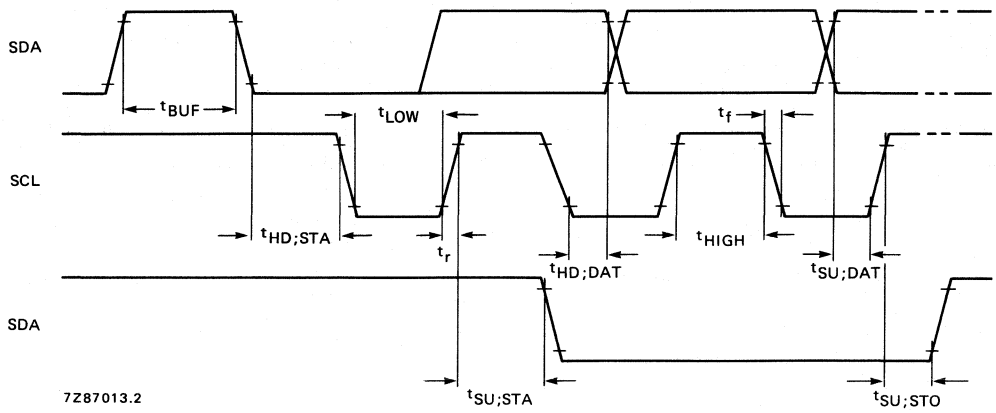
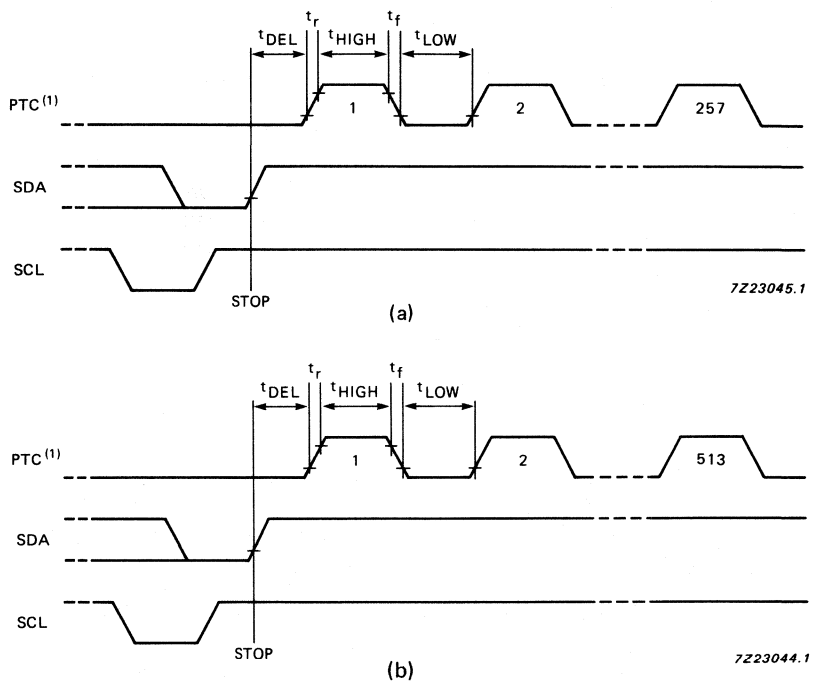


Fig. 5 I²C-bus timing.



(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	–	1	mA
Output current	$\|I_O\|$	–	10	mA

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	V_{OH} = V_{DD}	I_{LO}	–	–	1	μA
Input leakage current (SCL)	V_I = V_{DD} or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1.	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	20	–	100	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	2.57	–	12.85	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

CLOCK CALENDAR WITH 256 × 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

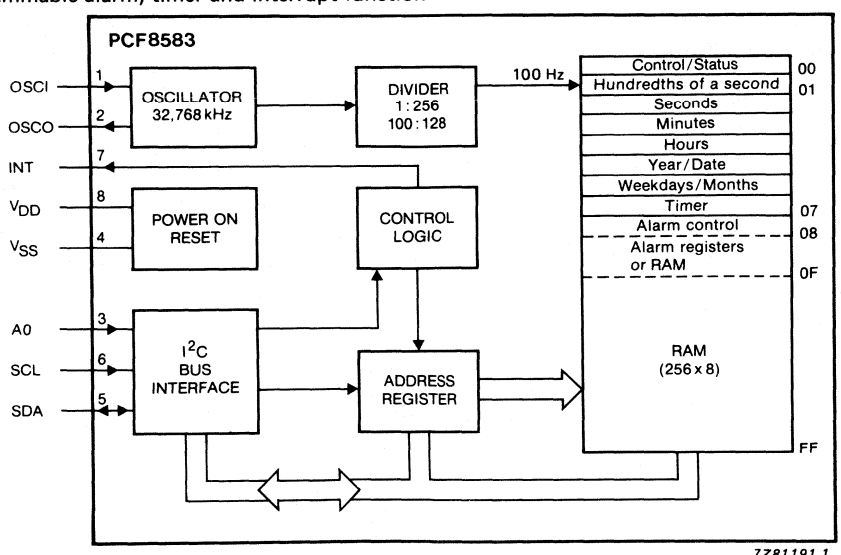


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C bus
6	SCL	serial clock line	I^2C bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

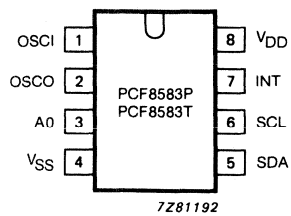


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V_{DD}		−0,8 to 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
DC input current (any input)	I_I	max.	10	mA
DC output current (any output)	I_O	max.	10	mA
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

Note

1. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

DEVELOPMENT DATA

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

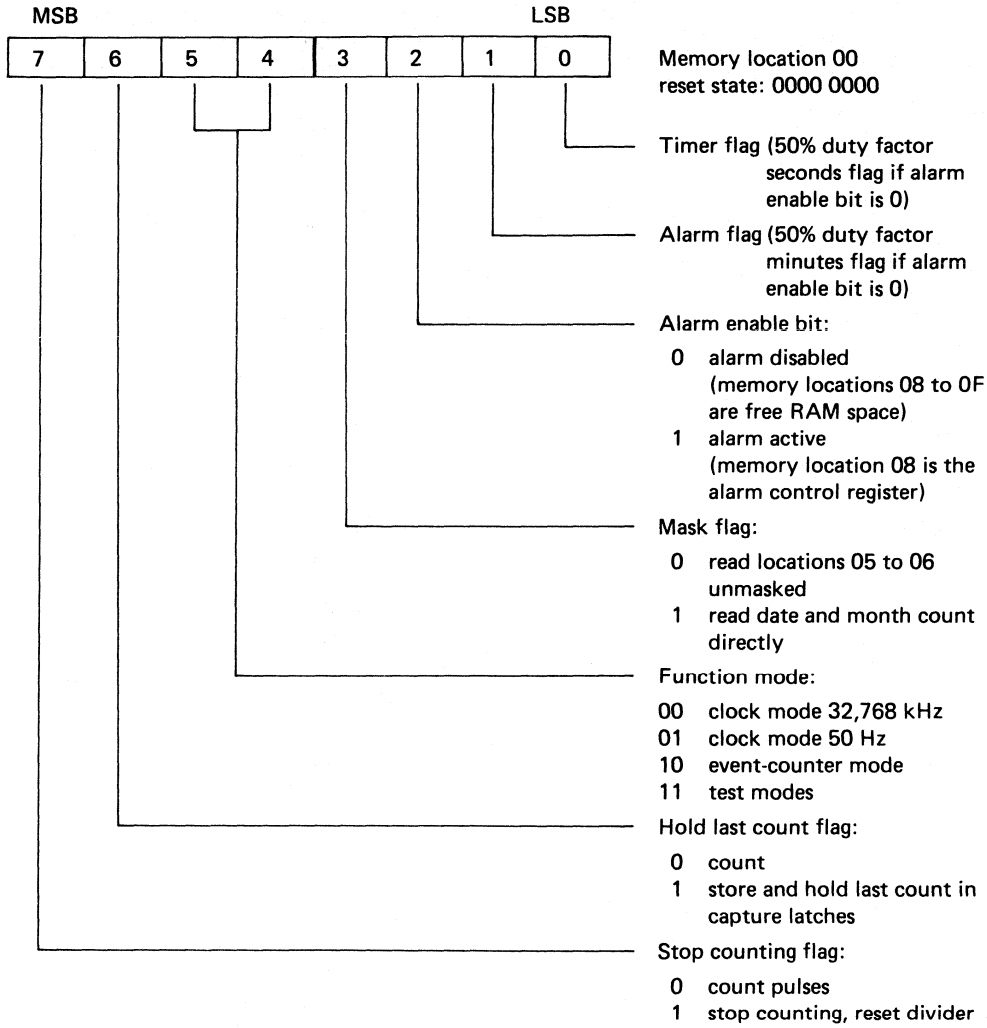


Fig. 3 Control/status register.

DEVELOPMENT DATA

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

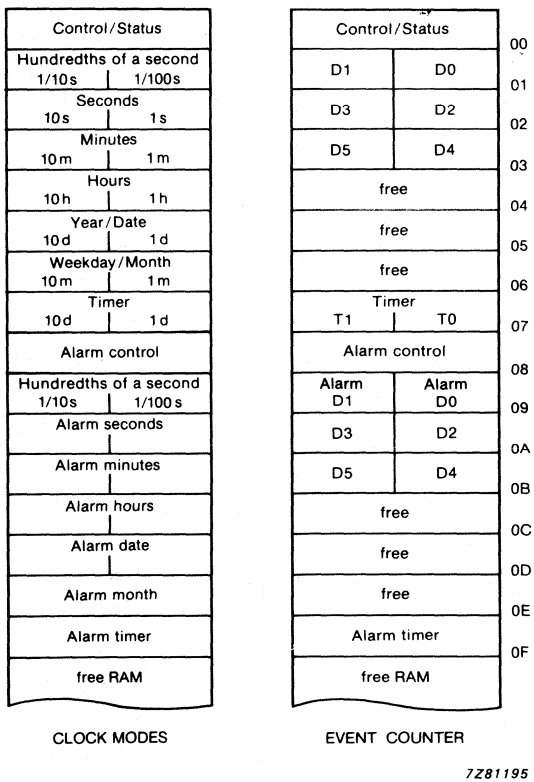


Fig. 4 Register arrangement.

Counter registers (continued)

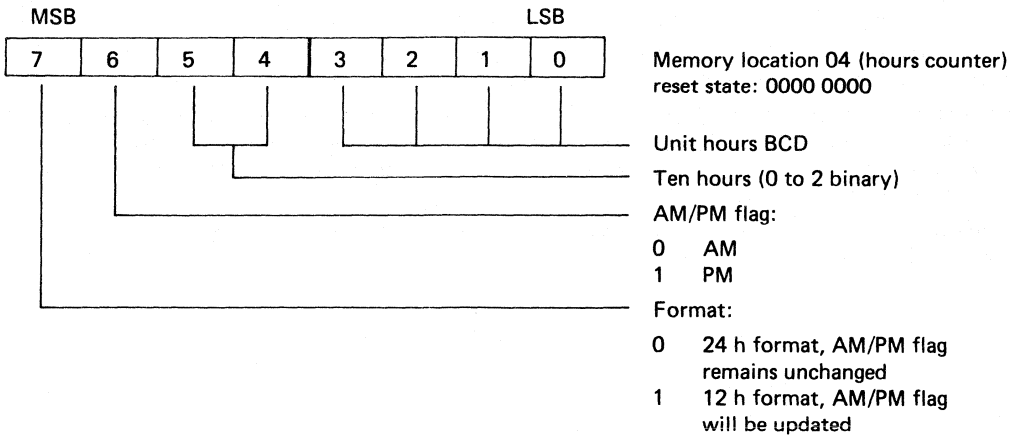


Fig. 5 Format of the hours counter.

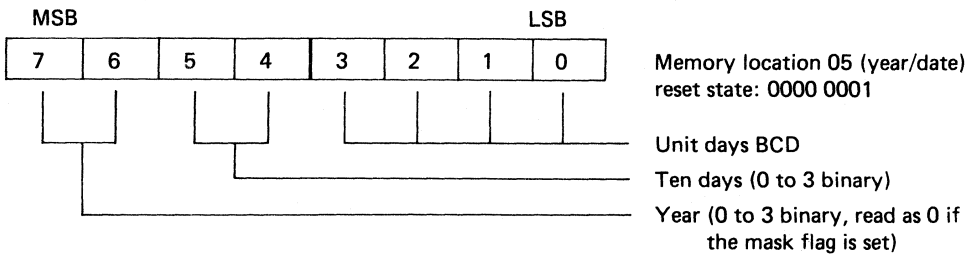


Fig. 6 Format of the year/date counter.

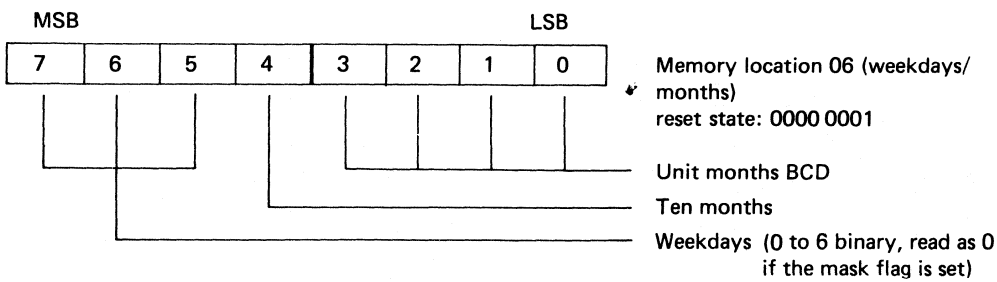


Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, 12
	01 to 30	30 to 01	4, 6, 9, 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

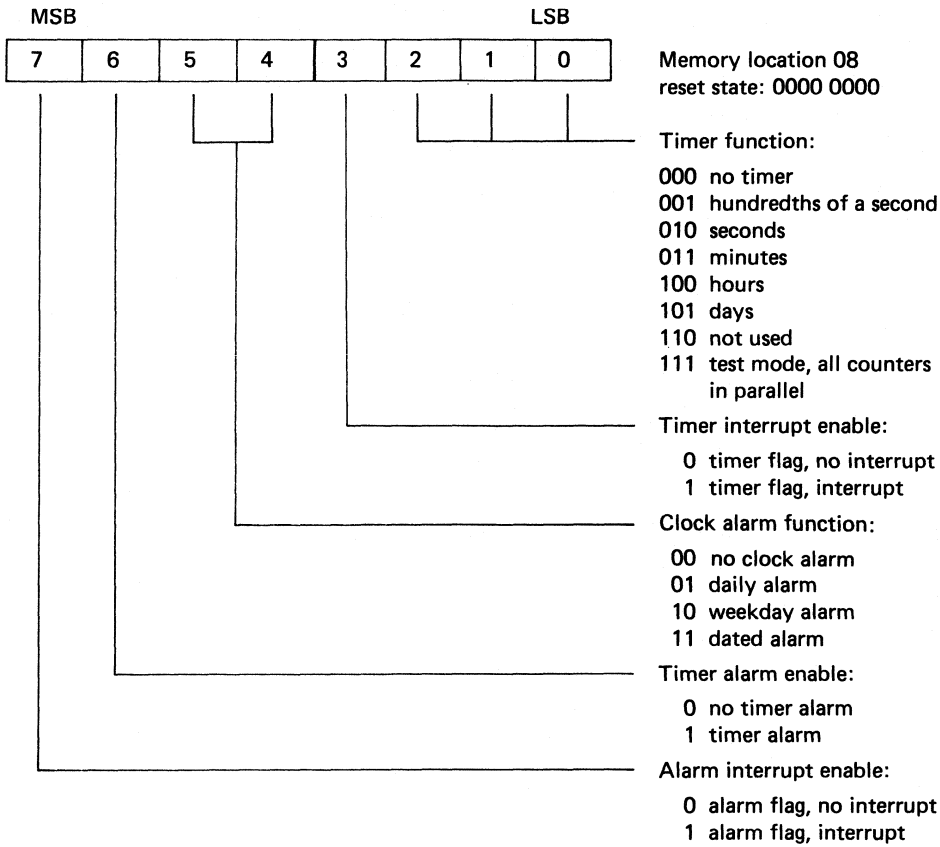


Fig. 8a Alarm control register, clock modes.

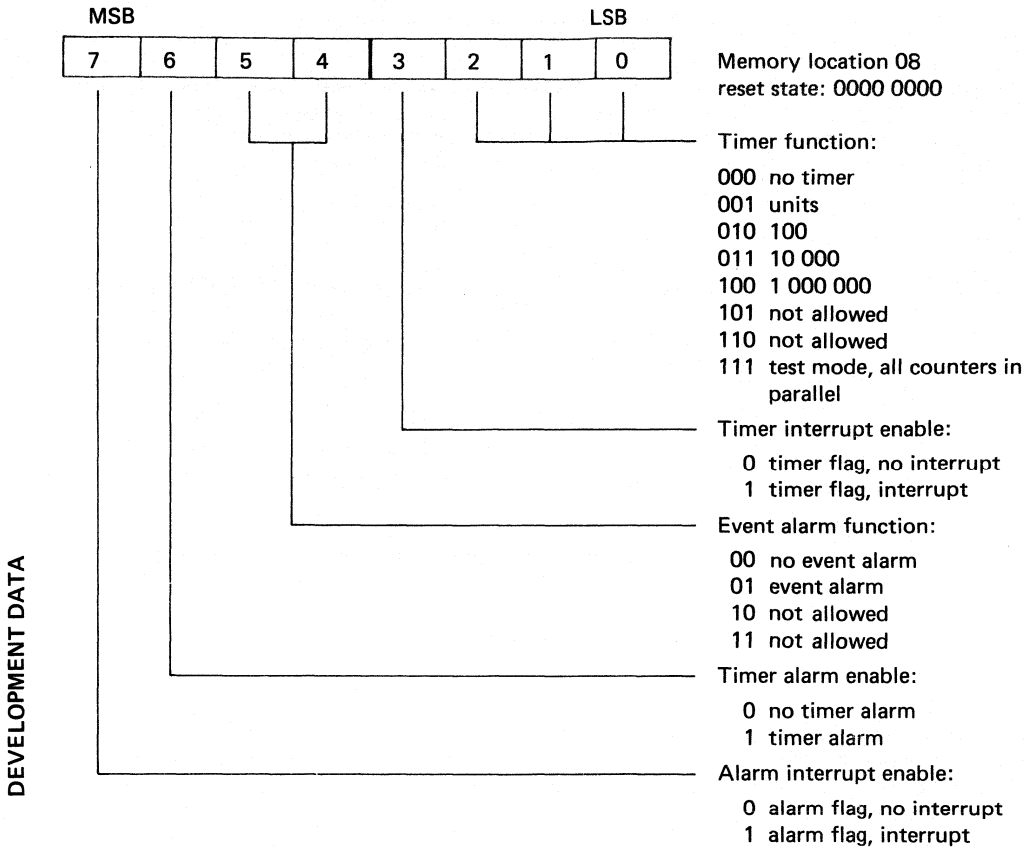


Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

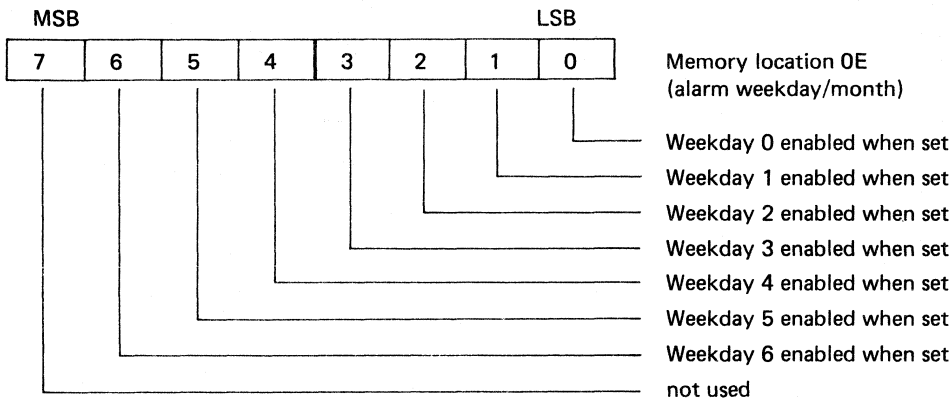


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I^2C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

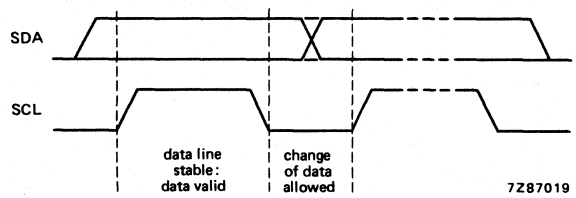


Fig. 10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

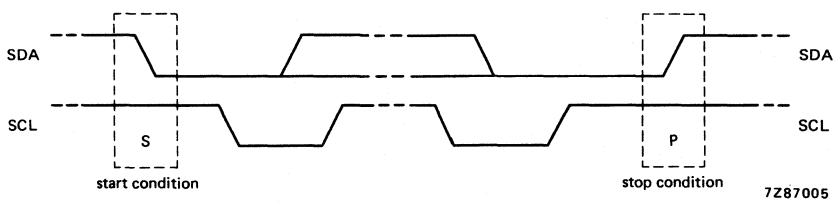


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

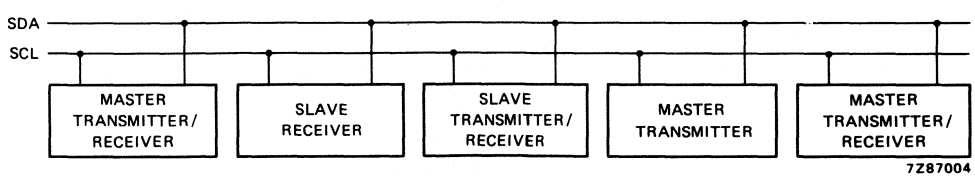


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

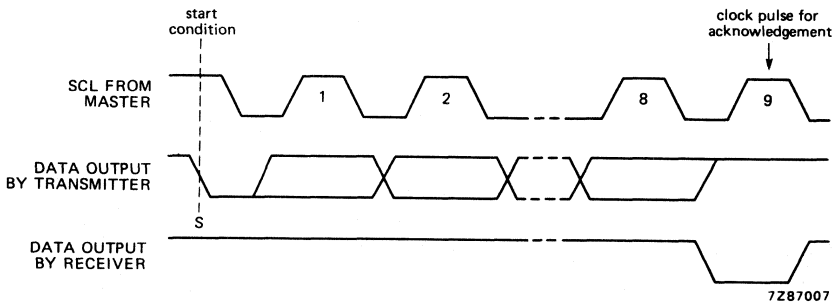


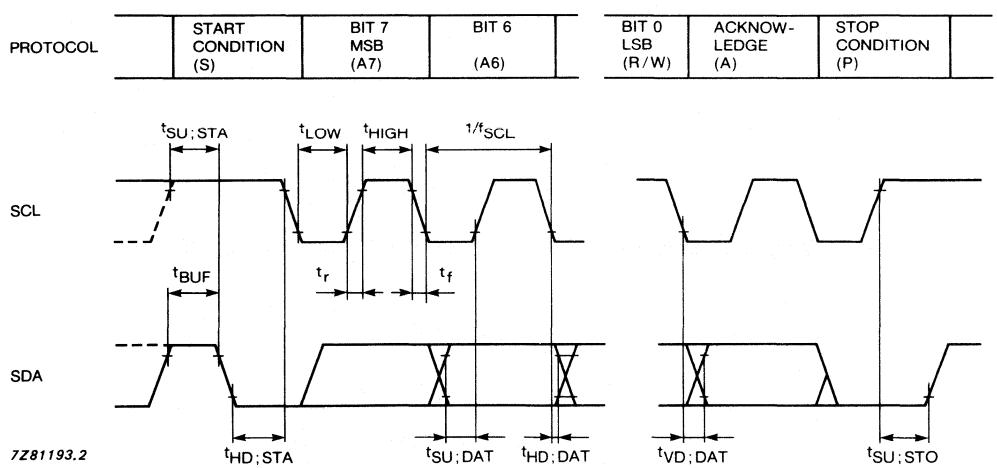
Fig. 13 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs



I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

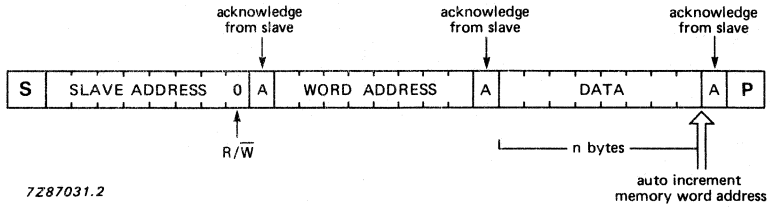


Fig. 15a Master transmits to slave receiver (WRITE mode).

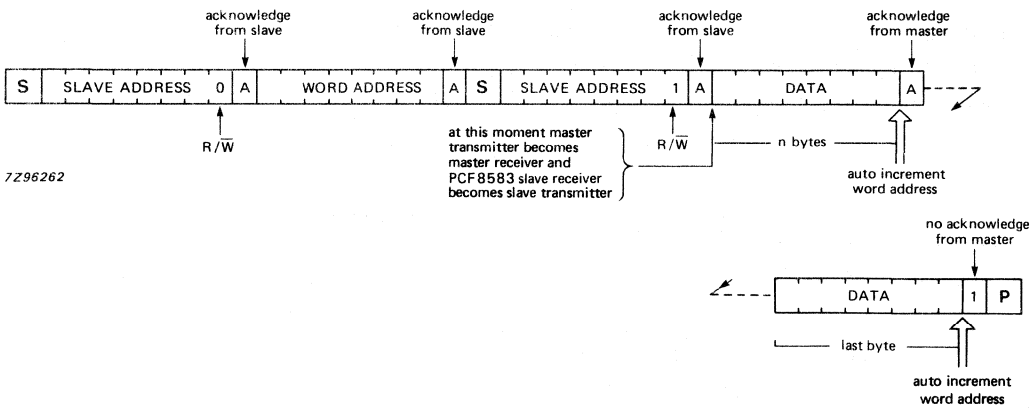


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

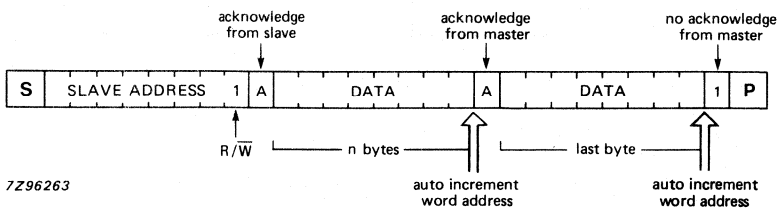


Fig. 15c Master reads slave immediately after first byte (READ mode).

CHARACTERISTICS

V_{DD} = 2,0 to 6,0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (operating)	V_{DD}	2,5	–	6	V
Supply voltage (clock)	V_{DD}	1,0	–	6	V
Supply current T_{amb} = 0 to 70 °C operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
Clock at V_{DD} = 5 V	I_{DDO}	–	10	50	μA
Clock at V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW (note 2)	V_{IL}	–0,8	–	0,3 x V_{DD}	V
Input voltage HIGH (note 2)	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
Input leakage current at V_I = V_{DD} or V_{SS}	± I_I	–	–	250	nA
Input capacitance (SCL, SDA) at V_I = V_{SS}	C_I	–	–	7	pF
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V (note 3)	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = –25 to + 70 °C (note 3)	I_{DDR}	–	–	2	μA
Oscillator					
Integrated oscillator capacitance	C_{OSC}	–	40	–	pF
Oscillator stability for: ΔV_{DD} = 100 mV at V_{DD} = 1,5 V; T_{amb} = 25 °C	f/f_{OSC}	–	2×10^{-6}	–	–

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	KΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.
3. Event or 50 Hz mode only (no Quartz).

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

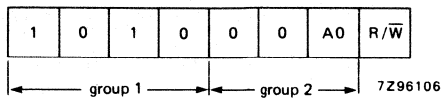


Fig. 16 PCF8583 address.

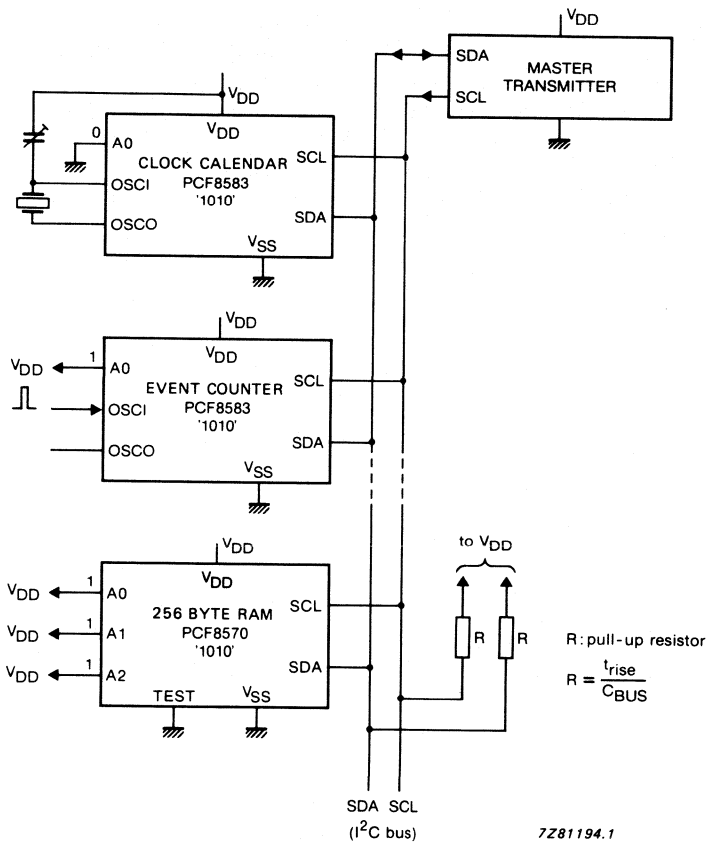


Fig. 17 PCF8583 application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

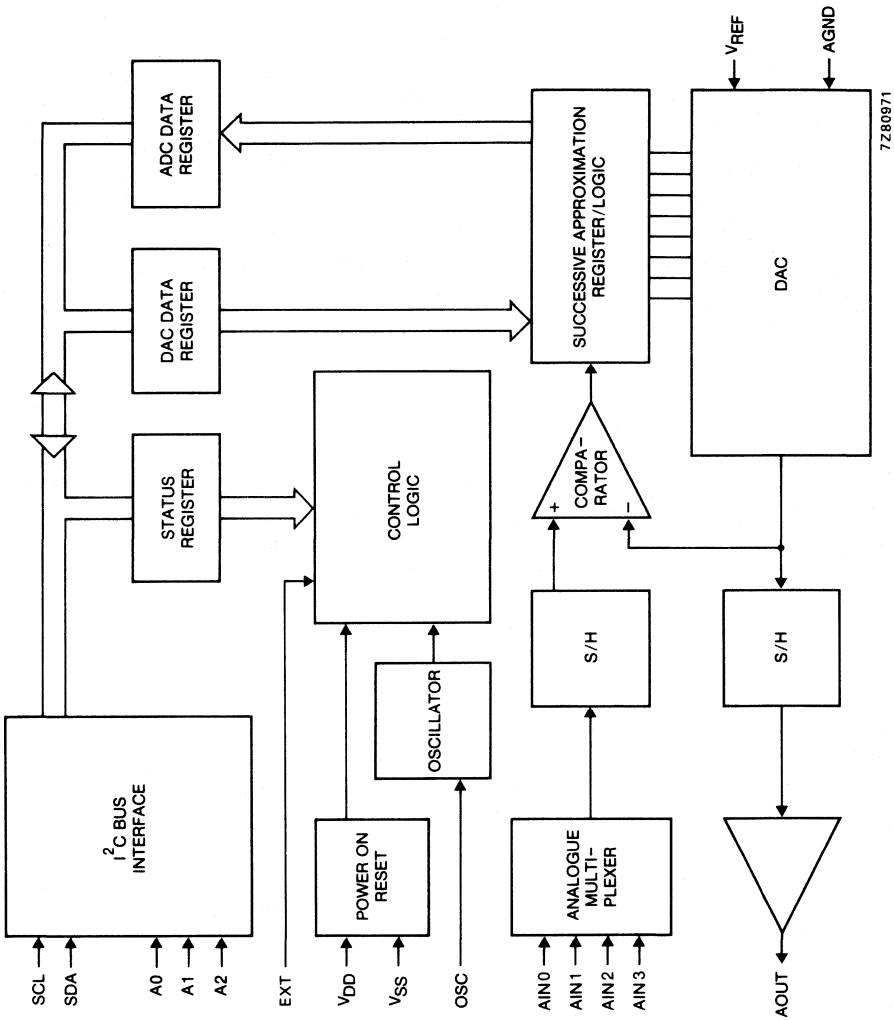


Fig. 1 Block diagram.

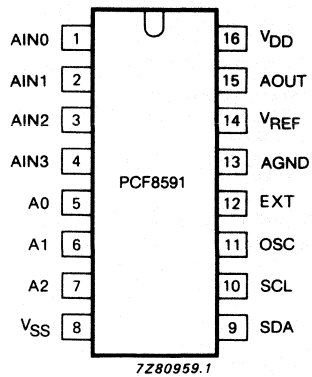


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

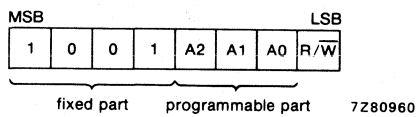


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

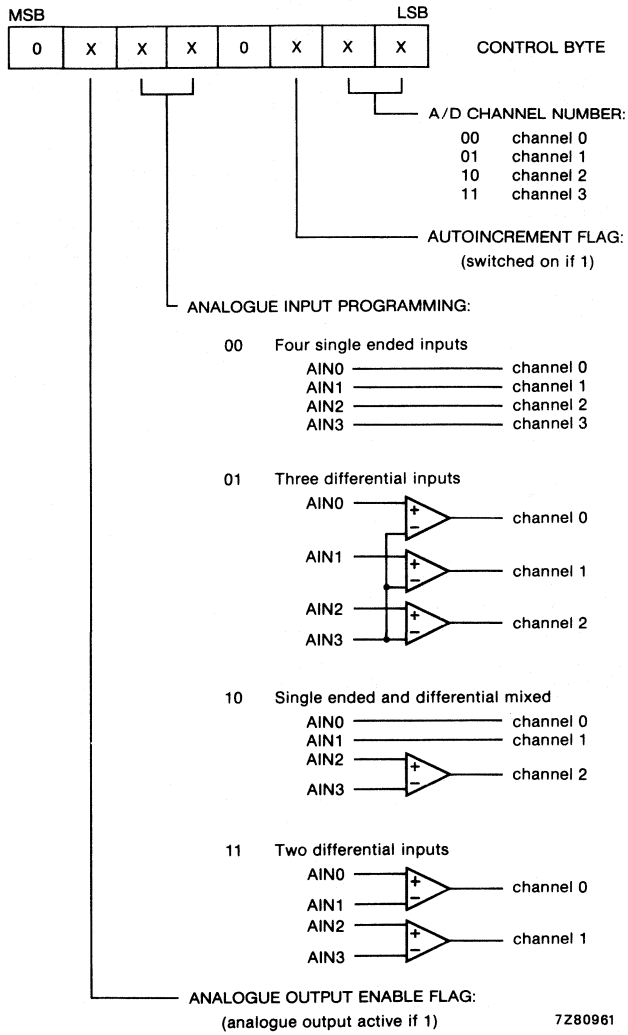


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

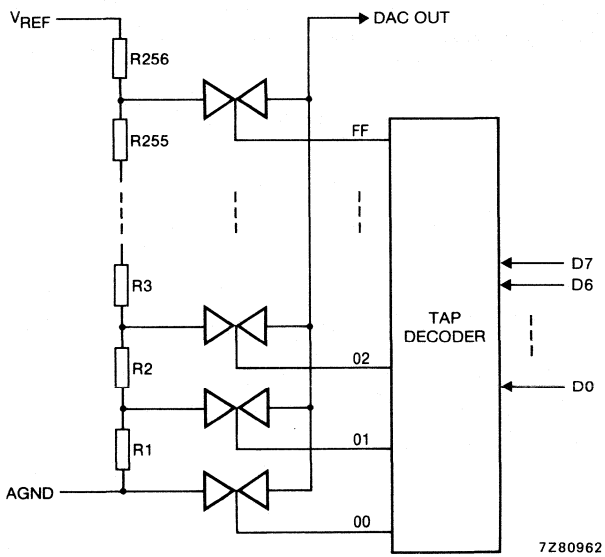


Fig. 5 DAC resistor divider chain.

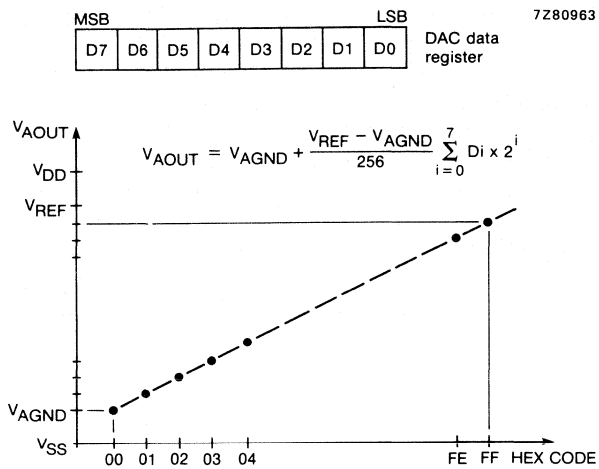


Fig. 6 DAC data and d.c. conversion characteristics.

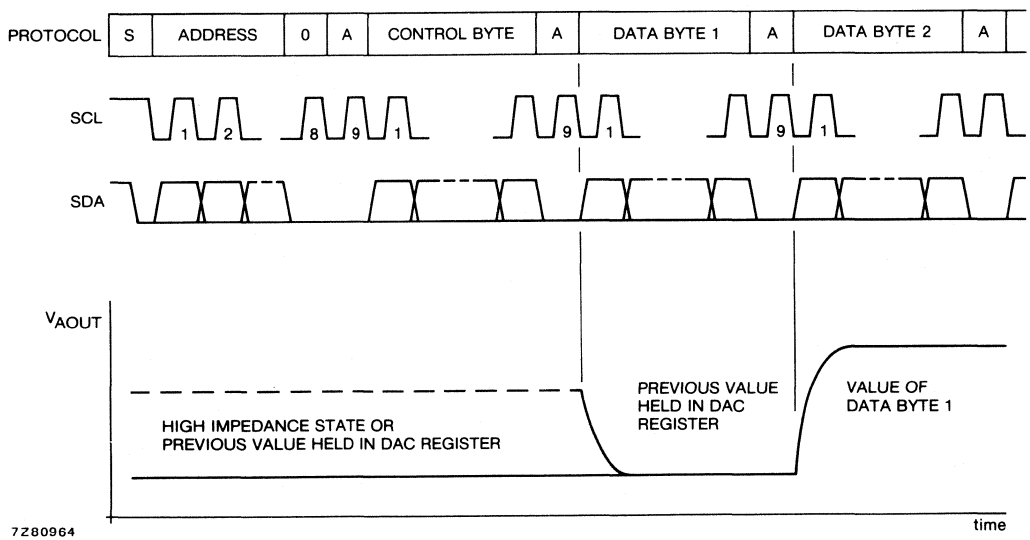


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

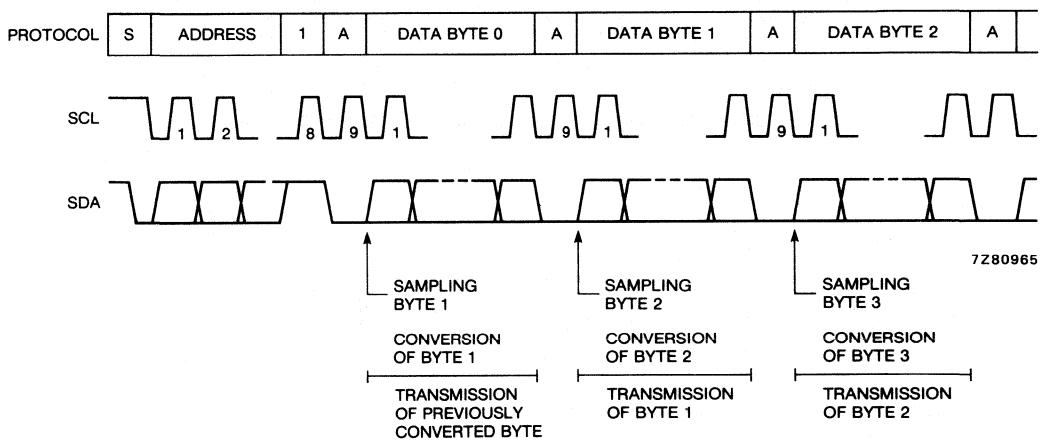


Fig. 8 A/D conversion sequence.

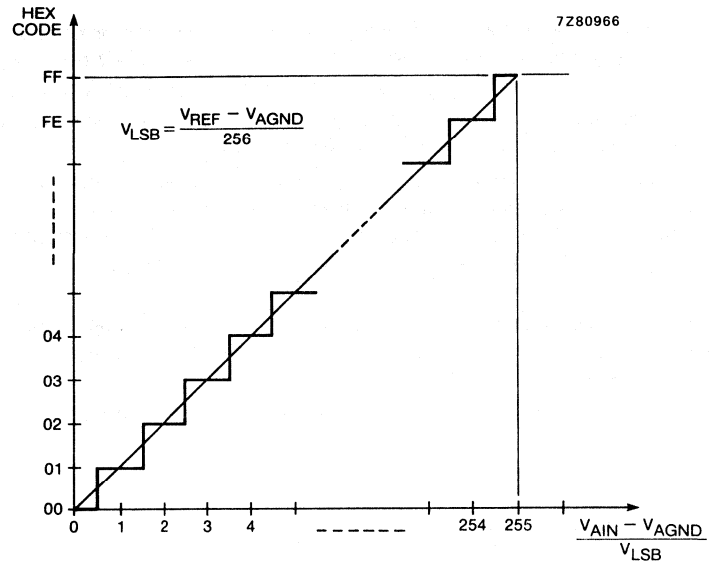


Fig. 9a A/D conversion characteristics of single-ended inputs.

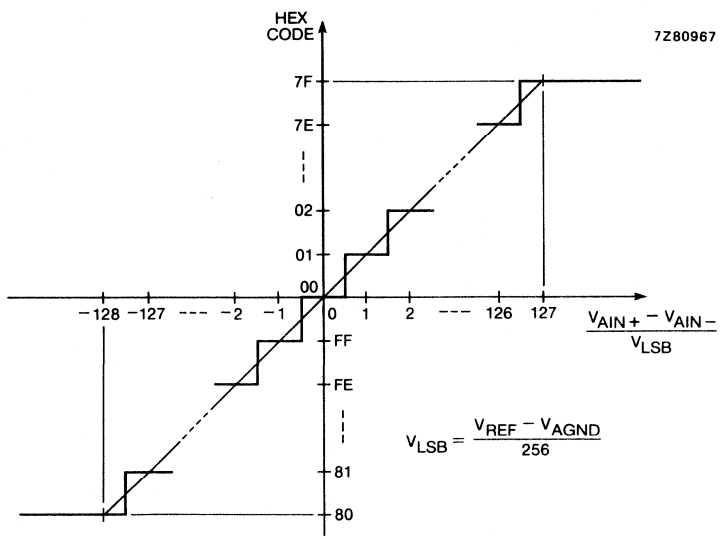


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

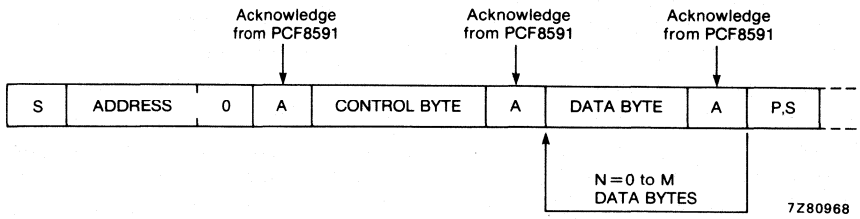


Fig. 10a Bus protocol for write mode, D/A conversion.

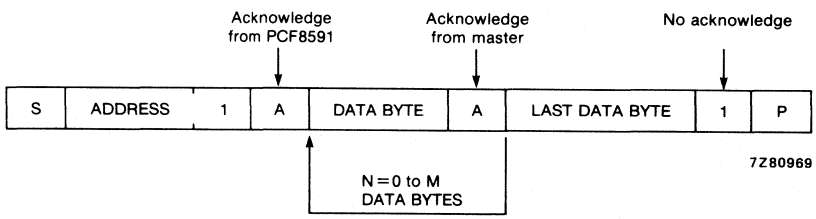


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

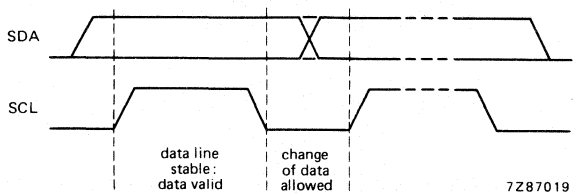


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

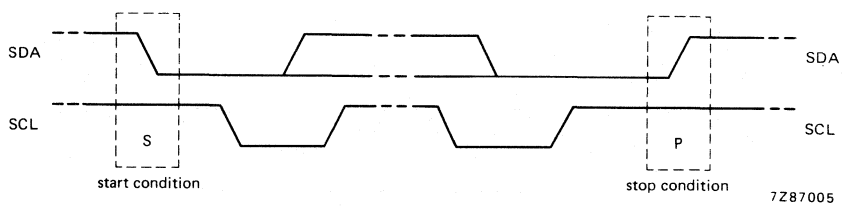


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

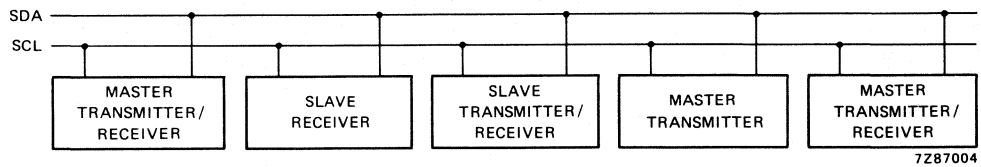


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

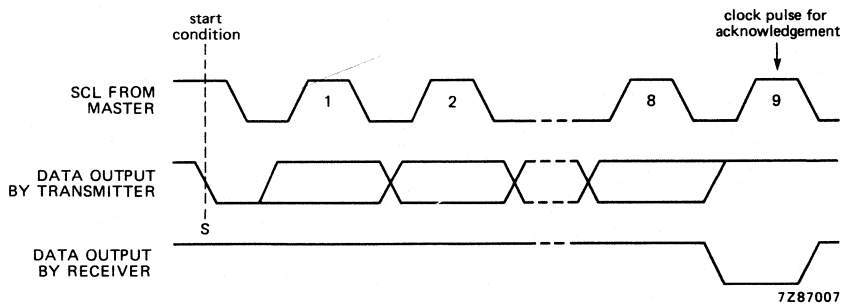


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

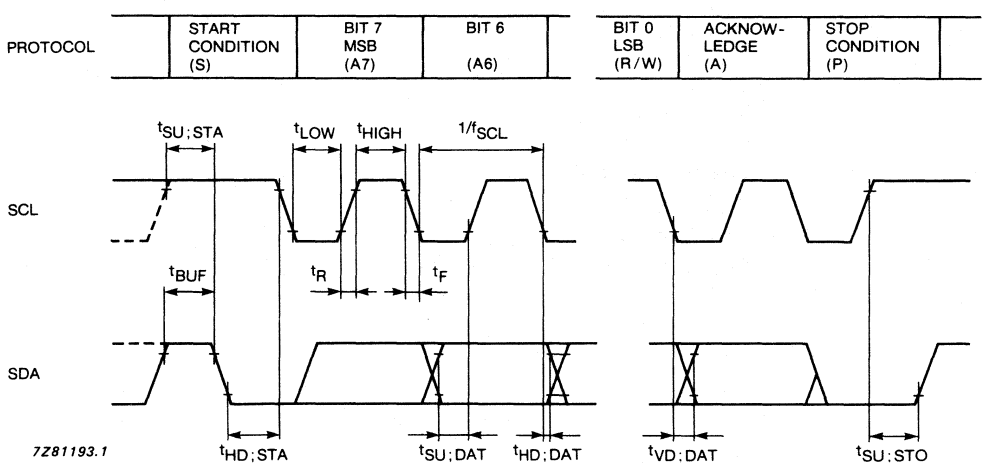


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

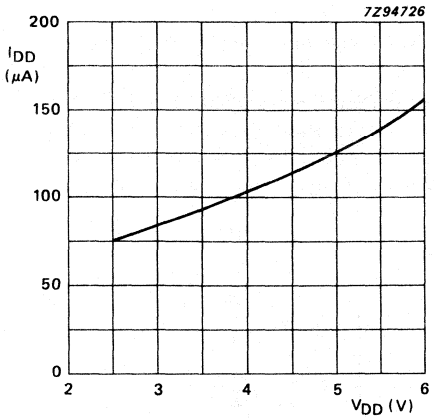
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

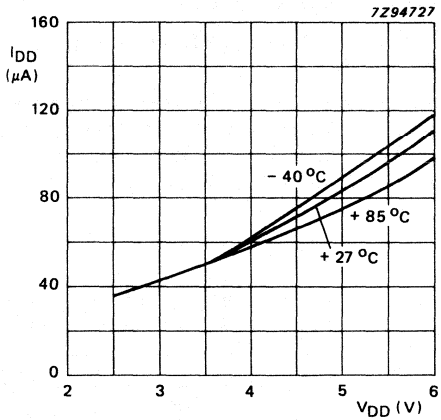
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; V_{DDN} = 0,1xV_{PP}	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



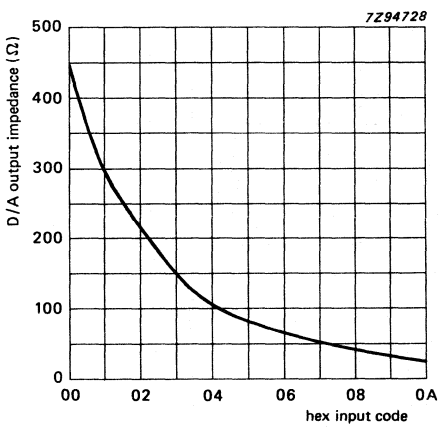
(a) internal oscillator; T_{amb} = + 27 °C.



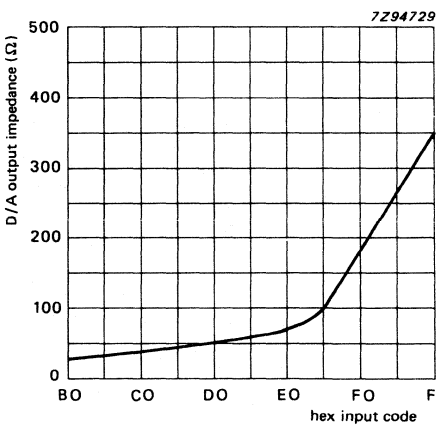
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10 μF) are recommended for power supply and reference voltage inputs.

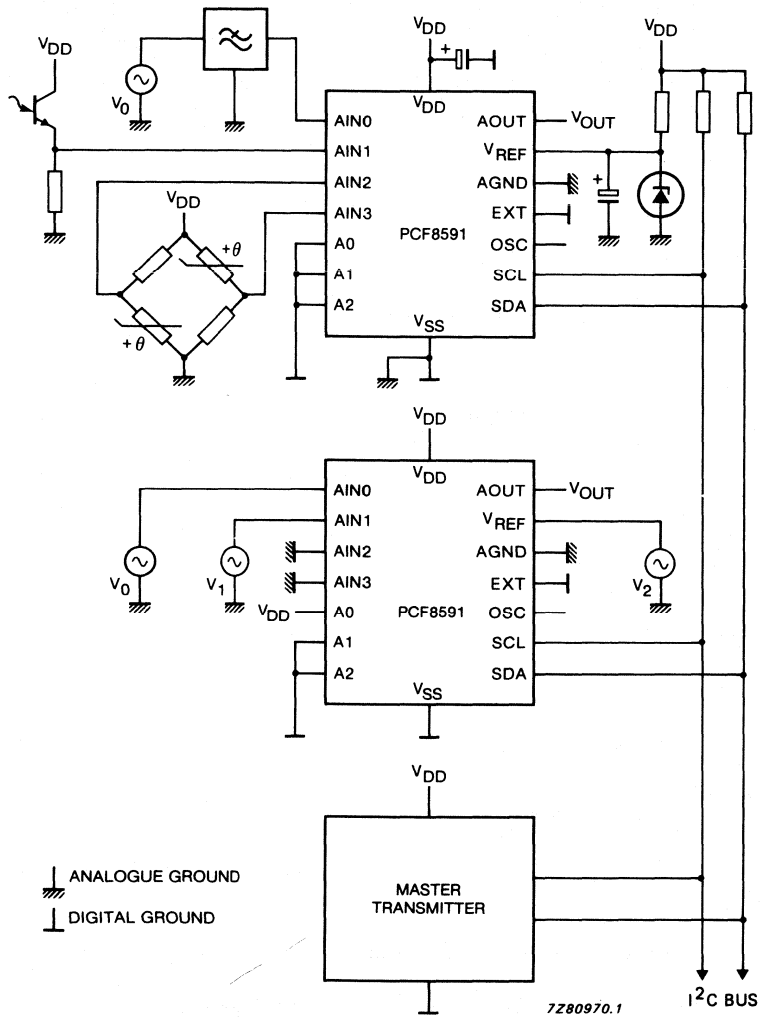


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

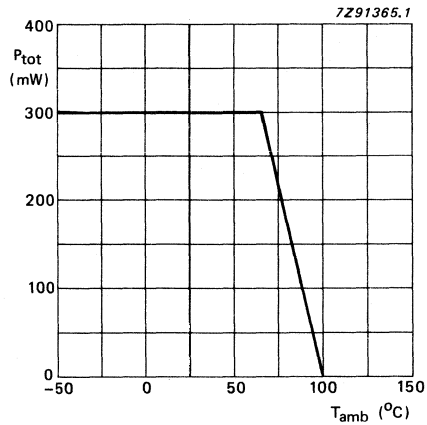


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

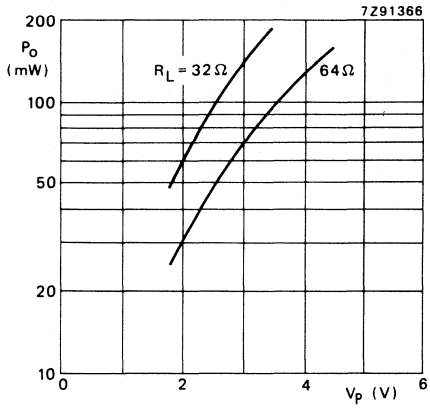


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

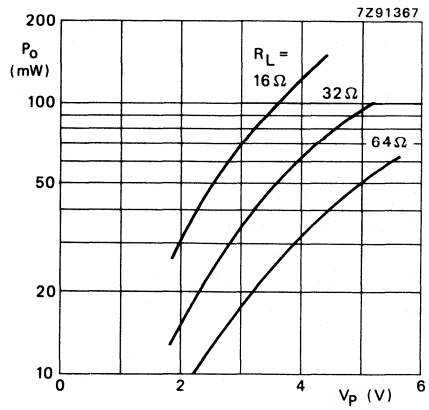


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

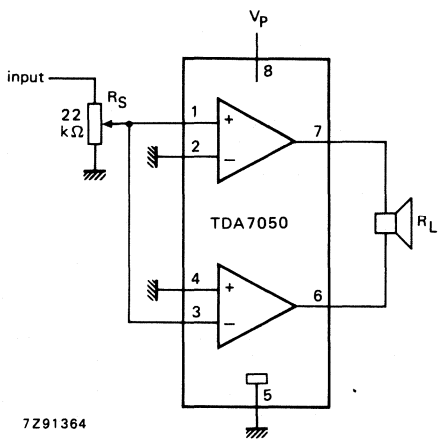


Fig. 4 Application diagram (BTL); also used as test circuit.

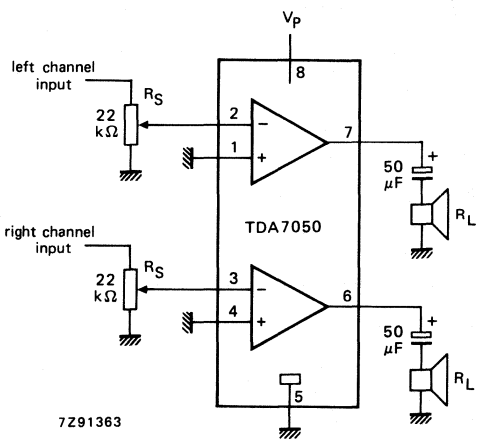


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6	V
Peak output current	I_{OM}	max.	150	mA
Total power dissipation	see derating curve Fig. 1			
Storage temperature range	T_{stg}	−55 to +	150	°C
Crystal temperature	T_c	max.	100	°C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5	s

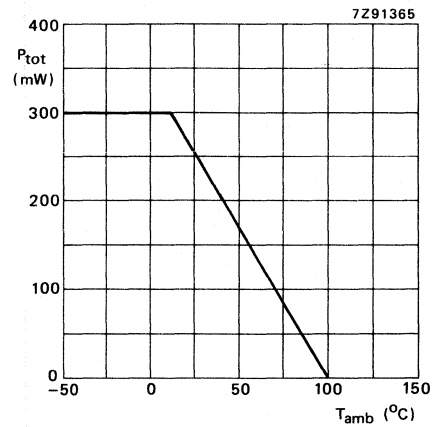


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\|\Delta V\|$	–	–	70	mV
Input impedance (at R_S = ∞)	$\|Z_i\|$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\|Z_i\|$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

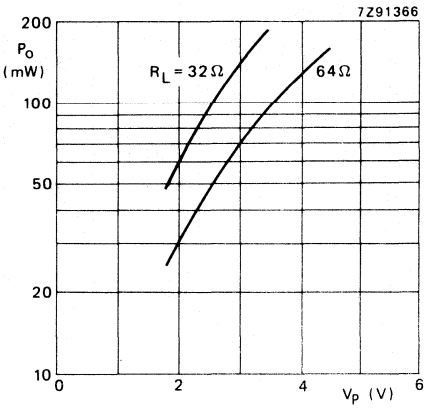


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

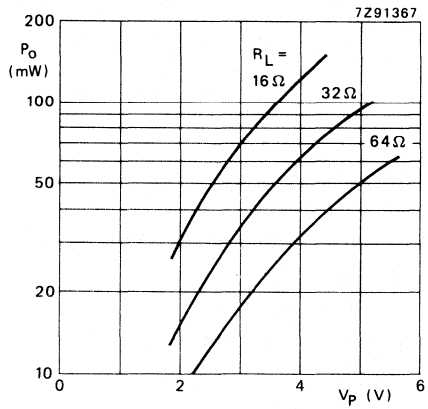


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

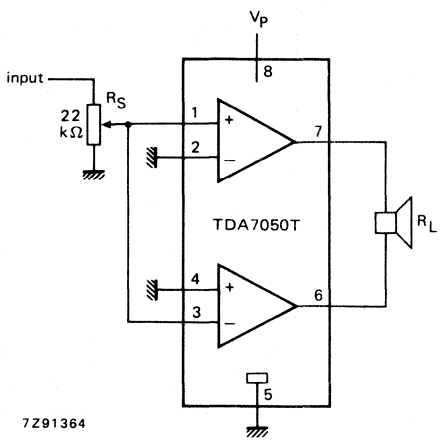


Fig. 4 Application diagram (BTL); also used as test circuit.

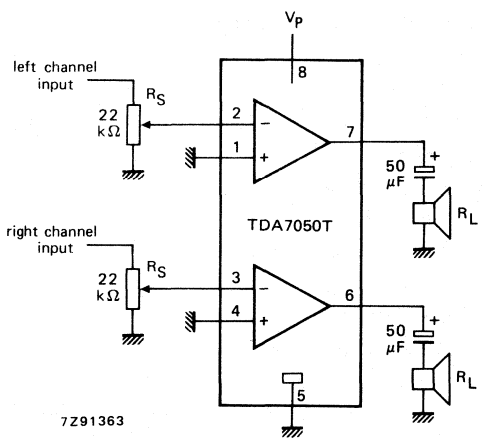


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

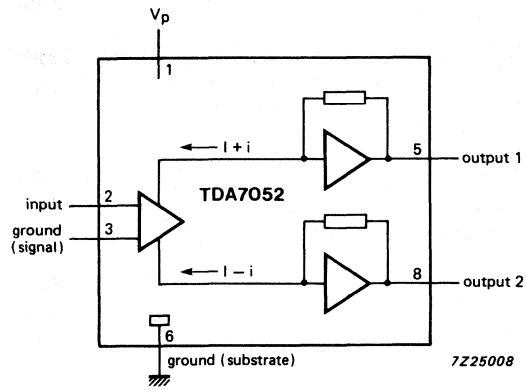


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

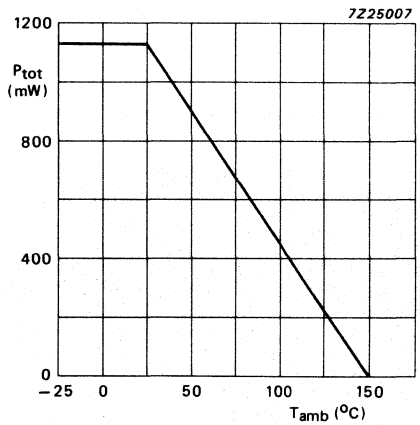


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_V	39	40	41	dB
Output power	THD = 10%	P_o	*	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

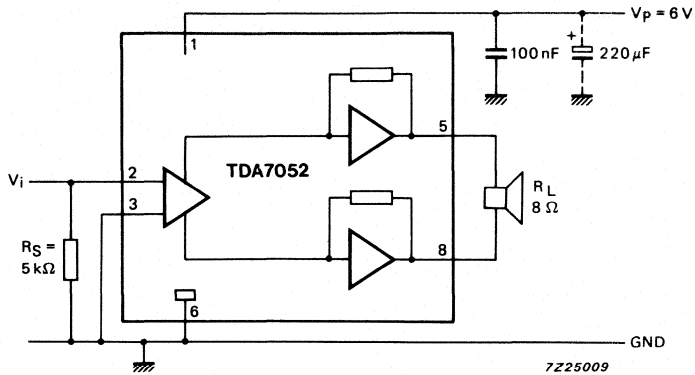


Fig. 3 Application diagram.

DEVELOPMENT DATA

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech, and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ. 4,45	V
Line current operating range (pin 1)	I_{line}	10 to 140	mA
Internal supply current			
power down input LOW	I_{CC}	typ. 1	mA
power down input HIGH	I_{CC}	typ. 55	μA
Supply voltage for pheripherals at I_{line} = 15 mA, mute input HIGH			
I_P = 1,2 mA	V_{CC}	min. 2,8	V
I_P = 1,7 mA	V_{CC}	min. 2,5	V
Voltage amplification range			
microphone amplifier			
TEA1060	A_{vd}	44 to 60	dB
TEA1061	A_{vd}	30 to 46	dB
receiving amplifier	A_{vd}	17 to 39	dB
Line loss compensation			
Amplification control range	ΔA_{vd}	typ. 5,9	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance range	R_{exch}	400 to 1000	Ω
Operating ambient temperature range	T_{amb}	−25 to + 75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

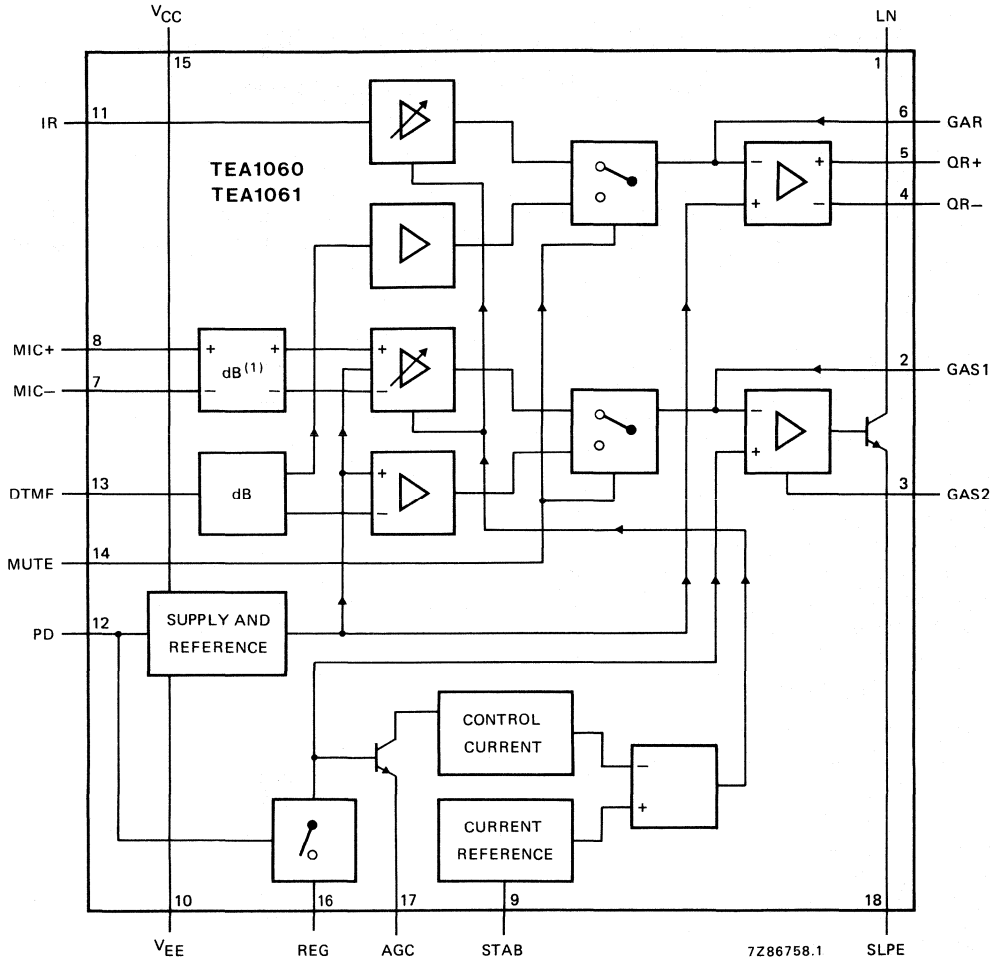


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

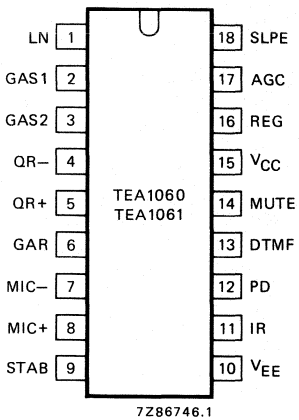


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line connection
2	GAS1	gain adjustment connection, sending amplifier
3	GAS2	gain adjustment connection, sending amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment connection, receiving amplifier
7	MIC–	non-inverting microphone input
8	MIC+	inverting microphone input
9	STAB	current stabilizer connection
10	V_{EE}	negative line connection
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling connection
16	REG	voltage regulator decoupling connection
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment connection

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the d.c. resistance of the subscriber line (R_{line}) and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current (I_{line}) exceeds the current I_{CC} + 0,5 mA required by the circuit itself (I_{CC} ca. 1 mA), plus the current I_P required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5 \times 10^{-3} - I_P) \times R9.$$

V_{ref} being an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.

Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0,5 mA + I_P. The static behaviour of the circuit then equals a 4,2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}.

FUNCTIONAL DESCRIPTION (continued)

Supply: V_{CC}, LN, SLPE, REG and STAB (continued)

This resistor connected between pins 1 and 16 (LN and REG) will decrease the internal reference voltage. R_{VA} connected between pins 16 and 18 (REG and SLPE) will increase the internal reference voltage.

The current I_P available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 4 shows this current for $V_{CC} > 2{,}2$ V and for $V_{CC} > 3$ V. Of which 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.
The TEA1060 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 8,2 kΩ (2 x 4,1 kΩ and its voltage amplification is typ. 52 dB.
The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40,8 kΩ (2 x 20,4 kΩ) and its voltage amplification is typ. 38 dB. The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier in both types can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25,5 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.

When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the average line impedance.

FUNCTIONAL DESCRIPTION (continued)

Side-tone suppression (continued)

The anti-side-tone network as used in the standard application (Fig. 10) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage (d.c.)	V_{LN}	max.	12	V
Repetitive line voltage during switch-on or line interruption	V_{LN}	max.	13,2	V
Repetitive peak line voltage t_p/P = 1 ms/5 s; R_{10} = 13 Ω; R_9 = 20 Ω (see Fig. 10)	$V_{LN(RM)}$	max.	28	V
Line current	I_{line}	max.	140	mA
Voltage on all other pins	V_i	max.	V_{CC} + 0,7	V
	$-V_i$	max.	0,7	V
Total power dissipation	P_{tot}	max.	660	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C, R9 = 20 Ω; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	3,95	4,25	4,55	V
at I_{line} = 15 mA	V_{LN}	4,25	4,45	4,65	V
at I_{line} = 100 mA	V_{LN}	5,40	6,10	6,7	V
at I_{line} = 140 mA	V_{LN}	–	–	7,5	V
Variation with temperature					
at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit					
at I_{line} = 15 mA					
$R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3,50	3,80	4,05	V
$R_{VA} = R_{16\text{-}18}$ = 39 kΩ	V_{LN}	4,70	5,0	5,30	V
Supply current					
PD = LOW; V_{CC} = 2,8 V	I_{CC}	–	0,96	1,30	mA
PD = HIGH; V_{CC} = 2,8 V	I_{CC}	–	55	82	μA
Microphone inputs MIC+ and MIC (pins 7 and 8)					
Input impedance					
TEA1060	$\lvert z_{is} \rvert$	3,3	4,1	4,9	kΩ
TEA1061	$\lvert z_{is} \rvert$	16,5	20,4	24,3	kΩ
Common-mode rejection ratio; TEA1060	k_{CMR}	–	82	–	dB
Voltage amplification					
I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060	A_{vd}	51	52	53	dB
TEA1061	A_{vd}	37	38	39	dB
Variation with frequency					
at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Dual-tone multi-frequency input DTMF (pin 13)					
Input impedance	$\lvert z_{is} \rvert$	16,8	20,7	24,6	kΩ
Voltage amplification					
I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	24,5	25,5	26,5	dB
Variation with frequency					
f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)					
Amplification variation with R7 connected between pins 2 and 3; transmitting amplifier	ΔA_{vd}	−8	–	+ 8	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,9	2,3	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage					
I_{line} = 15 mA; R7 = 68 kΩ; pins 7 and 8 open					
psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR (pin 11)					
Input impedance	$\lvert z_{is} \rvert$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)					
Output impedance; single-ended	$\lvert z_{os} \rvert$	–	4	–	Ω
Voltage amplification from pin 11 to pin 4 or 5					
I_{line} = 15 mA; R4 = 100 kΩ;					
single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency					
f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Output voltage at I_p = 0; d_{tot} = 2%;					
sine-wave drive; R4 = 100 kΩ					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,3	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF					
R_{series} = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage					
I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open					
psophometrically weighted (P53 curve)					
single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)					
Amplification variation with R4					
between pins 6 and 5; receiving amplifier	ΔA_{vd}	−8	–	+8	dB
MUTE input (pin 14)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA

parameter	symbol	min.	typ.	max.	unit
Reduction of voltage amplification from MIC+ and MIC− to LN at MUTE = HIGH	$-\Delta A_{vd}$	–	70	–	dB
Voltage amplification from DTMF to QR+ or QR−; MUTE = HIGH; R4 = 100 kΩ; single-ended load R_L = 300 Ω	A_{vd}	−21	−19	−17	dB
Power down input PD					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control input AGC					
Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN R6 = 110 kΩ (between AGC and V_{EE}) amplification control range (I_{line} = 70 mA)	$-\Delta A_{vd}$	5,5	5,9	6,3	dB
Highest line current for maximum amplification	I_{line}	–	23	–	mA
Lowest line current for minimum amplification	I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA	$-\Delta A_{vd}$	1,0	1,5	2,0	dB

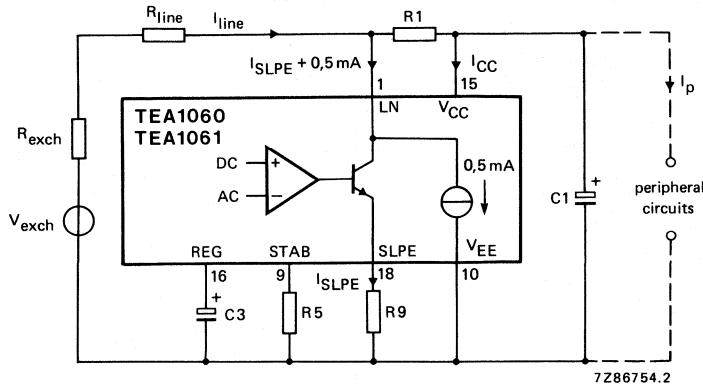
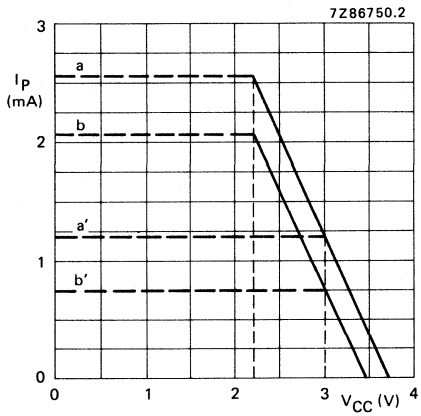


Fig. 3 Supply arrangement.



I_{line} = 15 mA at V_{LN} = 4,45 V
R1 = 620 Ω
R9 = 20 Ω

Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2,2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).
a) = 2,55 mA; b) = 2,1 mA; a') = 1,2 mA and b') = 0,75 mA.

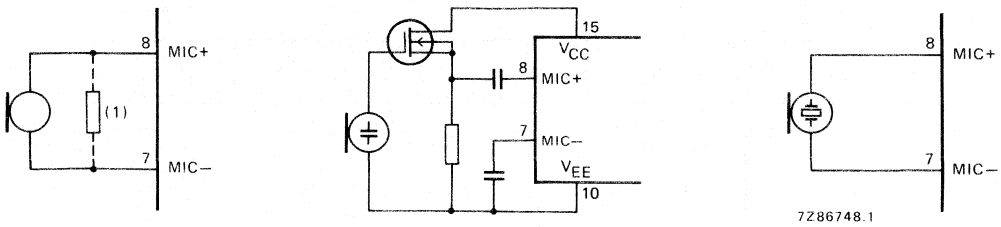


Fig. 5 Alternative microphone arrangements. a) magnetic or dynamic microphone, TEA1060. The resistor marked (1) may be connected to lower the terminating impedance. b) electret microphone, TEA1061. c) piezoelectric microphone, TEA1061.

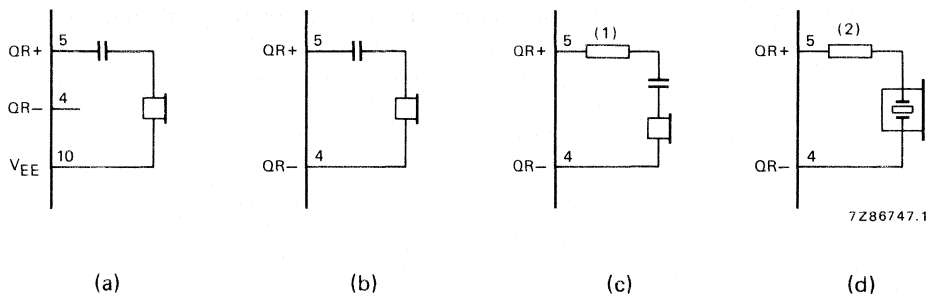


Fig. 6 Alternative receiver arrangements. a) dynamic telephone with less than 450 Ω impedance. b) dynamic telephone with more than 450 Ω impedance. c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load) d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

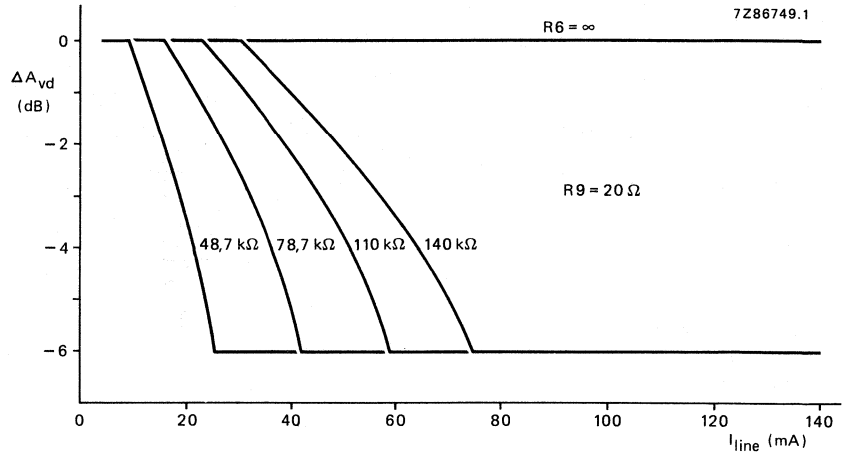


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

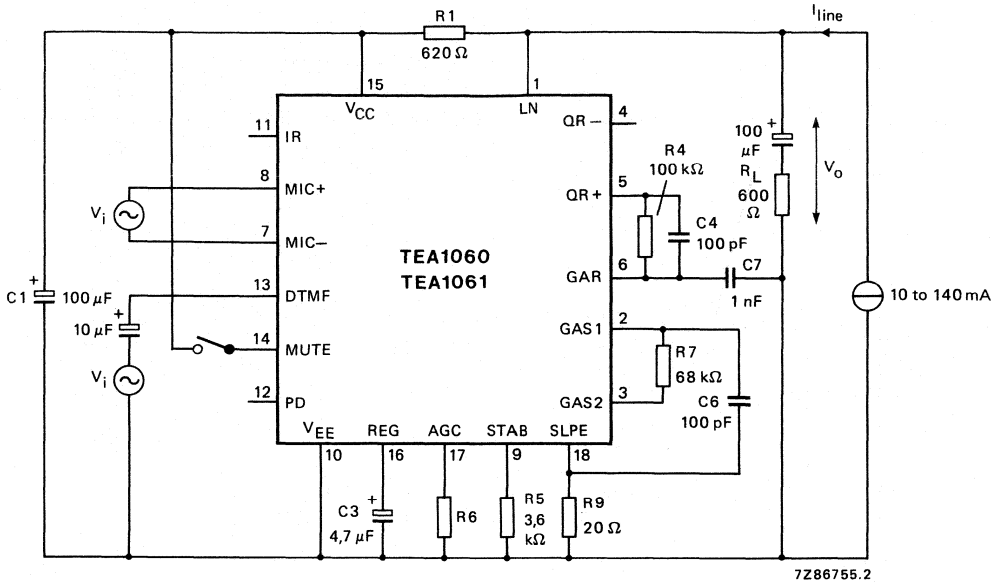


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

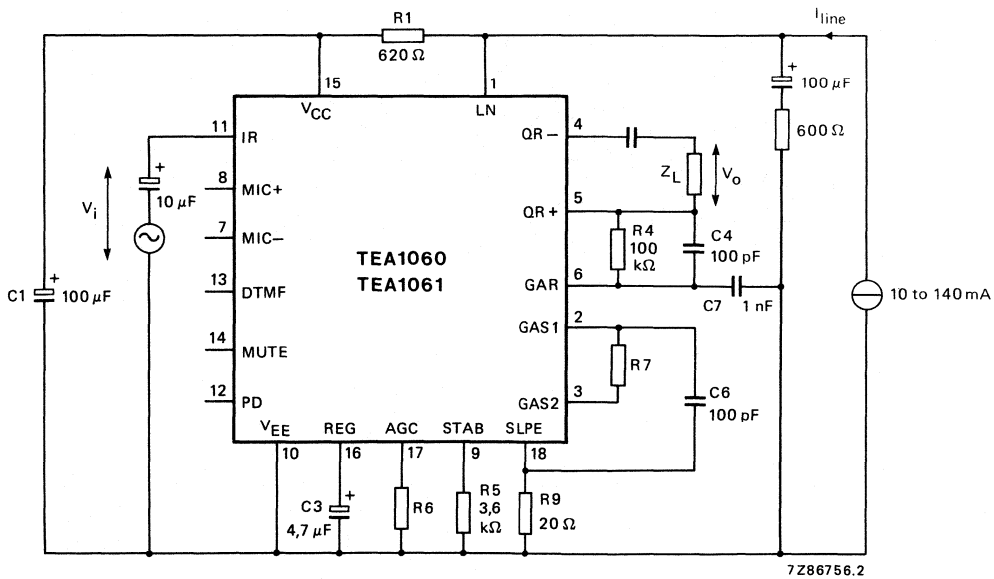


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

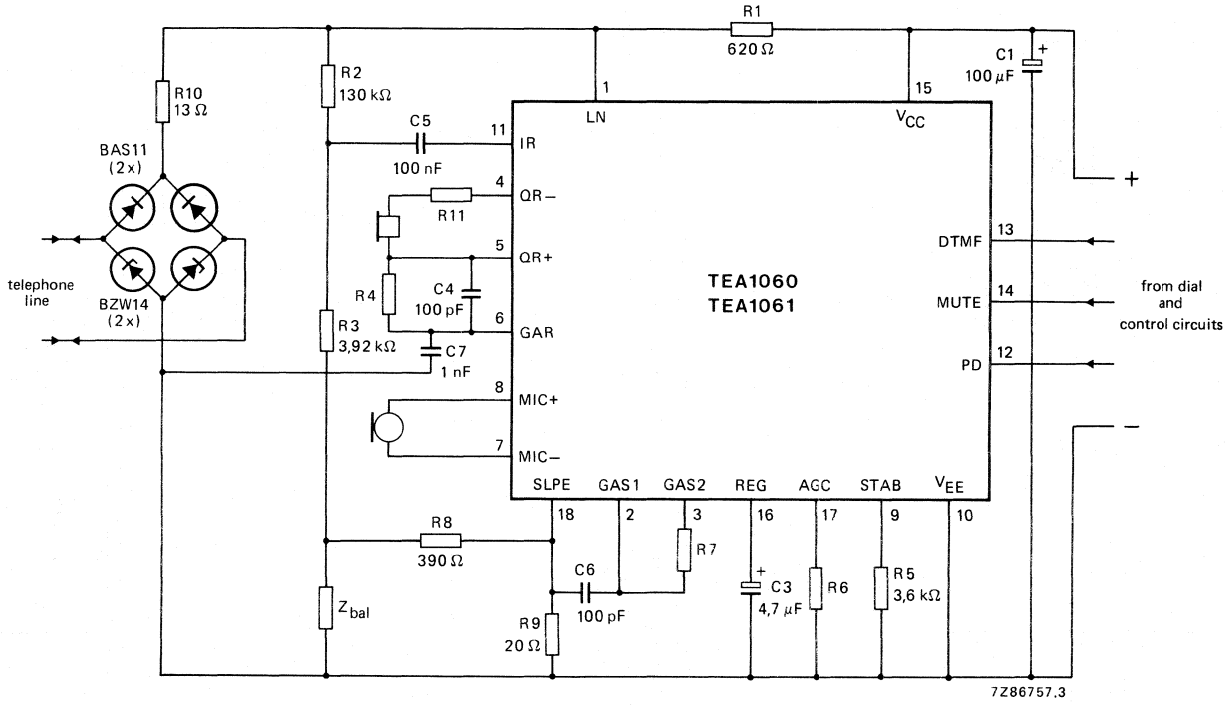


Fig. 10 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

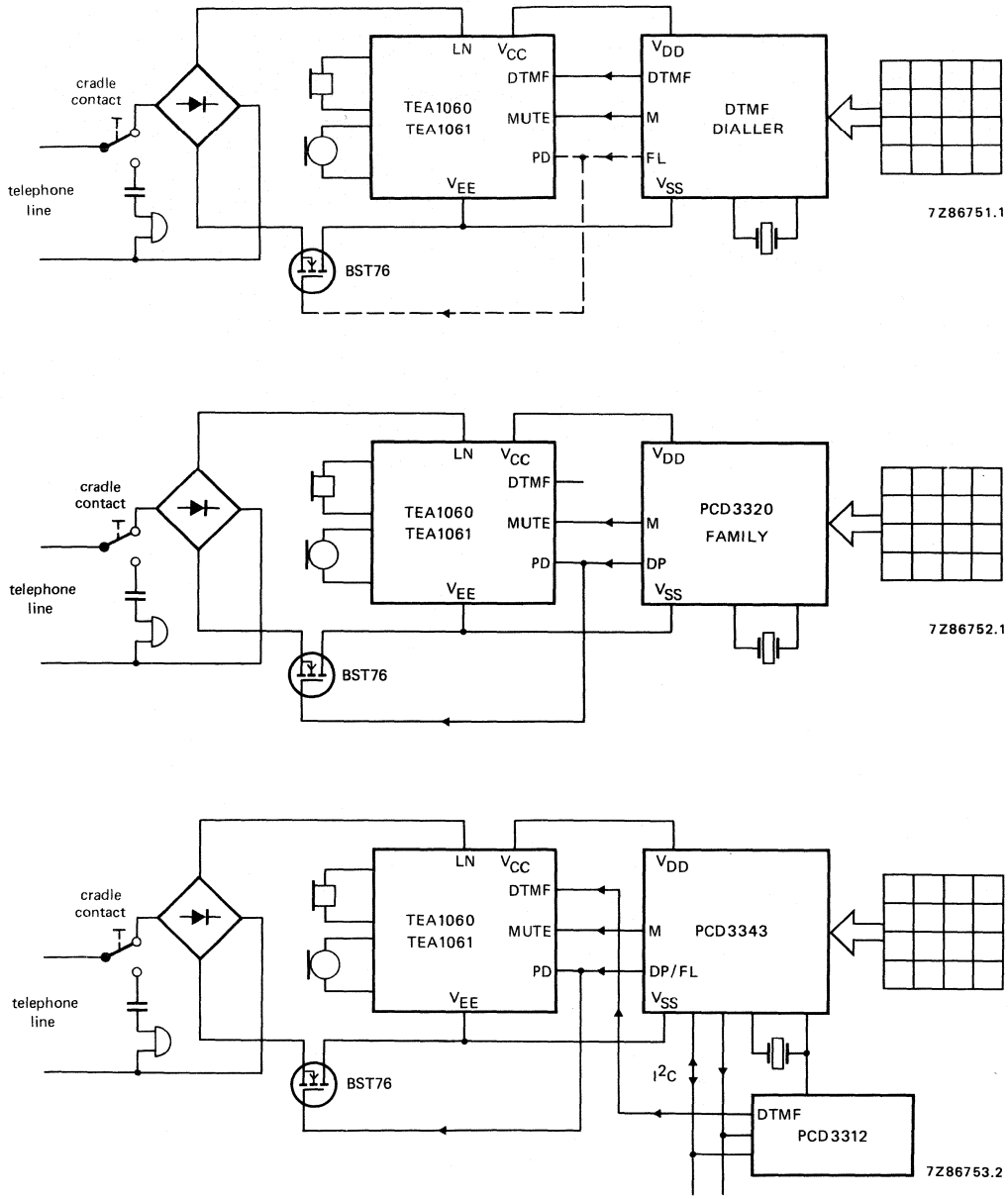


Fig. 11 Typical applications of the TEA1060 or TEA1061 (simplified). a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break). b) Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits. c) Dual-standerd (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE AND TRANSMIT LEVEL DYNAMIC LIMITING

GENERAL DESCRIPTION

The TEA1064 is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.7 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

Features

- Low DC line voltage; operates down to 1.7 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  unregulated supply, regulated line voltage;
  stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions

PACKAGE OUTLINES

TEA1064 : 20-lead DIL; plastic (SOT146).
TEA1064T: 20-lead mini-pack; plastic (SO20; SOT163A).

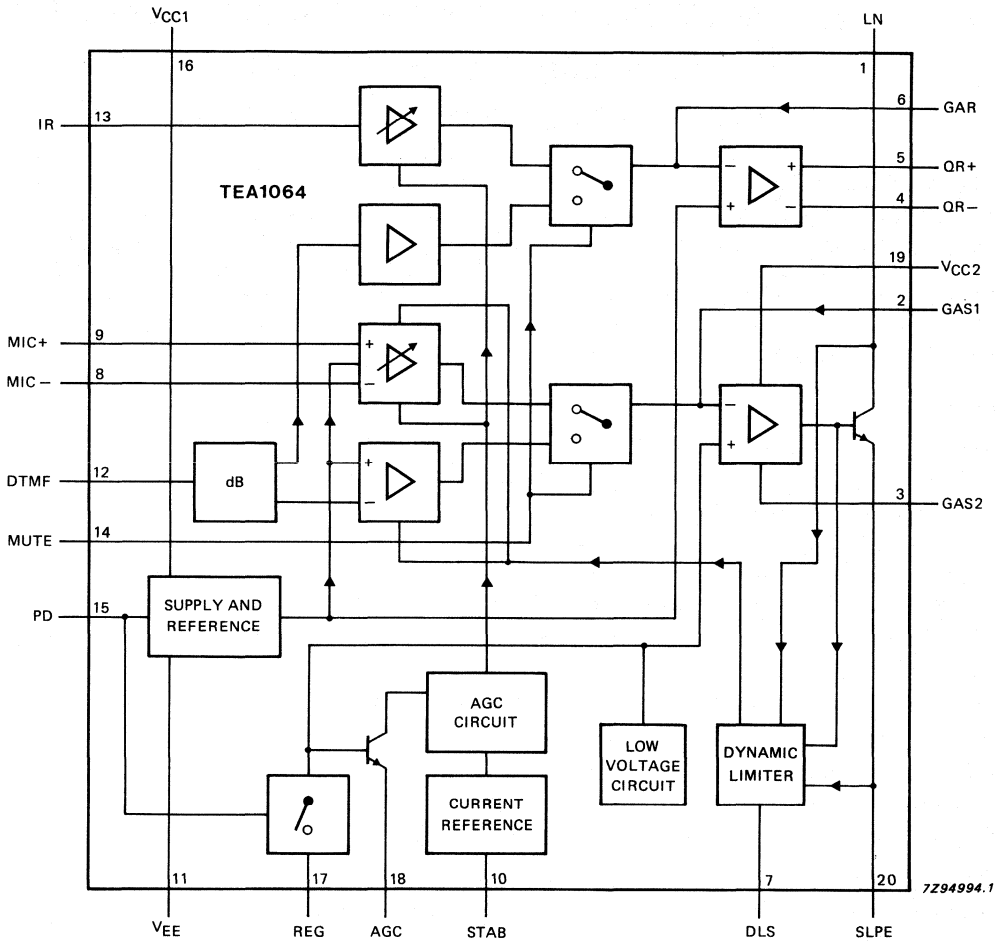


Fig. 1 Block diagram.

DEVELOPMENT DATA

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C
Line current operating range:						
normal operation		I_{line}	11	–	140*	mA
with reduced performance		I_{line}	2	–	11	mA
Internal supply current:						
power-down input LOW	V_{CC1} = 2.8 V	I_{CC1}	–	1.2	–	mA
power-down input HIGH	V_{CC1} = 2.8 V	I_{CC1}	–	60	–	μA
Voltage gain range:						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation:						
gain control range		G_v	–	6	–	dB
exchange supply voltage range		V_{exch}	36	–	60	V
exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω					
	I_{line} = 15 mA					
	I_p = 2 mA	$V_{LN(p-p)}$	–	3.95	–	V
	I_p = 4 mA	$V_{LN(p-p)}$	–	3.25	–	V
Regulated line voltage application						
	R15 = 0 Ω; R16 = 392 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 1.4 mA	V_p	2.5	–	–	V
	I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	V_p	2.9	–	–	V
DC line voltage	I_{line} = 15 mA					
	without $R_{REG-SLPE}$	V_{LN}	–	3.6	–	V
	$R_{REG-SLPE}$ = 20 kΩ	V_{LN}	–	4.57	–	V
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 0 to 4 mA	$V_{CC2-SLPE}$	3.05	3.3	3.55	V
DC line voltage	I_{line} = 15 mA					
	I_p = 2 mA	V_{LN}	–	4.5	–	V
	I_p = 4 mA	V_{LN}	–	5.2	–	V

* For TEA1064T the maximum line current depends on the heat dissipating qualities of the mounted device.

PINNING

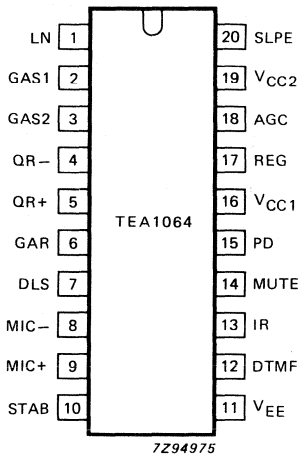


Fig. 2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	DLS	decoupling for transmit amplifier dynamic limiter
8	MIC−	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig. 3)

Power for the TEA1064 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig. 3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2\text{-}SLPE} = 3.3$ V (typ.)]. This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

- regulate directly the line voltage (stabilized $V_{LN\text{-}SLPE} = V_{CC2\text{-}SLPE}$)*;
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig. 3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 μF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig. 4. To increase the supply capabilities, the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$ or by decreasing the value of R16.

* The TEA1064 application with regulated line voltage is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.

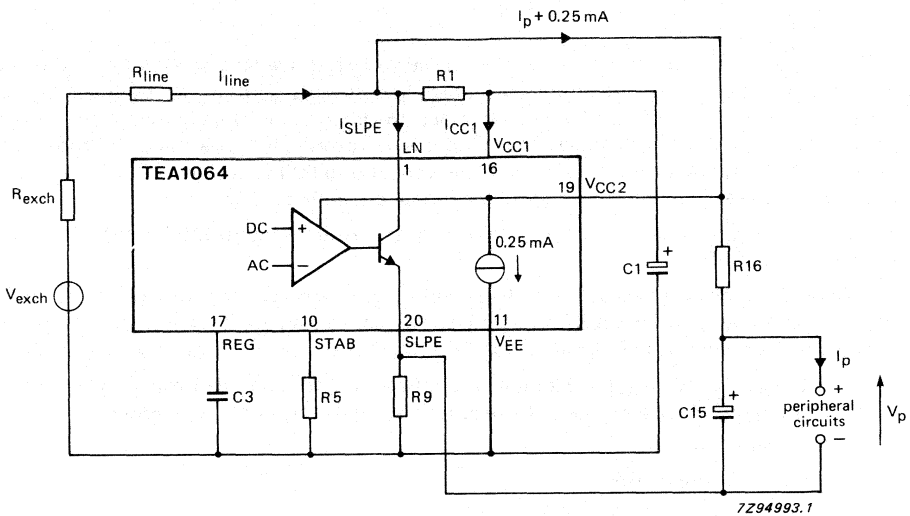


Fig. 3 Application with regulated line voltage (stabilized $V_{LN-SLPE}$). The voltage $V_{LN-SLPE}$ is fixed to V_{ref} = 3.3 ± 0.25 V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary). The line voltage V_{LN} = V_{ref} + ([I_{line} - 1.5 mA] x R9).

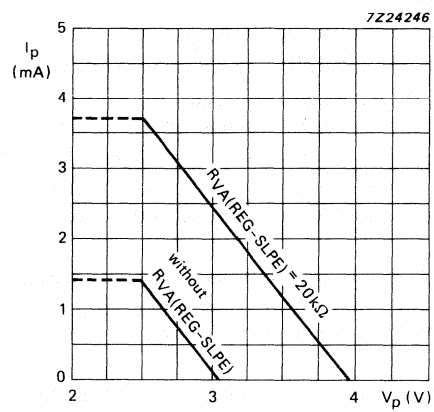


Fig. 4 Minimum supply current for peripherals (I_p) as a function of the peripheral supply voltage (V_p): I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Regulated line voltage (continued)

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN\text{-}SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig. 5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1064 also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1064 because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.2$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9)$$

$$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}] \times R9)$$

in which

V_{ref} = 3.3 V ± 0.25 V is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

V_{LN} = 3.57 ± 0.25 V at I_{line} = 15 mA

V_{LN} = 4.17 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 33 kΩ

V_{LN} = 4.57 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC1} + 0.25\ mA)$ and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig. 6.

The internal reference voltage $V_{CC2\text{-}SLPE}$ can be increased by external resistor $R_{VA(REG\text{-}SLPE)}$ connected between REG and SLPE. The supply voltage $V_{CC2\text{-}SLPE}$ is shown as a function of $R_{VA(REG\text{-}SLPE)}$ in Fig. 7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 9 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.7 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.7 V. At line currents below 9 mA (typ.), the circuit has limited sending and receiving levels.

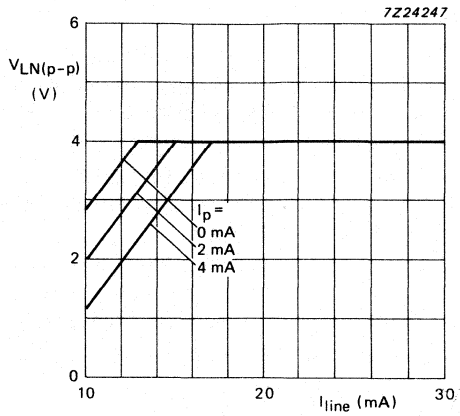


Fig. 5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

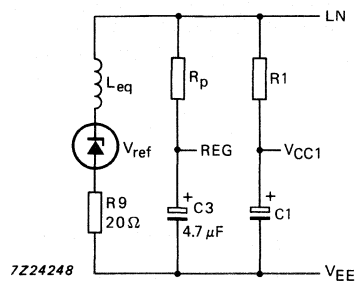


Fig. 6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN-SLPE}$:
R15 = 0 Ω
L_{eq} = C3 x R9 x R_p
R_p = 15.5 kΩ

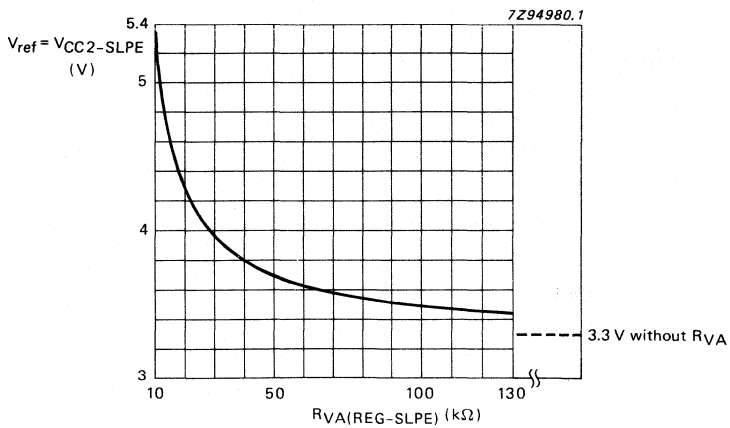


Fig. 7 Internal reference voltage $V_{CC2-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized supply application:

$$V_{LN} = V_{CC2-SLPE} + ([I_p + 0.25 \times 10^{-3}] \times R15) + ([I_{line} - 1.5 \times 10^{-3}] \times R9)\ V$$

In the unregulated supply application (R15 = 0 Ω):

$$V_{LN} = V_{CC2-SLPE} + ([I_{line} - 1.5 \times 10^{-3}] \times R9)\ V$$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage

The configuration shown in Fig. 8 provides a stabilized voltage across pins V_{CC2} and SPLE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2\text{-}SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\,\Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 μF; C3 = 470 nF. The ratio $R15/R16 \leqslant 8$ is for stable loop operation with sufficient phase margin, and $R15/R16 \geqslant 6$ is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different (further information is given in the TEA1064 Application Report*).

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig. 9, the curve parameter is the peripheral supply current (I_p). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results (these are described in the TEA1064 Application Report*).

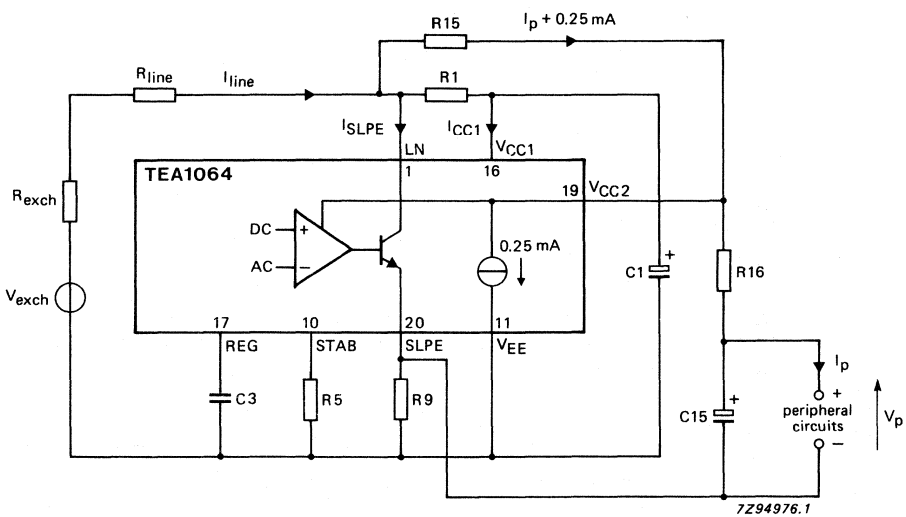


Fig. 8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

* Supplied on request.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3}] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}] \times R9)$$

in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.3 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)

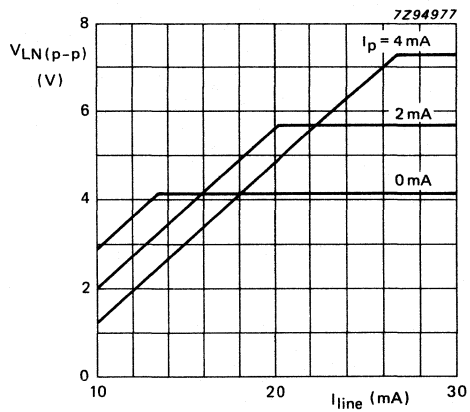


Fig. 9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω. As different values of R15 and R16 are allowed, different curves would then apply.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_p with R15 as a parameter is shown in Fig. 10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig. 8) is shown in Fig. 11.

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage (continued)

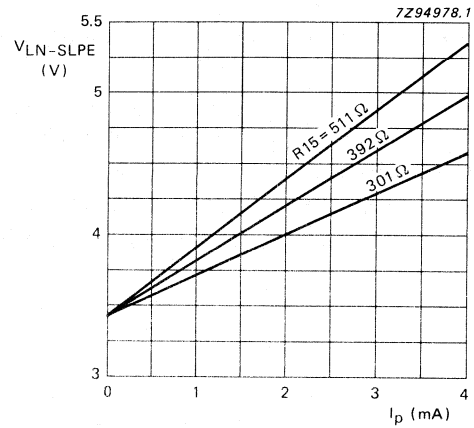
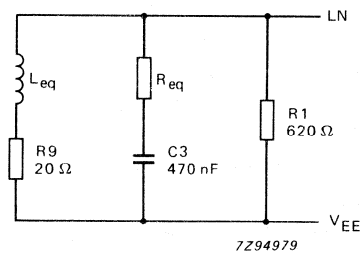


Fig. 10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2-SLPE}$ = 3.3 V (R_{VA} not connected). $V_{CC2-SLPE}$ can be adjusted between approximately 3.3 and 4.3 V by changing the value of R_{VA}, this results in a parallel-shift of the curves.
The total voltage drop $V_{LN} \approx V_{LN-SLPE} + ([I_{line} - 1.5\ mA] \times R9)$.



$$R_{eq} = R_p \left(\frac{R15}{R16} + 1\right)$$

$$L_{eq} = C3 \times R9 \times R_{eq}$$
with R_p = 15.5 kΩ

Fig. 11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1064 has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig. 12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.

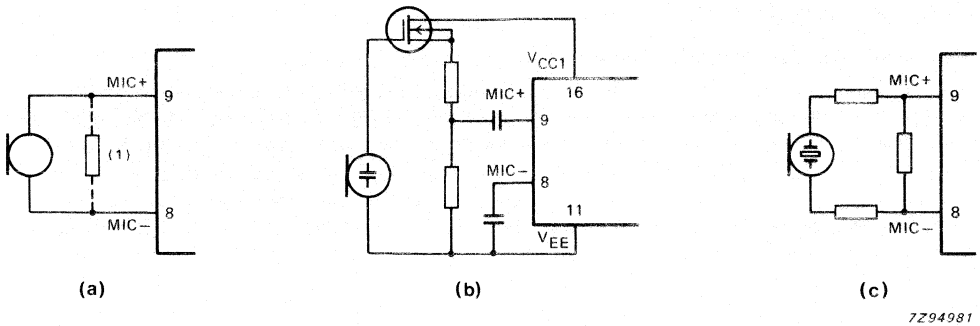


Fig. 12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (sending) pin DLS

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined by the capacitor connected to DLS (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.

Fig. 13 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_p$ as a parameter.

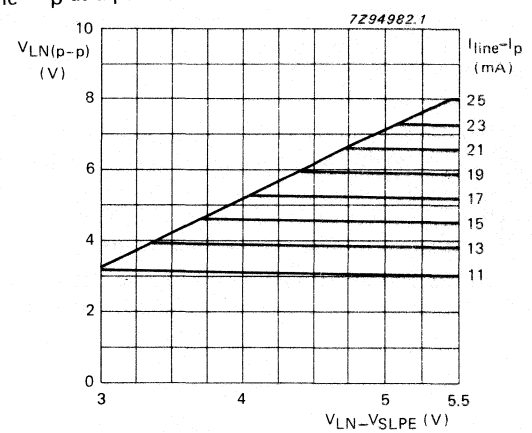


Fig. 13 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig. 14). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

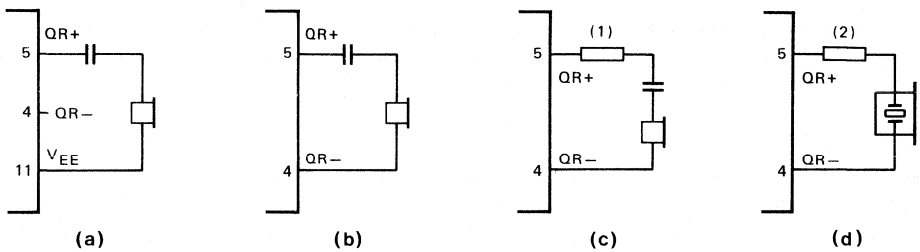


Fig. 14 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig. 15 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

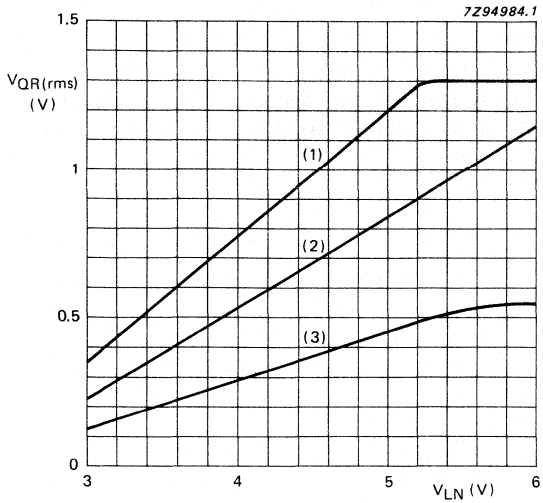


Fig. 15 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter.
valid for both supply options;
THD = 2%; I_{line} = 15 mA.
Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6 dB; this corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig. 16 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum gain.

DEVELOPMENT DATA

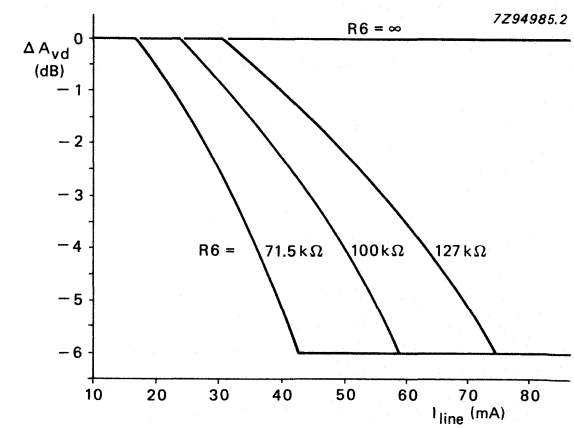


Fig. 16 Variation of amplification as a function of line current with R6 as a parameter; R9 = 20 Ω.

* Value to be fixed.

FUNCTIONAL DESCRIPTION (continued)

Automatic gain control input AGC (continued)

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	90.9	71.5	X	X
	48	127	100	82.5	71.5
	60	X	X	105	90.9

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

The MUTE function is operational down to V_{LN} = 2.8 V (V_{CC1} = 2.1 V). It is not possible to enable the DTMF amplifier for $V_{LN} < 2.8$ V, in this way the optimum performance of the speech amplifiers is guaranteed under extremely low voltage conditions (parallel operation). The speech amplifiers can be disabled by means of the MUTE function down to V_{LN} = 1.7 V.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 26 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE.
These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.2 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 17). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$

b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; $k = (R8/R1)$.

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| \ll R3$ to fulfill condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 17 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig. 18). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.)

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

Side-tone suppression (continued)

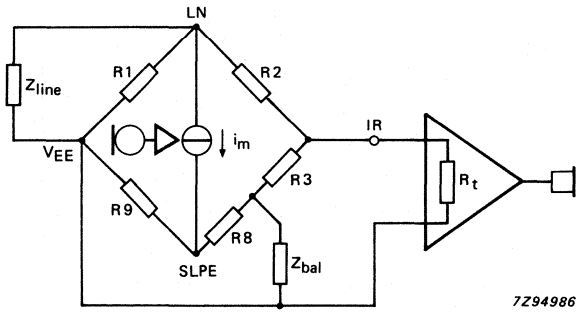


Fig. 17 Equivalent circuit of TEA1060 family anti-side-tone bridge.

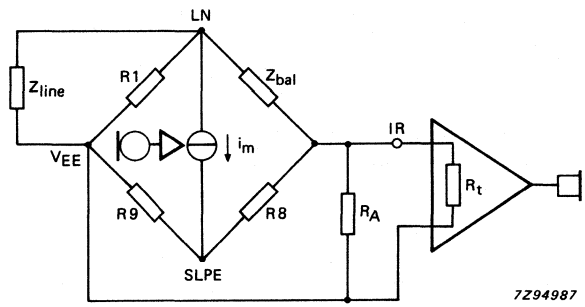


Fig. 18 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage; one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 23)	V_{LN}	–	28	V
Line current TEA1064		I_{line}	–	140	mA
Line current TEA1064T		I_{line}	–	83*	mA
Input voltage on pins other than LN and V_{CC2}		V_i	$V_{EE}-0.7$	$V_{CC1}+0.7$	V
Total power dissipation		P_{tot}	see Figs 19 and 20		
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

* Calculated for maximum T_{amb} = 75 °C and a thermal resistance of 120 K/W; the value depends mostly on the maximum required T_{amb} and on the heat dissipating capabilities of the mounted device (see Fig. 20).

THERMAL RESISTANCE

From junction to ambient in free air

TEA1064	$R_{th\ j\text{-}a}$	typ.	70	K/W
TEA1064T mounted on ceramic substrate 50 x 50 x 0,7 mm	$R_{th\ j\text{-}a}$	typ.	120	K/W

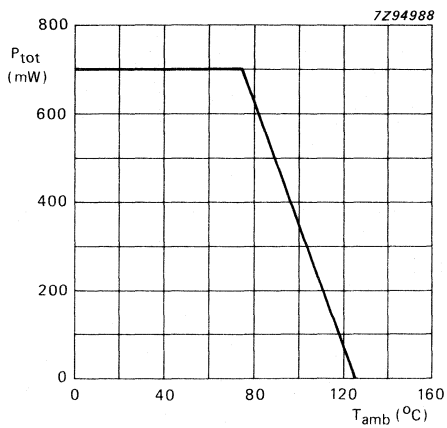


Fig. 19 TEA1064 power derating curve.

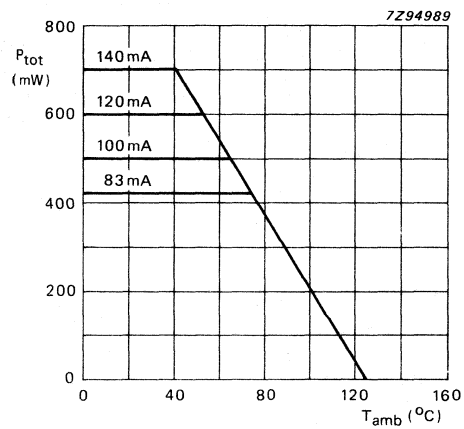


Fig. 20 TEA1064T power derating curve.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuit of Fig. 21 or 22); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between V_{CC2} and SLPE	I_{line} = 15 mA I_p = 0; 4 mA					
R_{VA} not connected		$V_{CC2-SLPE}$	3.05	3.3	3.55	V
Variation with temperature	I_{line} = 15 mA	$\frac{\Delta V_{CC2-SLPE}}{\Delta T}$	−4	−2	0	mV/K
Variation with line current referred to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2-SLPE}$	−	+3	−	mV
With R_{VA} connected between REG and SLPE	R_{VA} = 33 kΩ	$V_{CC2-SLPE}$	3.6	3.9	4.2	V
	R_{VA} = 20 kΩ	$V_{CC2-SLPE}$	3.95	4.3	4.65	V
DC line voltage: voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_p = 0 mA	V_{LN}	3.4	3.7	4.0	V
	I_p = 2 mA	V_{LN}	4.2	4.5	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.2	5.5	V
at I_{line} = 100 mA	I_p = 2 mA	V_{LN}	−	6.2	7.0	V
at I_{line} = 140 mA	I_p = 2 mA	V_{LN}	−	7.0	7.8	V
Voltage drop under low current conditions	I_p = 0 mA					
	I_{line} = 2 mA	V_{LN}	−	1.7	−	V
	I_{line} = 4 mA	V_{LN}	*	2.0	*	V
	I_{line} = 7 mA	V_{LN}	*	2.9	*	V
	I_{line} = 11 mA	V_{LN}	*	3.6	*	V
Internal supply current I_{CC1}: current into pin V_{CC1}	V_{CC1} = 2.8 V					
	PD = LOW	I_{CC1}	−	1.2	1.5	mA
	PD = HIGH	I_{CC1}	−	60	82	μA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Common mode rejection ratio		CMRR	–	82	–	dB
Voltage gain (see Fig. 21)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Variation of G_v with frequency, referred to 0,8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	−0.5	± 0.1	+ 0.5	dB
Variation of G_v with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.8	20.7	24.6	kΩ
Voltage gain (see Fig. 21)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	25	26	27	dB
Variation of G_v with frequency, referred to 0,8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	−0.5	± 0.1	+ 0.5	dB
	f = 697 and 1633 Hz	$\Delta G_v/\Delta f$	−0.2	± 0.05	+ 0.2	dB
Variation of G_v with temperature, referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier, gain adjustment range		ΔG_v	−8	–	+ 0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; I_p = 0 mA; $V_{i(rms)}$ = 3.6 mV	$V_{LN(p-p)}$	3.6	4.1	4.5	V
Total harmonic distortion	V_i = 3.6 mV + 10 dB	THD	–	1.2	2.0	%
	V_i = 3.6 mV + 15 dB	THD	–	2.8	10.0	%
Output voltage swing (peak-to-peak value)	V_i = 3.6 mV + 10 dB					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_p = 0 mA; I_{line} = 7 mA	$V_{LN(p-p)}$	–	1.8	–	V
	I_p = 0 mA; I_{line} = 4 mA	$V_{LN(p-p)}$	–	0.8	–	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
LN output (continued)						
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} jumps from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	17	21	25	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig. 22; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	30	31	32	dB
differential; R_T = 600 Ω		G_v	36	37	38	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	–0.5	–0.2	0	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_p = 0 mA	$V_{o(rms)}$	0.18	0.23	–	V
	I_p = 2 mA	$V_{o(rms)}$	0.30	0.38	–	V
differential; R_T = 450 Ω	I_p = 0 mA	$V_{o(rms)}$	0.34	0.43	–	V
	I_p = 2 mA	$V_{o(rms)}$	0.58	0.68	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_p = 0 mA	$V_{o(rms)}$	0.50	0.63	–	V
	I_p = 2 mA	$V_{o(rms)}$	0.8	1.0	–	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (RMS value)	I_p = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open					
	single-ended; R_T = 300 Ω	$V_{no(rms)}$	–	45	–	μV
	differential; R_T = 600 Ω	$V_{no(rms)}$	–	90	–	μV
Noise output voltage (RMS value)	in circuit of Fig. 22; S1 in position 2; single-ended; R_T = 300 Ω					
	R7 = 68 kΩ	$V_{no(rms)}$	–	100	–	μV
	R7 = 24.9 kΩ	$V_{no(rms)}$	–	65	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	−11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-on	MUTE = HIGH	$-\Delta G_v$	–	100	–	dB
Voltage gain from input DTMF-SLPE to QR+ output with mute on	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	*	−18	*	dB

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR– (pins 4, 5) and the gain from MIC+, MIC– (pins 8, 9) to LN (pin 1)	R6 = 100 kΩ (between pins 18 and 11)					
gain control range with respect to I_{line} = 15 mA	I_{line} = 70 mA	$-\Delta G_v$	*	6.1	*	dB
Highest line current for maximum gain		I_{line}	–	24	–	mA
Lowest line current for minimum gain		I_{line}	–	61	–	mA
Change of gain between I_{line} = 15 and 35 mA		$-\Delta G_v$	*	1.4	*	dB

* Value to be fixed.

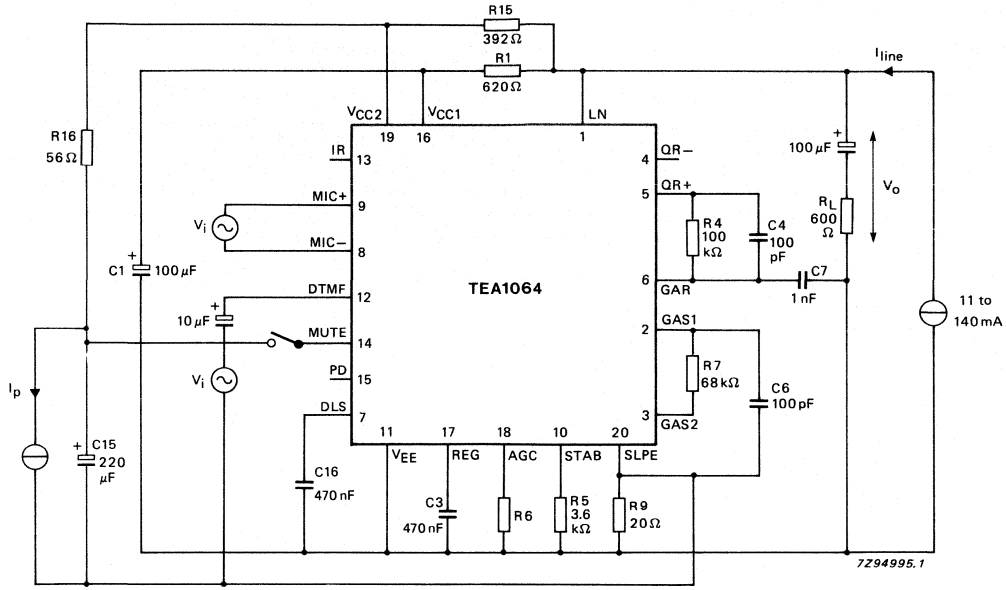


Fig. 21 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_V) is defined as 20 log$|V_o/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

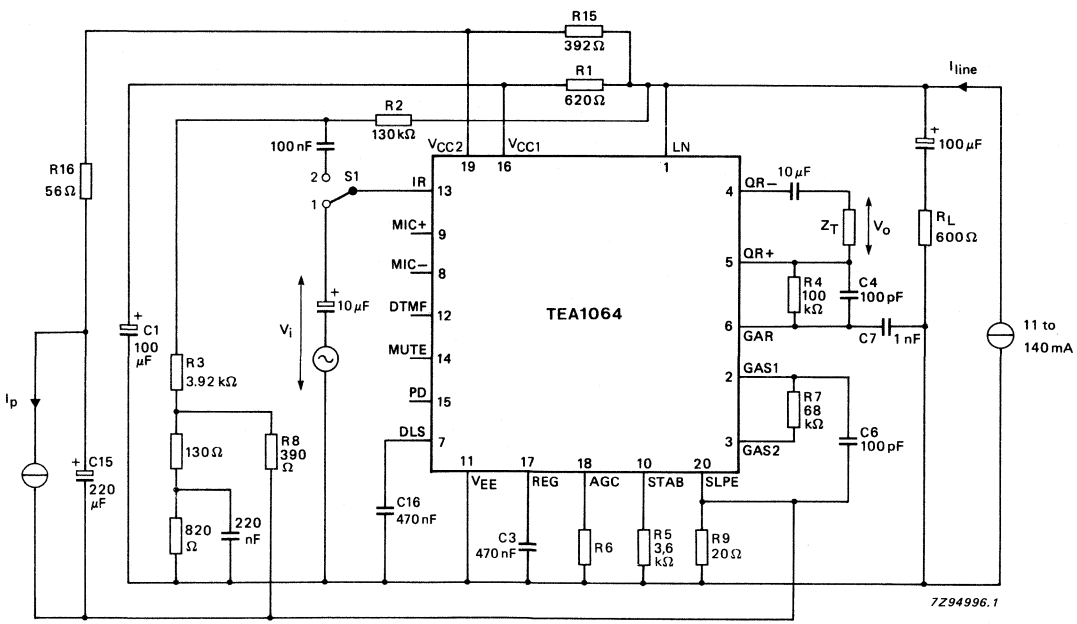


Fig. 22 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_V) is defined as 20 log$|V_o/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 23 and some typical applications are shown in Figs 24, 25 and 26.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN\text{-}SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is the same as that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2\text{-}SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

DEVELOPMENT DATA

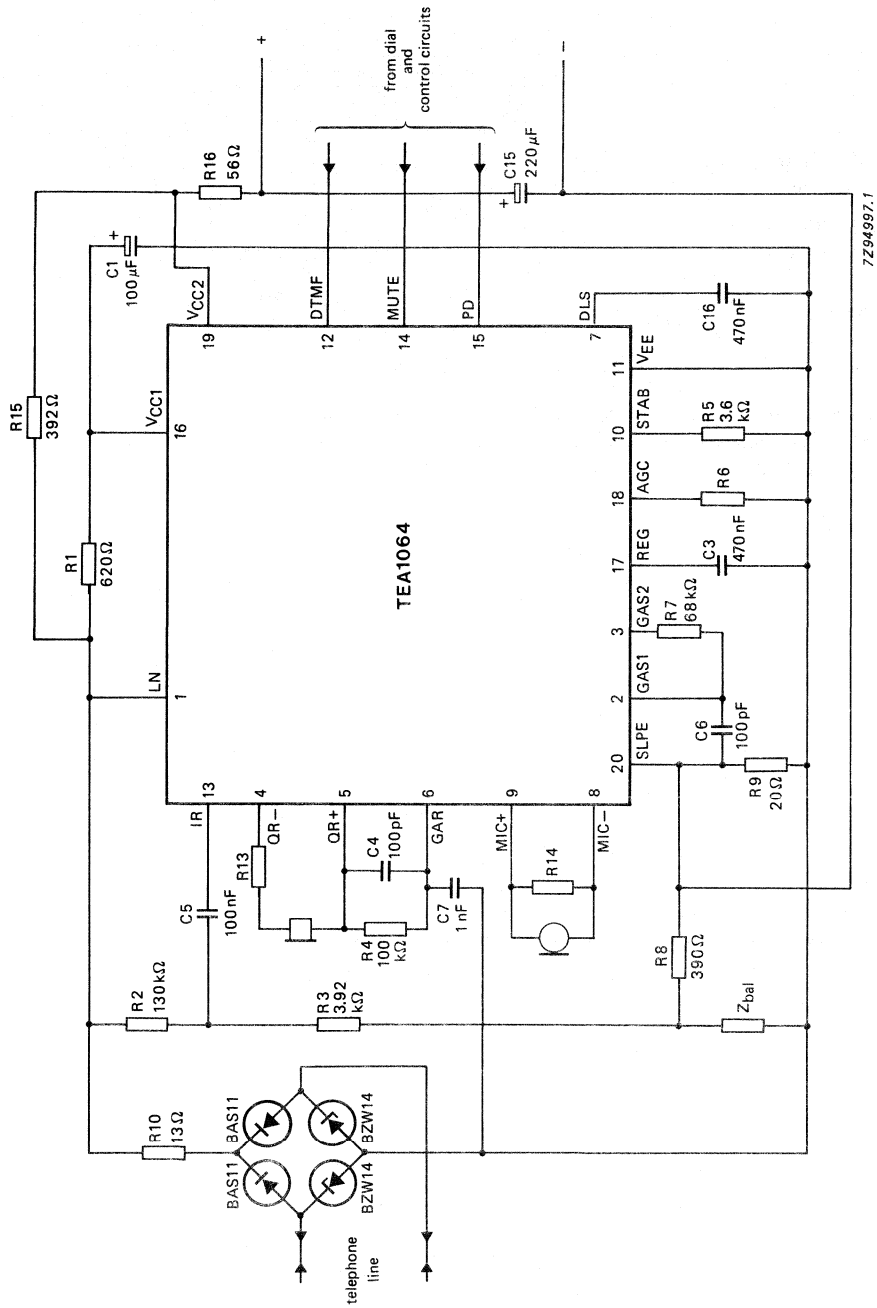


Fig. 23 Basic application of the TEA1064 with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

- R15 must be short-circuited;
- the value of R16 is changed to 392 Ω;
- the value of C3 is changed to 4.7 μF.

APPLICATION INFORMATION (continued)

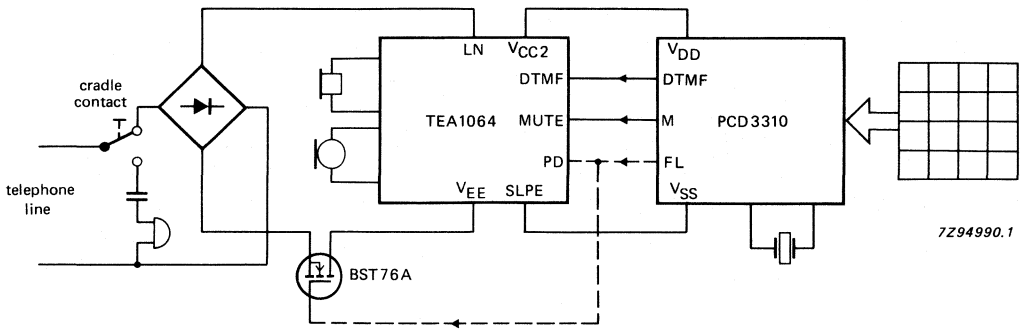


Fig. 24 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064 with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

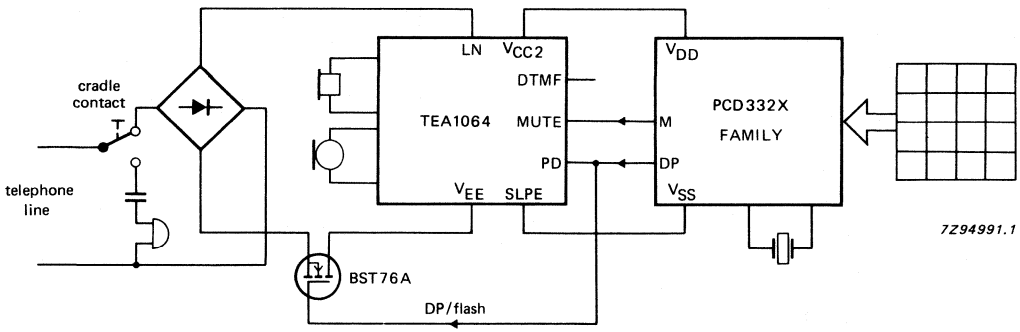


Fig. 25 Typical pulse dial set application circuit (simplified) showing the TEA1064 with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

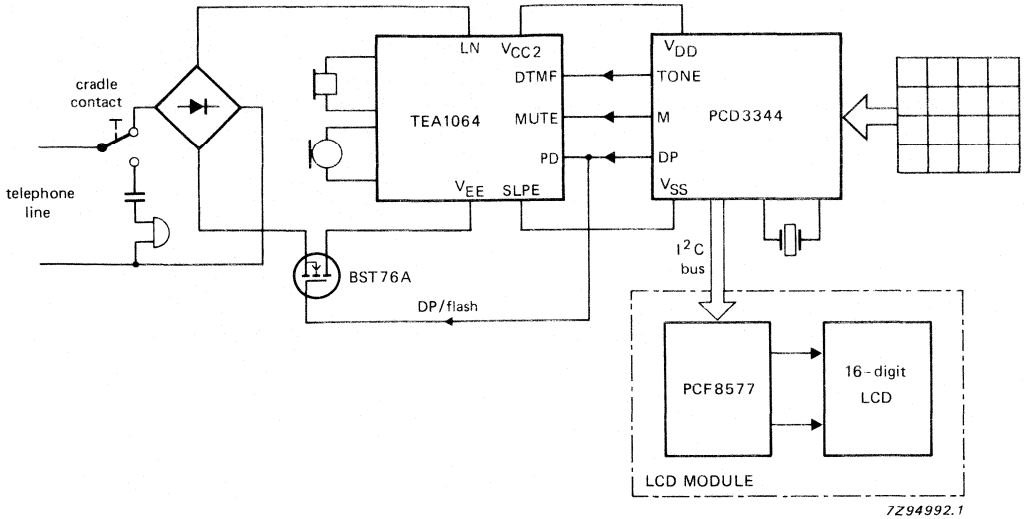


Fig. 26 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064 and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit performing all speech, and line interface functions required in fully electronic telephone sets. The circuit internally performs electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ.	4.45	V
Line current operating range	I_{line}		10 to 100	mA
Internal supply current				
power down input LOW	I_{CC}	typ.	1	mA
power down input HIGH	I_{CC}	typ.	55	μA
Supply voltage for peripherals				
I_{line} = 15 mA; mute input HIGH				
Ip = 1,2 mA	V_{CC}	min.	2,8	V
Ip = 1,7 mA	V_{CC}	min.	2,5	V
Voltage amplification range microphone amplifier				
low impedance inputs (pins 9 and 7)	A_{vd}		44 to 60	dB
high impedance inputs (pins 10 and 8)	A_{vd}		30 to 46	dB
receiving amplifier	A_{vd}		17 to 39	dB
Line loss compensation				
Amplification control range	ΔA_{vd}	typ.	5,9	dB
Exchange supply voltage range	V_{exch}		24 to 60	V
Exchange feeding bridge resistance range	R_{exch}		400 to 1000	Ω
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

PACKAGE OUTLINE

20-lead MINI-PACK; plastic (SO20; SOT163A).

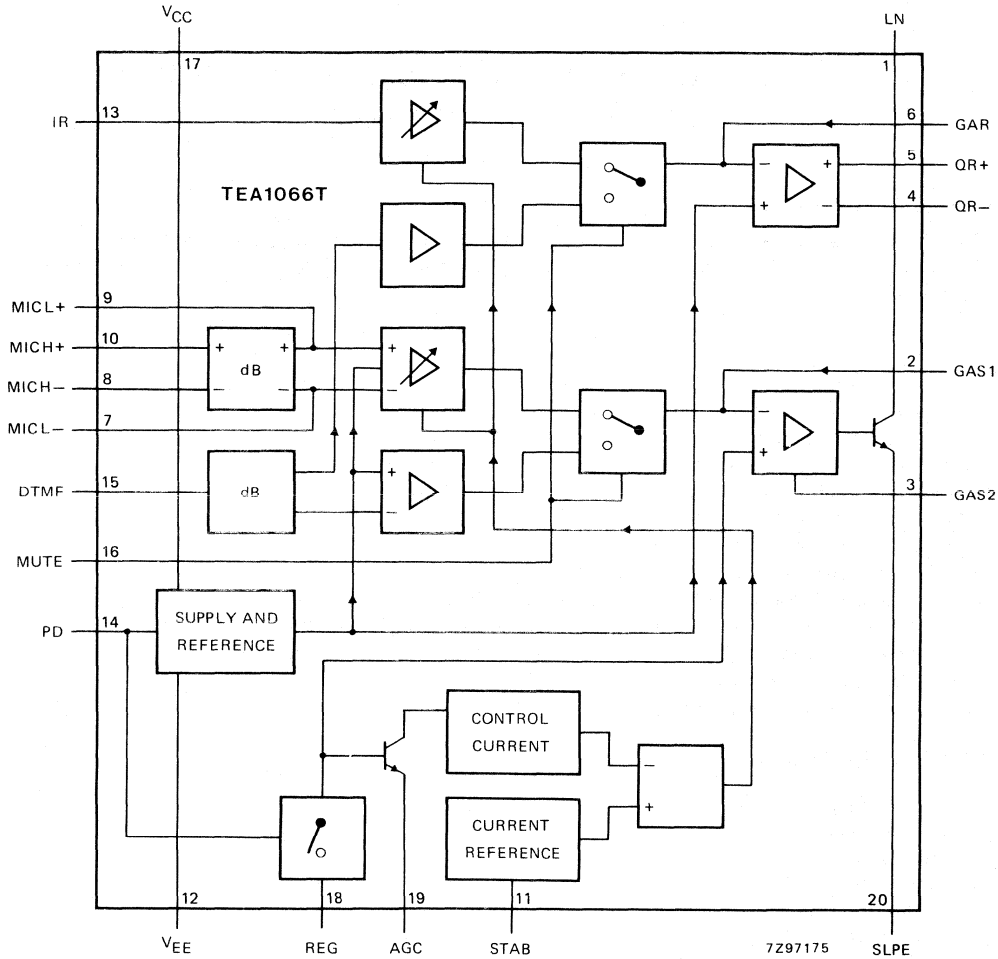


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators.

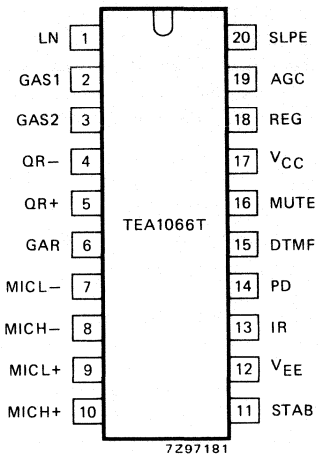


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment transmitting amplifier
3	GAS2	gain adjustment transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment receiving amplifier
7	MICL–	inverting microphone input, low impedance
8	MICH–	inverting microphone input, high impedance
9	MICL+	non-inverting microphone input, low impedance
10	MICH+	non-inverting microphone input, high impedance
11	STAB	current stabilizer
12	V_{EE}	negative line terminal
13	IR	receiving amplifier input
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (d.c. resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself, about 1 mA, plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5 \times 10^{-3} - I_p) \times R9$. V_{ref} being an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing R9 will have influence on microphone gain, gain control characteristics, side tone and maximum output swing on LN.

FUNCTIONAL DESCRIPTION (continued)

Under normal conditions $I_{SLPE} \geqslant I_{CC} + 0{,}5\ mA + I_p$. The static behaviour of the circuit then equals a 4,2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This R_{VA} connected between LN and REG (pins 1 and 16) will decrease the internal reference voltage. R_{VA} connected between REG and SLPE (pins 16 and 18) will increase the internal reference voltage.

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 4 shows this current for $V_{CC} > 2{,}2$ V and > 3 V. 3 volt being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MICL+, MICH+, MICL− and MICH− and gain adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL− inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Input impedance is 8,2 kΩ (2 x 4,1 kΩ) and its voltage amplification is typ. 52 dB. The MICH+ and MICH− inputs are intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40,8 kΩ (2 x 20,4 kΩ) and its voltage amplification is typical 38 dB.
The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifiers can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25,5 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezo-electric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C6 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off' frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| < R3$.
To obtain optimum side tone suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$$

where k is a scale factor; k = (R8/R1).

Scale factor k (value of R8) must be chosen to meet the following criteria:
- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

FUNCTIONAL DESCRIPTION (continued)

The anti-side-tone network as used in the standard application (Fig. 10) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage (d.c.)	V_{LN}	max.	12	V
Repetitive line voltage during switch-on or line interruption	V_{LN}	max.	13,2	V
Repetitive peak line voltage t_p/P = 1 ms/5 s; R_{lim} = 13 Ω; R_{10} = 13 Ω; R_g = 20 Ω (see Fig. 10)	$V_{LN(RM)}$	max.	28	V
Line current	I_{line}	max.	100	mA
Voltage on all other pins	V_i	max.	V_{CC} + 0,7	V
	$-V_i$	max.	0,7	V
Total power dissipation	P_{tot}	max.	470	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

CHARACTERISTICS

$I_{line} = I_1$ = 10 to 100 mA; V_{EE} = 0 V; f = 800 Hz; R9 = 20 Ω; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 17)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{1-12}	3,95	4,25	4,55	V
at I_{line} = 15 mA	V_{1-12}	4,25	4,45	4,65	V
at I_{line} = 100 mA	V_{1-12}	5,40	6,10	7,00	V
Voltage drop variation					
with temperature at I_{line} = 15 mA	ΔV_{LN}	−4	−2	0	mV/K
Voltage drop over circuit at I_{line} = 15 mA;					
$R_{VA} = R_{1-16}$ = 68 kΩ	V_{LN}	3,50	3,80	4,05	V
$R_{VA} = R_{18-20}$ = 39 kΩ	V_{LN}	4,70	5,0	5,30	V
Supply current (pin 17)					
PD (pin 14) = LOW; V_{CC} = 2,8 V	I_{CC}	–	0,96	1,3	mA
PD (pin 14) = HIGH; V_{CC} = 2,8 V	I_{CC}	–	55	82	μA
Microphone inputs MICL+ and MICL−; MICH+ and MICH−					
Input impedance					
MICL+ (pin 9); MICL− (pin 7)	$\lvert z_{is} \rvert$	3,3	4,1	4,9	kΩ
MICH+ (pin 10); MICH− (pin 8)	$\lvert z_{is} \rvert$	16,5	20,4	24,3	kΩ
Common-mode rejection ratio	k_{CMR}	–	82	–	dB
Voltage amplification					
at I_{line} = 15 mA; R7 = 68 kΩ					
MICL+; MICL−	A_{vd}	51	52	53	dB
MICH+; MICH−	A_{vd}	37	38	39	dB
Variation with frequency					
at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Variation with temperature at					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Dual-tone multi-frequency input DTMF (pin 15)					
Input impedance	$\lvert z_{is} \rvert$	16,8	20,7	24,6	kΩ
Voltage amplification (pin 15 to pin 1)					
at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	24,5	25,5	26,5	dB
Variation with frequency					
at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	+ 0,2	+ 0,5	dB
Variation with temperature at					
I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+ 8	dB
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,9	2,3	–	V
d_{tot} = 10 %	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR (pin 13)					
Input impedance	$\lvert z_{is} \rvert$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)					
Output impedance; single-ended	$\lvert z_{os} \rvert$	–	4	–	Ω
Voltage amplification from pin 13 to pins 4 or 5 I_{line} = 15 mA; R4 = 100 kΩ;					
single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Amplification variation at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	−0,5	± 0,2	+ 0,5	dB
Amplification variation I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,2	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive; R4 = 100 kΩ					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,30	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF; R_{series} = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open psophometrically weighted (P53 curve)					
single-ended R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)					
Amplification variation with R4 connected between pin 6 and pin 5; receiving amplifier	ΔA_{vd}	−8	–	+ 8	dB

parameter	symbol	min.	typ.	max.	unit
MUTE input (pin 16)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	I_{IL}	–	–	0,3	V
Input current	I_{14}	–	5	10	μA
Reduction of voltage amplification from MICL+ (pin 9) and MICL– (pin 7) to LN (pin 1) at MUTE = HIGH	ΔA_{vd}	–	70	–	dB
Voltage amplification from DTMF to QR+ or QR– at MUTE = HIGH; R4 = 100 kΩ single-ended load R_L = 300 Ω	A_{vd}	–21	–19	–17	dB
Power-down input PD (pin 14)					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{14}	–	5	10	μA
Automatic gain control input AGC					
Controlling the gain from IR to QR+/QR– and the gain from MIC+/MIC– to LN R6 = 110 kΩ (between AGC and V_{EE}) amplification control range (I_{line} = 70 mA)	$-\Delta A_{vd}$	5,5	5,9	6,3	dB
Highest line current for maximum amplification	I_{line}	–	23	–	mA
Lowest line current for minimum amplification	I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA	$-\Delta A_{vd}$	1,0	1,5	2,0	dB

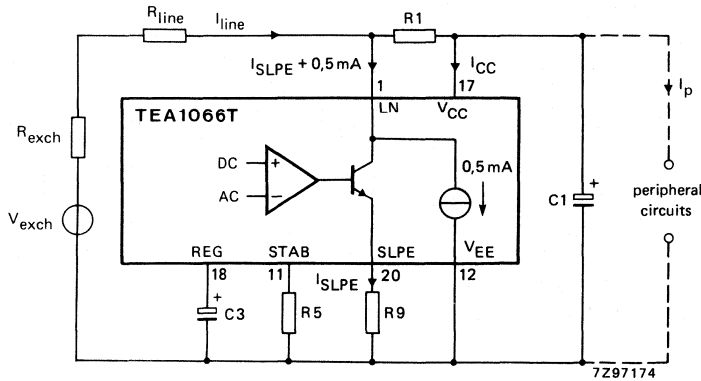


Fig. 3 Supply arrangement.

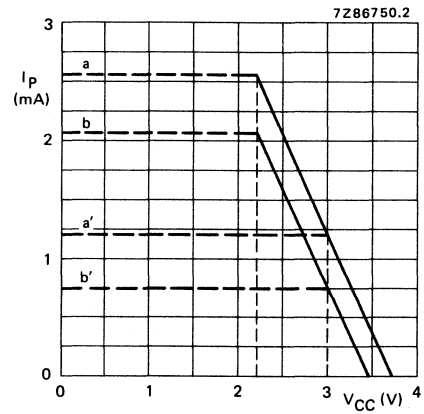


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).
I_{line} = 15 mA; V_{LN} = 4,45 V; R1 = 620 Ω and R9 = 20 Ω.
(a) = 2,55 mA; (b) = 2,1 mA; (a') = 1,2 mA and (b') = 0,75 mA.

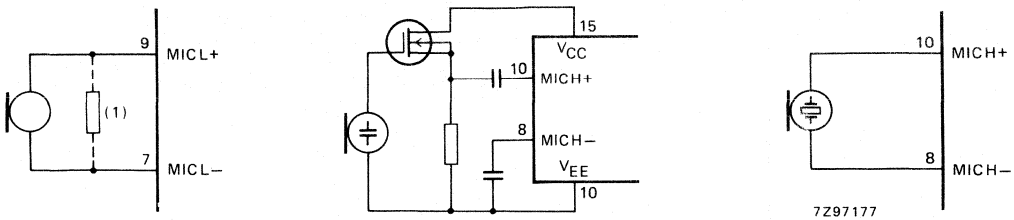


Fig. 5 Alternative microphone arrangements. (a) magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, (c) piezo-electric microphone.

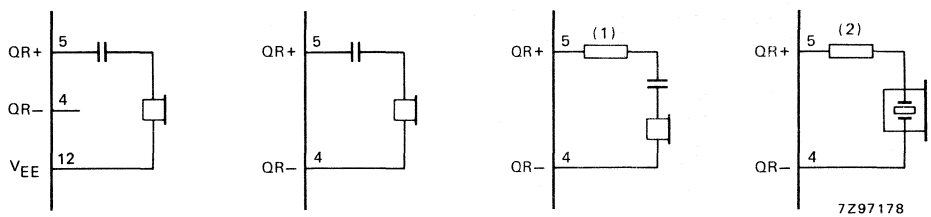


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

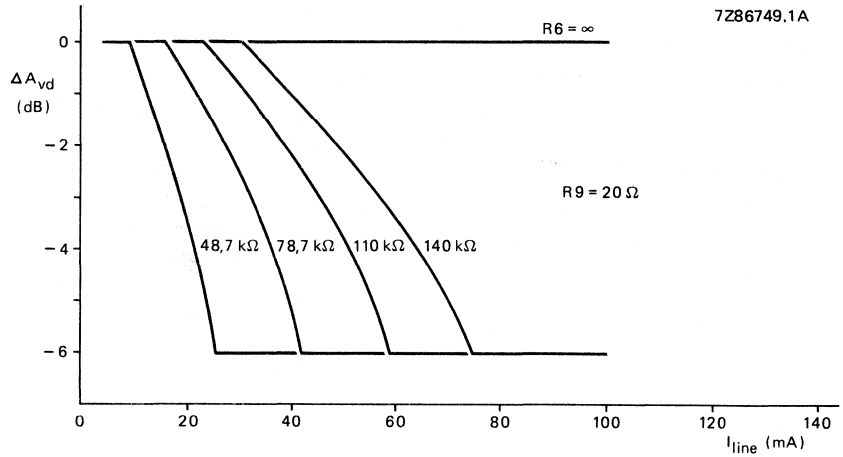


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

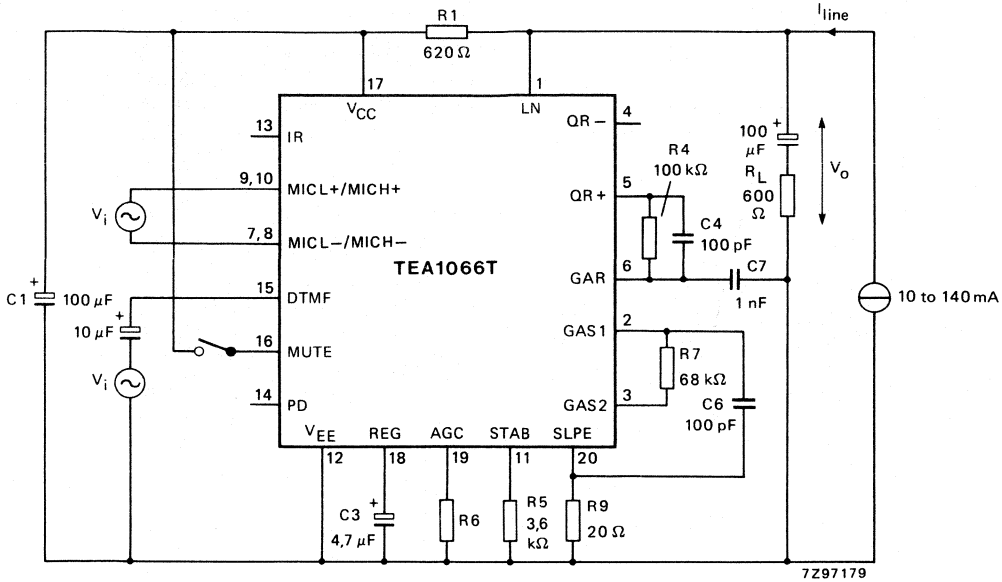


Fig. 8 Test circuit for defining voltage amplification of MICL+, MICL−, MICH+, MICH− and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MICL+; MICL− or MICH+ and MICH− the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

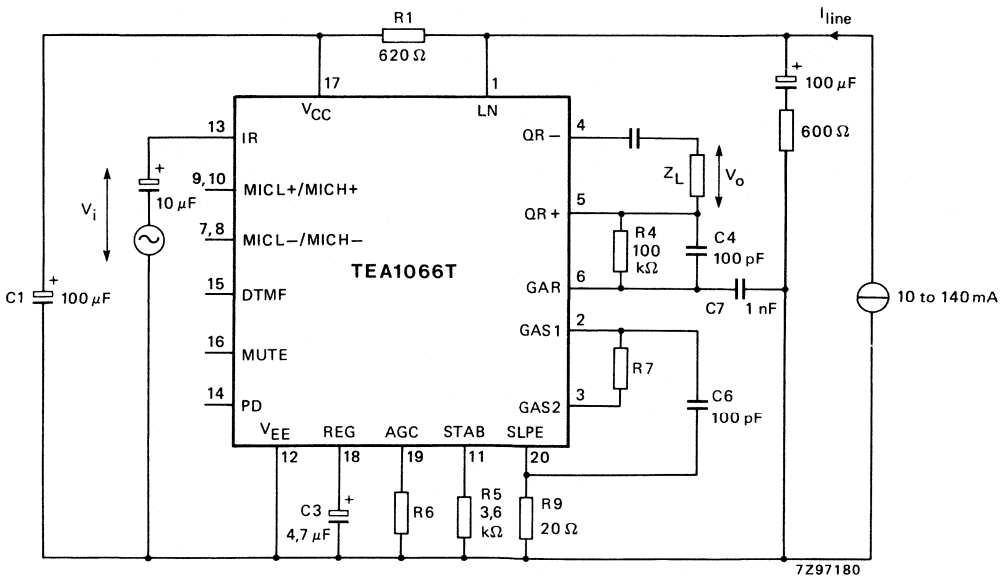


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

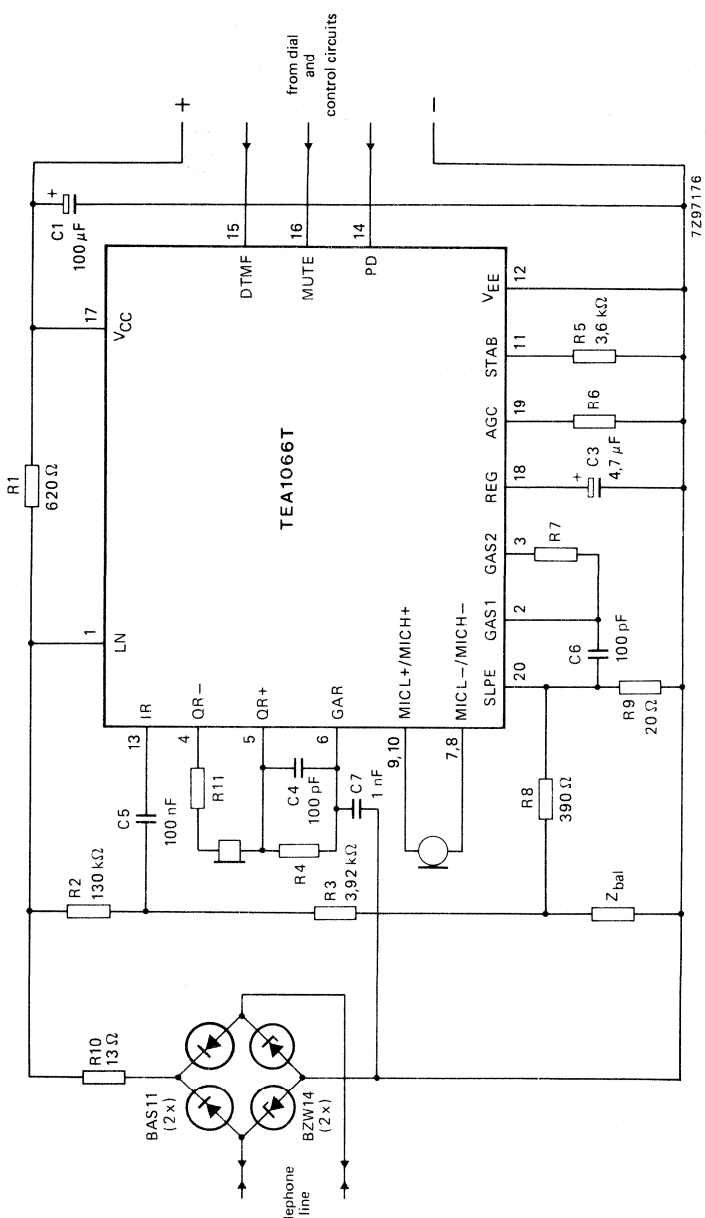
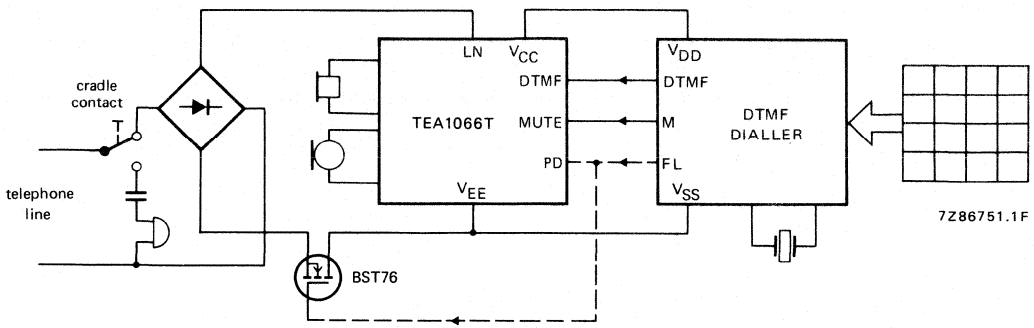
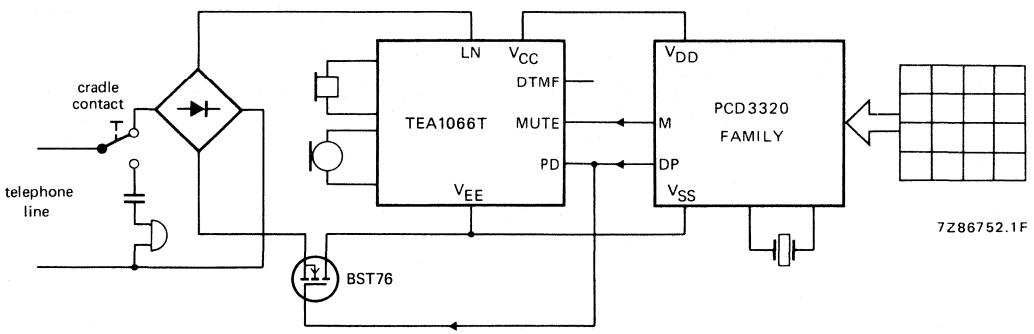


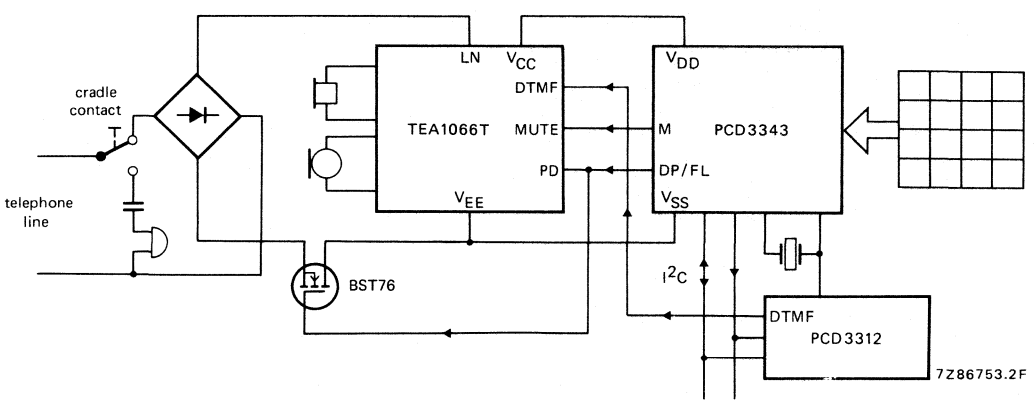
Fig. 10 Typical application of the TEA1066T, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.



(a)



(b)



(c)

Fig. 11 Typical applications of the TEA1066T (simplified). (a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).
b: Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

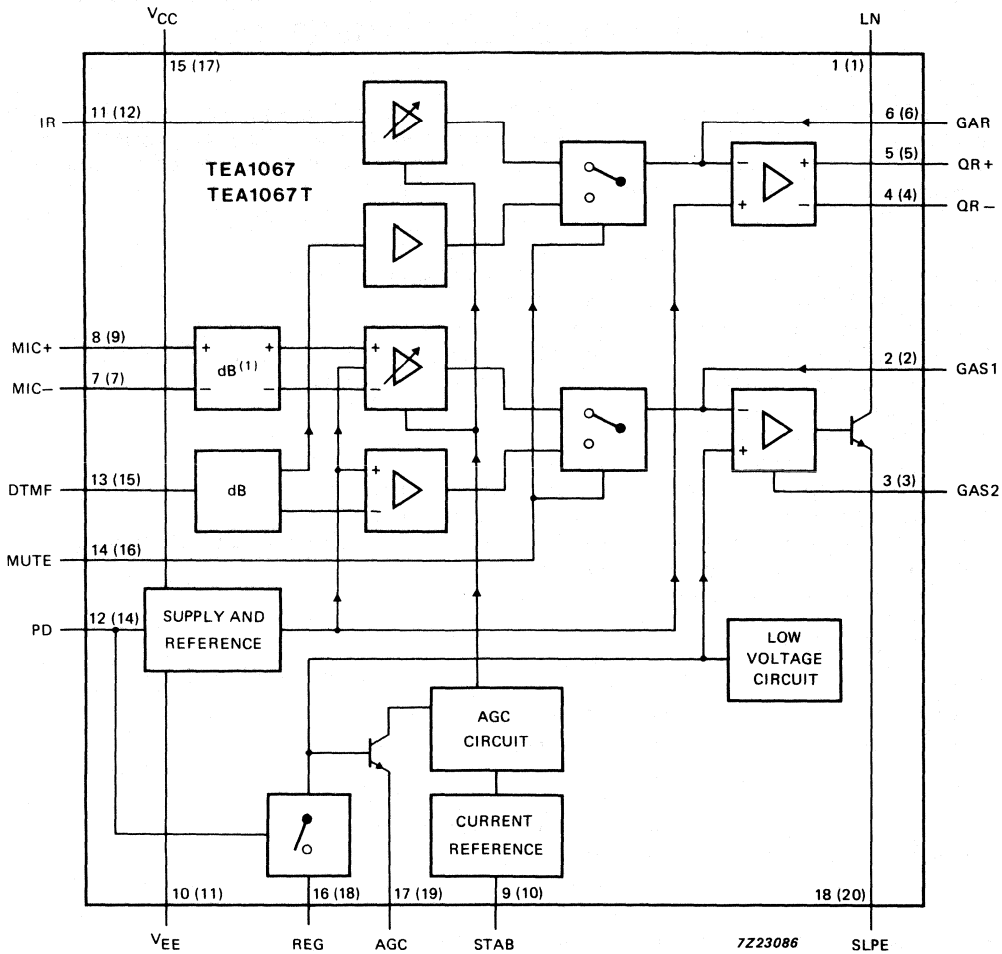
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	–	3.9	–	V
Line current operating range	normal operation					
	TEA1067	I_{line}	11	–	140	mA
	TEA1067T	I_{line}	11	–	100 *	mA
	with reduced performance	I_{line}	1	–	11	mA
Internal supply current	power down					
	input LOW	I_{CC}	-	1	–	mA
	input HIGH	I_{CC}	–	55	–	μA
Supply voltage for peripherals	I_{line} = 15 mA; I_p = 1.4 mA; mute input HIGH	V_{CC}	2.2	–	–	V
	I_{line} = 15 mA; I_p = 0.9 mA; mute input HIGH	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation gain control range		ΔG_v	–	5.9	–	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

* See note to the Ratings

PACKAGE OUTLINES

TEA1067: 18-lead DIL; plastic (SOT102).
TEA1067T: 20-lead mini-pack; plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1067T.

Fig. 1 Block diagram.

PINNING

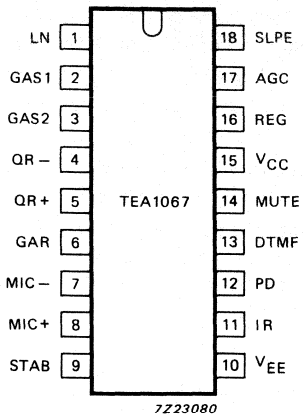


Fig. 2 (a) Pinning diagram for TEA1067 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

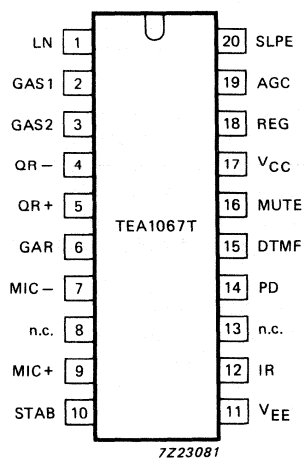


Fig. 2 (b) Pinning diagram for TEA1067T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment, receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1067 and its peripheral circuits is usually obtained from the telephone line. The supply voltage (V_{CC}) is derived from the line via a dropping resistor and regulated by the TEA1067. V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

The TEA1067 has an internal current stabilizer working at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 6). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

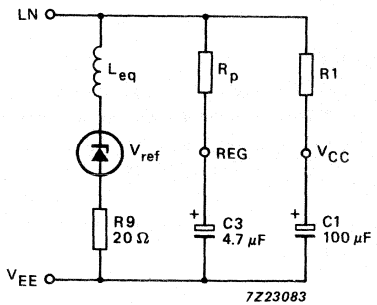
$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}) - I_p] \times R9$$

where; V_{ref} is an internally generated temperature compensated reference voltage of 3.6 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics side-tone and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5\text{ mA} + I_p$, the static behaviour of the circuit is that of a 3.6 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that the operation of more sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig. 7 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig. 14 (c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



R_p = 16.2 kΩ; the loading is provided by R_p, R9 and C3

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 11). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 8.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Gain of over 52 dB and up to 60 dB can be achieved but this increases the spread of V_{LN} and the minimum voltage (V_{LN} = 3.55 V) at 11 mA cannot be guaranteed. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligable clicking on the telephone outputs and line. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independently to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving Amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 9). IR to QR + gain is typically 31 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single end drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).
The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

FUNCTIONAL DESCRIPTION (continued)

Receiving Amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 20 and 39 dB with single-ended drive and between 26 and 45 dB with differential drive, to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 10 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R9 and Z_{bal}, (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line impedance at which the optimum suppression is present can be calculated by;
210 Ω + (1265 Ω//140 nF). This represents a 5 km line of 0.5 mm diameter, copper, twisted pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

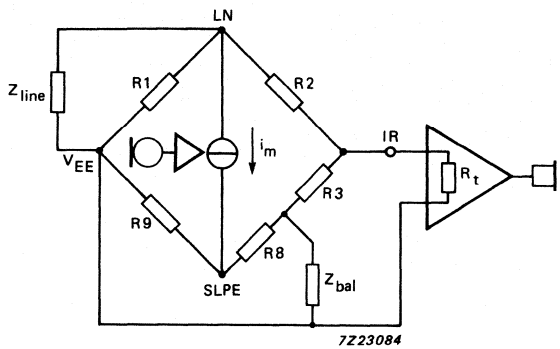


Fig. 4 Equivalent circuit of TEA1060 anti-sidetone bridge.

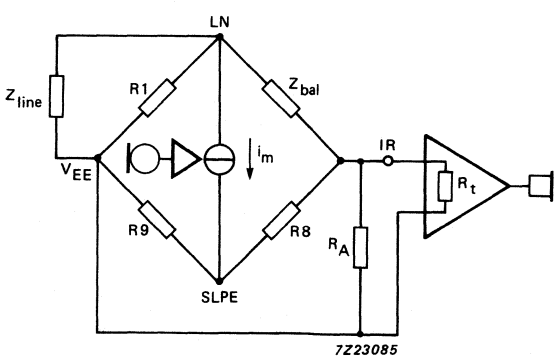


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage	continuous	V_{LN}	–	12	V
Repetitive line voltage	during switch-on or line interruption	V_{LN}	–	13.2	V
Repetitive peak line voltage	t_p/p = 1 ms/5 s R10 = 13 Ω; R9 = 20 Ω; see Fig. 13	V_{LN}	–	28	V
Line current					
TEA1067		I_{line}	–	140	mA
TEA1067T	note 1	I_{line}	–	100*	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.1	V
Total power dissipation					
TEA1067		P_{tot}	–	660	mW
TEA1067T		P_{tot}	–	450	mW
Operating ambient temperature range		T_{amb}	−25	+75	°C
Storage temperature range		T_{stg}	−40	+125	°C

Note to the ratings

1. * At a maximum operating ambient temperature of 65 °C (i.s.o. 75 °C), a maximum line current of 120 mA can be quaranteed. The total power dissipation is then 550 mW max.

CHARACTERISTICS

I_{line} = 11 to 140 mA (100 mA for TEA1067T); V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply; LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	1.75	2.0	2.25	V
	I_{line} = 7 mA	V_{LN}	2.25	2.8	3.35	V
	I_{line} = 11 mA	V_{LN}	3.55	3.8	4.05	V
	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
	I_{line} = 100 mA	V_{LN}	4.9	5.6	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−3	−1	1	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.1	3.4	3.7	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.2	4.5	4.8	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	1.0	1.35	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.4 mA	V_{CC}	2.2	2.4	–	V
	I_p = 0 mA	V_{CC}	3.0	3.2	–	V
Microphone inputs MIC+ and MIC−						
Input impedance (differential) between MIC− and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC− or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	$\Delta G_v/\Delta f$	–0.5	± 0.2	+0.5	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	$\Delta G_v/\Delta f$	–0.5	±0.2	+0.5	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C I_{line} = 50 mA	$\Delta G_v/\Delta T$	–	±0.2	–	dB
Gain adjustment GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	0	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	–	1.9	–	V
	THD = 10%	$V_{LN(rms)}$	1.9	2.2	–	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	–	0.8	–	V
	I_{line} = 7 mA; THD = 10%	$V_{LN(rms)}$	–	1.4	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR–						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR–	I_{line} = 15 mA R4 = 100 kΩ					
single-ended	R_L (from QR+ or QR–) = 300 Ω	G_v	30	31	32	dB
differential	R_L (from QR+ or QR–) = 600 Ω	G_v	36	37	38	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	$\Delta G_v/\Delta f$	–0.5	–0.2	0	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	$\Delta G_v/\Delta T$	–	±0.2	—	dB
Output voltage	sinewave drive I_{line} = 15 mA; I_p = 0 mA; THD = 2% R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.25	0.29	–	V
differential	RL = 450 Ω	$V_{o(rms)}$	0.45	0.55	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.65	0.80	–	V
Output voltage	THD = 10%; RL = 150 Ω R4 = 100 kΩ					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−11	–	+8	dB
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Voltage attenuation MIC+ or MIC− to LN	MUTE = HIGH	G_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC Controlling the gain from IR to QR+/QR− and the fain from MIC+/MIC− to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		G_v	−1.0	−1.5	−2.0	dB

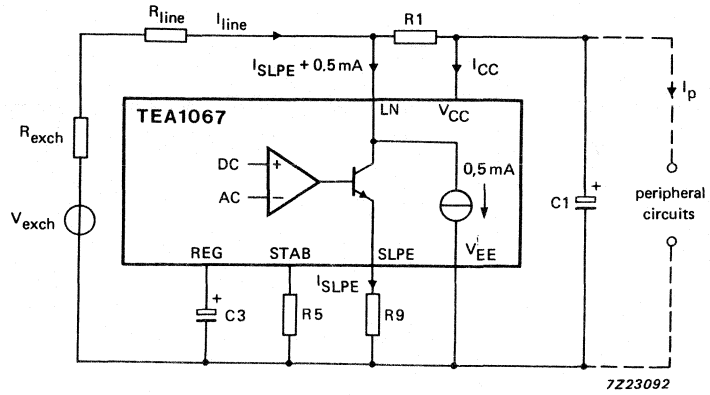
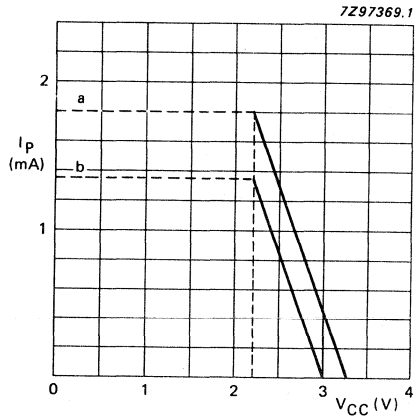


Fig. 6 Supply arrangement.



(a) I_p = 1.8 mA
(b) I_p = 1.35 mA
I_{line} = 15 mA at V_{LN} = 3.9 V
R1 = 620 Ω and R9 = 20 Ω.

Fig. 7 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical.
The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

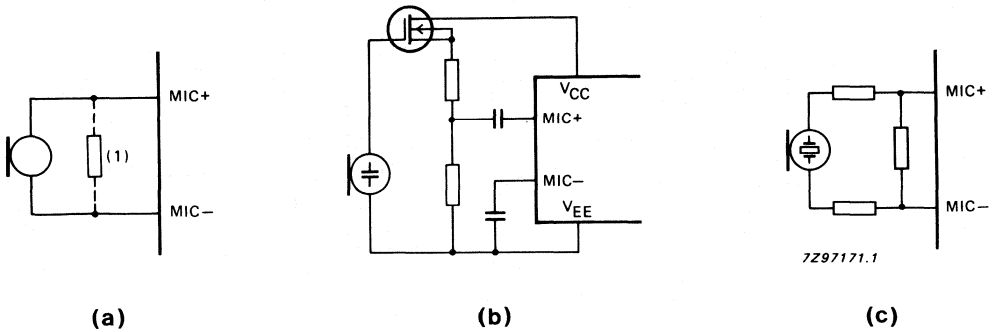


Fig. 8 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

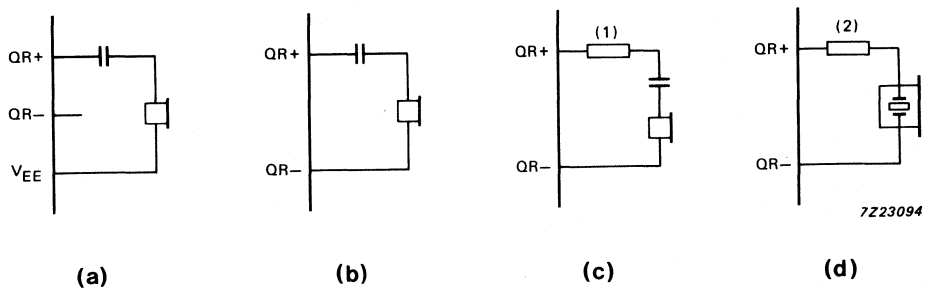
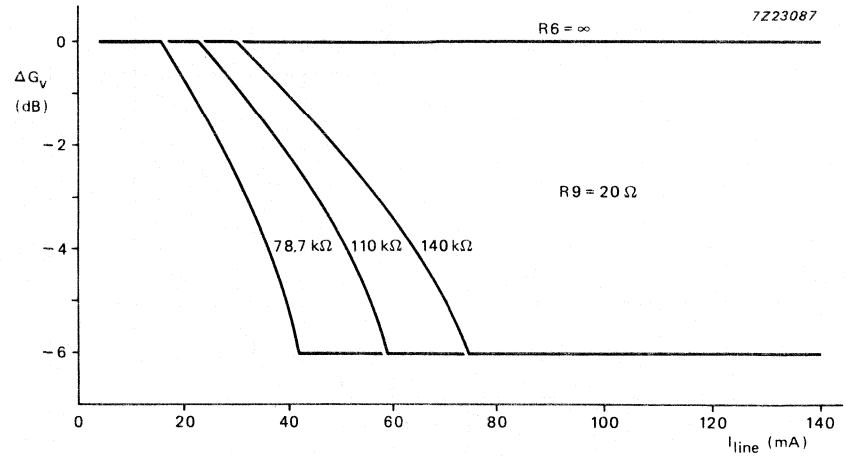


Fig. 9 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).



Note: $I_{line} > 100$ mA for TEA1067 only.

Fig. 10 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

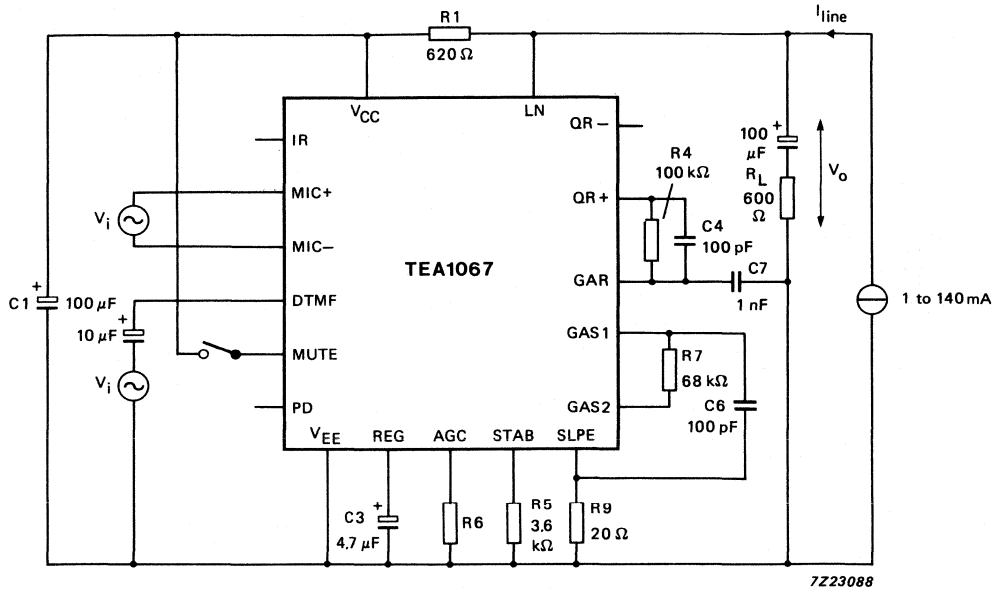


Fig. 11 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

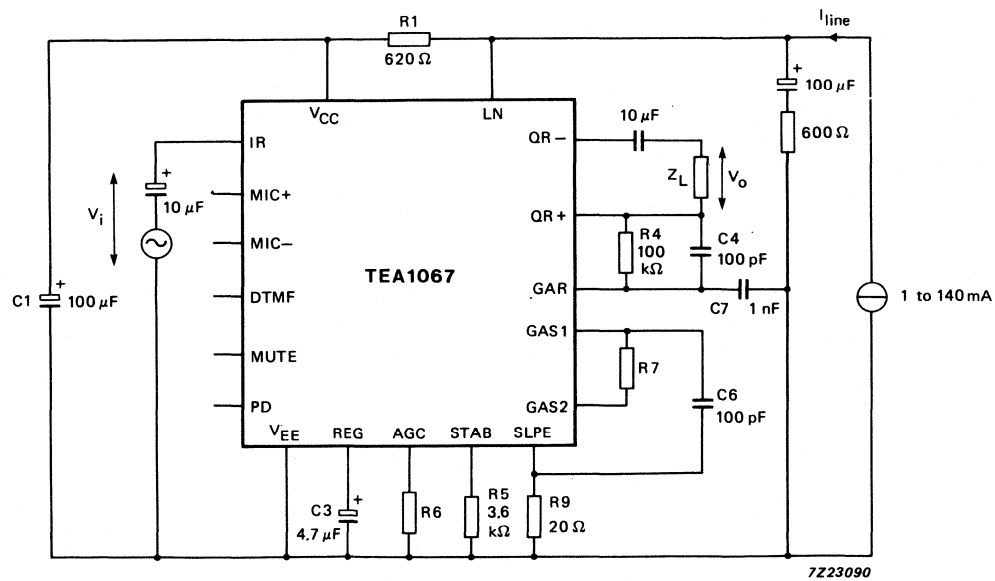


Fig. 12 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

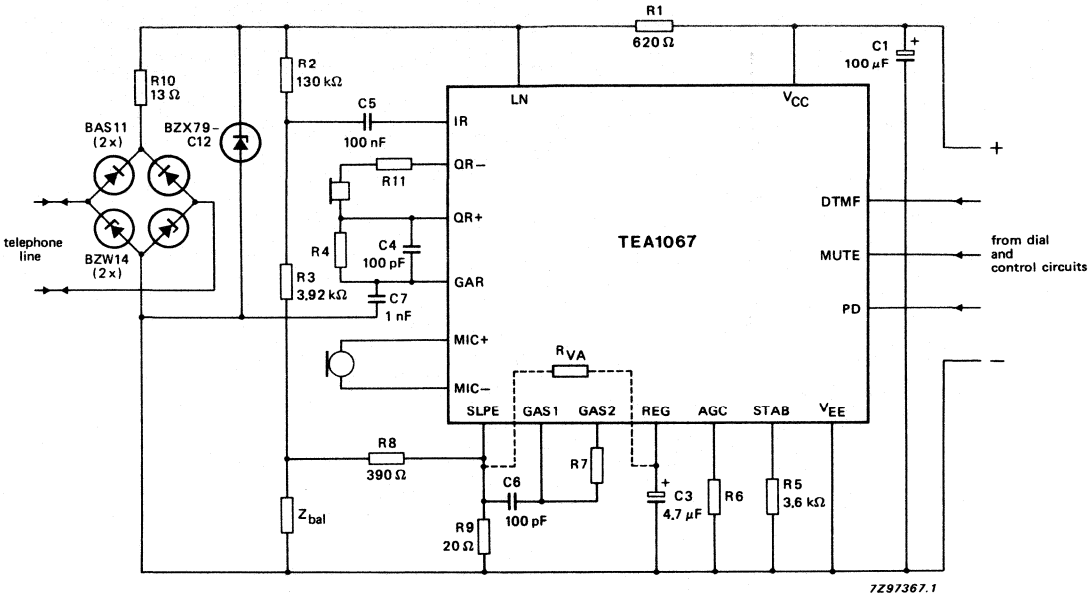
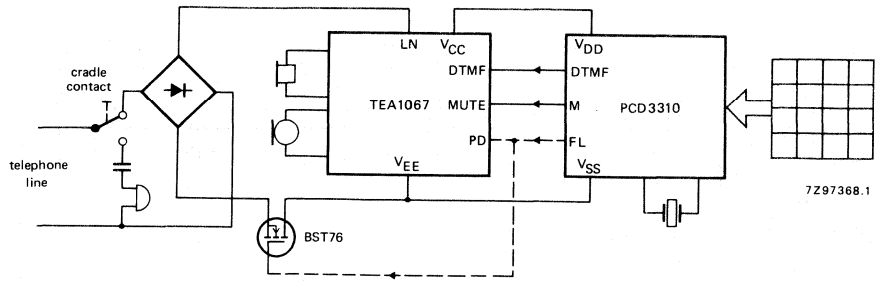
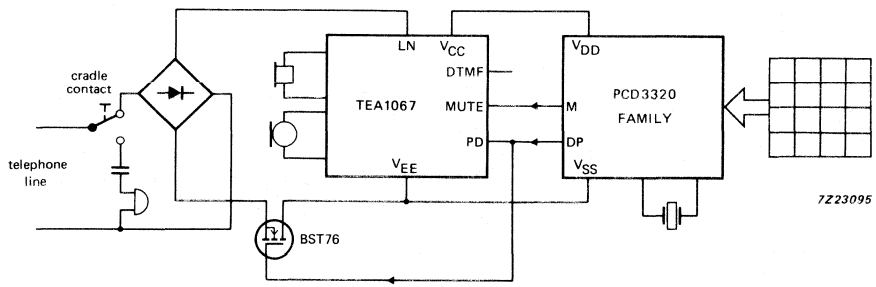


Fig. 13 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).

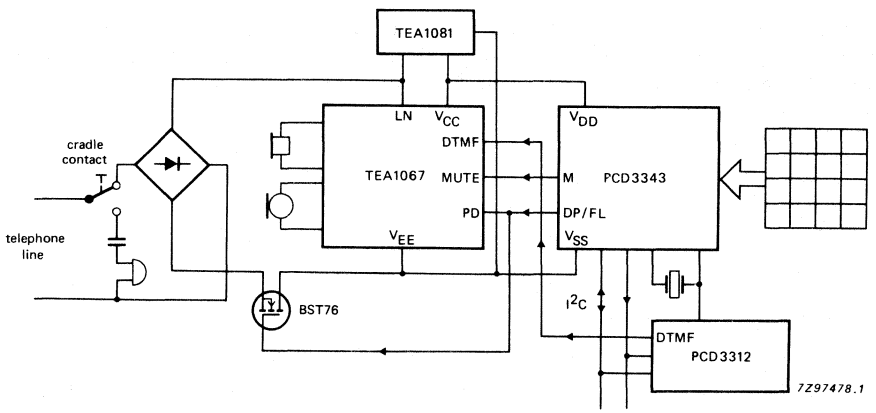
APPLICATION INFORMATION (continued)



(a)



(b)



(c)

Fig. 14 Typical applications of the TEA1067 (simplified).

(a) DTMF-Pulse set with CMOS-bilingual dialling circuit PCD3310.
The dashed lines show an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

Features

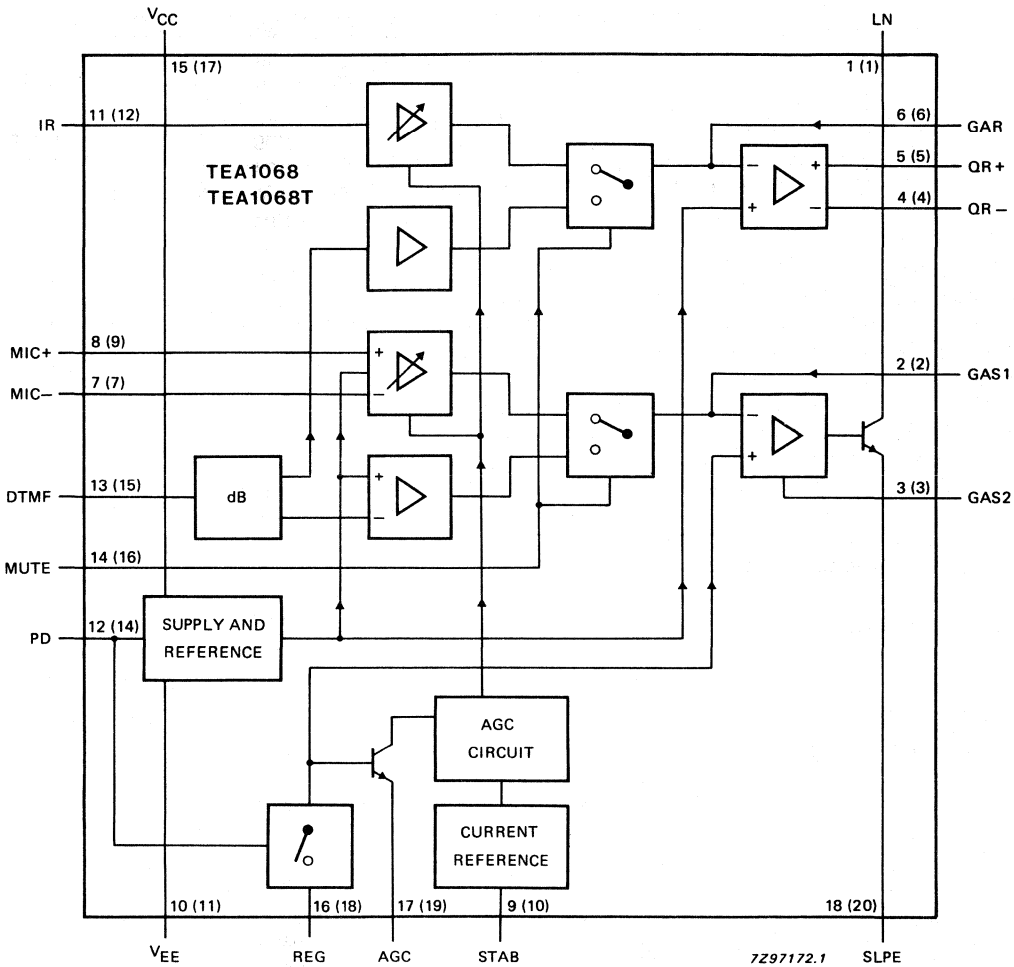
- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	–	4.45	–	V
Line current operating range	normal operation					
	TEA1068	I_{line}	10	–	140	mA
	TEA1068T	I_{line}	10	–	100	mA
Internal supply current	power down					
	input LOW	I_{CC}	–	1	–	mA
	input HIGH	I_{CC}	–	55	–	μA
Supply voltage for peripherals	I_{line} = 15 mA; mute input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	–	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	60	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation gain control range		ΔG_v	–	5.9	–	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1068: 18-lead DIL; plastic (SOT102).
TEA1068T: 20-lead mini-pack; plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1068T.

Fig. 1 Block diagram.

PINNING

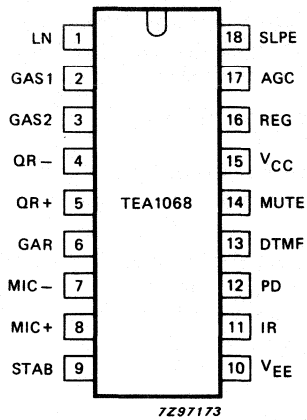


Fig. 2 (a) Pinning diagram for TEA1068 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

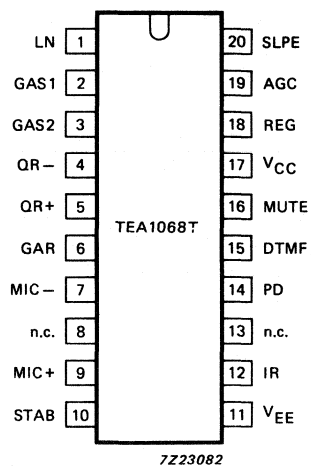


Fig. 2 (b) Pinning diagram for TEA1068T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply; V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1068 and its peripheral circuits is usually obtained from the telephone line. The supply voltage (V_{CC}) is derived from the line via a dropping resistor and regulated by the TEA1068. V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupiing of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

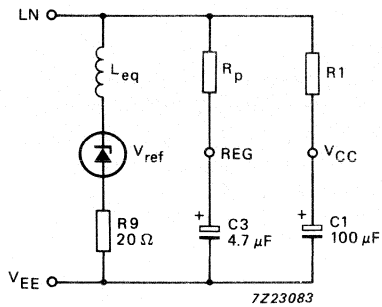
The TEA 1068 has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 6). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}) - I_p] \times R9$$

where: V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics side-tone and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5$ mA + I_p, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.
The current (I_p) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig. 7 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode). If MUTE is LOW when the receiving amplifier is driven available current is further reduced.



R_p = 17.5 kΩ; the loading is provided by R_p, R9 and C3

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 11). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 8.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligable clicking on the telephone outputs and the line.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 9). IR to QR + gain is typically 25 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single end drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

FUNCTIONAL DESCRIPTION (continued)

Receiving amplifier (IR, QR+, QR– and GAR) (continued)

The receiving amplifier gain can be adjusted between 17 and 33 dB with single-ended drive and between 26 and 39 dB with differential drive to match the sensitivity of the transducer in use. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subracting the anti-sidetone network attenuation, (32 dB), from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

Automatic gain control input (AGC)

Automatic line loss compensation is acieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 10 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, ($R1//Z_{line}$, R2, R3 and Z_{bal}), (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in;

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor, $k = (R8/R1)$.

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line impedance at which the optimum suppression is present can be calculated by;
210 Ω + (1265 Ω/140 nF). This represents a 5 km line of 0.5 mm diameter, copper, twisted pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

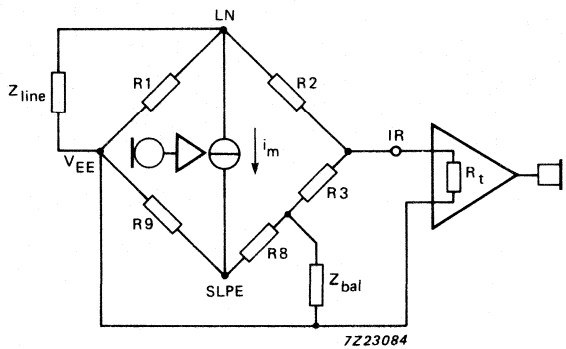


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

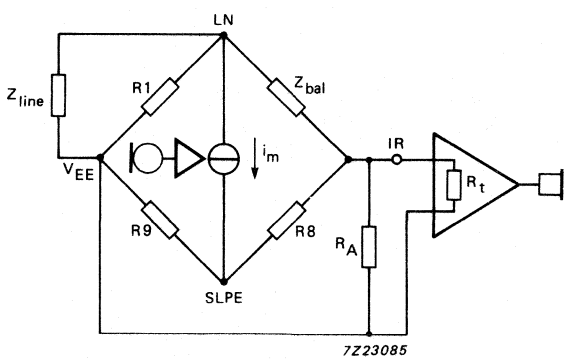


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage	continuous	V_{LN}	–	12	V
Repetitive line voltage	during switch-on or line interruption	V_{LN}	–	13.2	V
Repetitive peak line voltage	t_p/p = 1 ms/5 s R10 = 13 Ω; R9 = 20 Ω; see Fig. 13	V_{LN}	–	28	V
Line current					
TEA1068		I_{line}	–	140	mA
TEA1068T		I_{line}	–	100	mA
Voltage on all other pins		V_i	–	$V_{CC}+0.7$	V
		$-V_i$	–	0.7	V
Total power dissipation					
TEA1068		P_{tot}	–	660	mW
TEA1068T		P_{tot}	–	470	mW
Operating ambient temperature range		T_{amb}	−25	+75	°C
Storage temperature range		T_{stg}	−40	+125	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA (100 mA for TEA1068T); V_{EE} = 0 V; f = 800 Hz, T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–4	–2	0	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.45	3.8	4.1	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.65	5.0	5.35	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 0 mA	V_{CC}	3.5	3.75	–	V
Microphone inputs MIC+ and MIC–						
Input impedance (differential) between MIC– and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC– or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	$\Delta G_v/\Delta f$	–0.5	± 0.2	+0.5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C; without R6; I_{line} = 50 mA	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF ro LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	$\Delta G_v/\Delta f$	–0.5	± 0.2	+ 0.5	dB
Gain variation with temperature at – 25 °C and + 75 °C	w.r.t 25 °C I_{line} = 50 mA	$\Delta G_v/\Delta T$	–	± 0.5	–	dB
Gain adjustement GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	+ 8	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	1.9	2.3	–	V
	THD = 10%	$V_{LN(rms)}$	–	2.6	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	24	25	26	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	$\Delta G_v/\Delta f$	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +85 °C	w.r.t. 25 °C; I_{line} = 50 mA; without R6	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Output voltage	sinewave drive; I_{line} = 50 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
differential	RL = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	V
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	V
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−8	–	+8	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Voltage attenuation MIC+ or MIC– to LN	MUTE = HIGH	G_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	–21	–19	–17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC						
Controlling the gain from IR to QR+/QR– and the gain from MIC+/MIC– to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	–5.5	–5.9	–6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		G_v	–1.0	–1.5	–2.0	dB

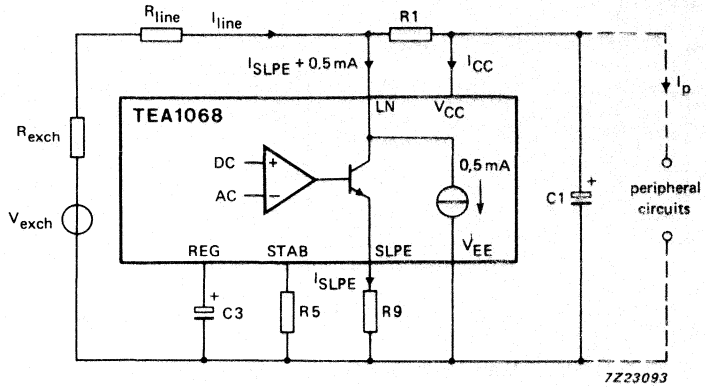


Fig. 6 Supply arrangement.

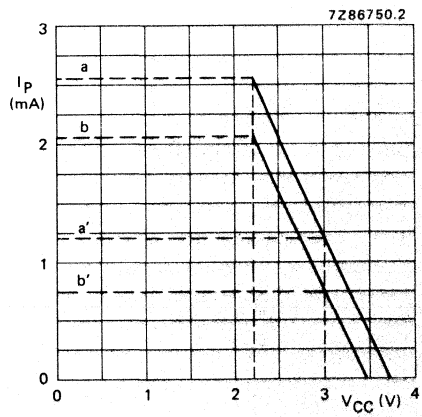


Fig. 7 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ asymmetrical. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

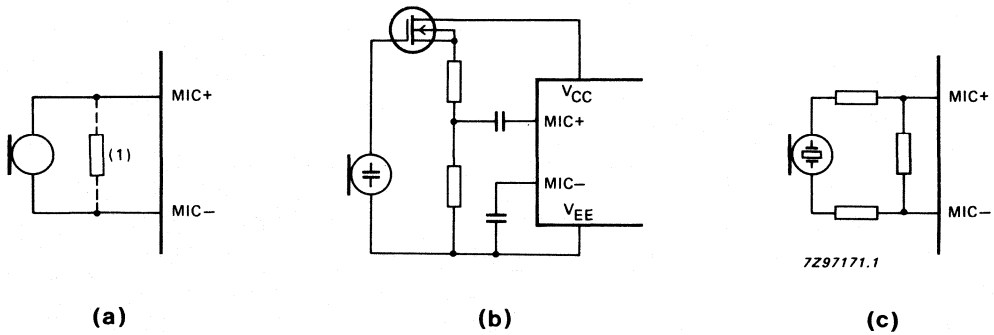


Fig. 8 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

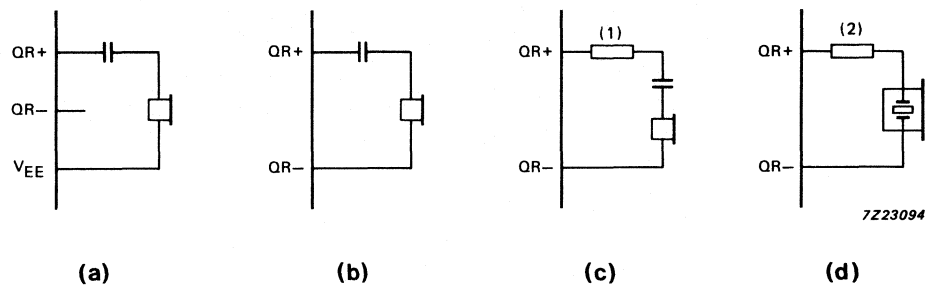
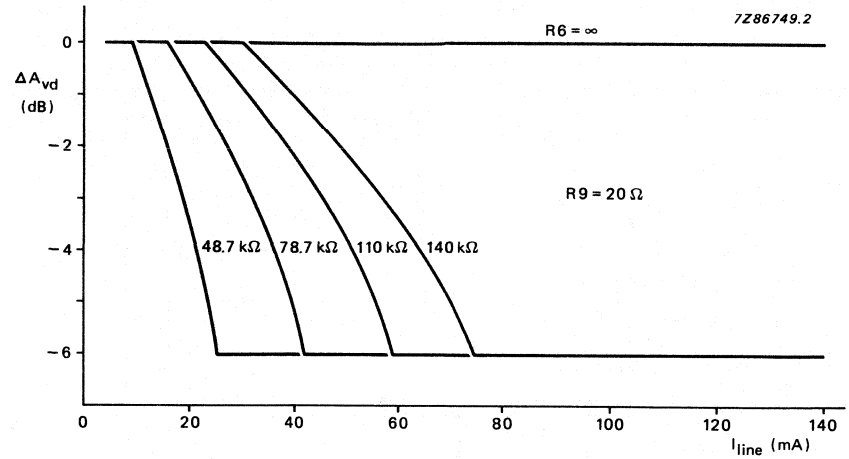


Fig. 9 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).



Note: $I_{line} > 100$ mA for TEA1068 only.

Fig. 10 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (KΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

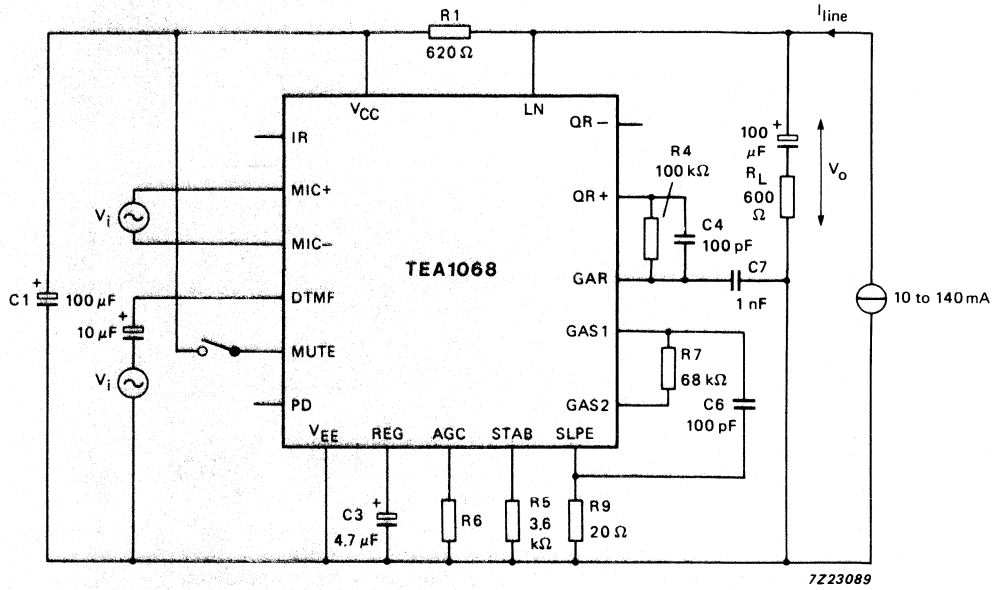


Fig. 11 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

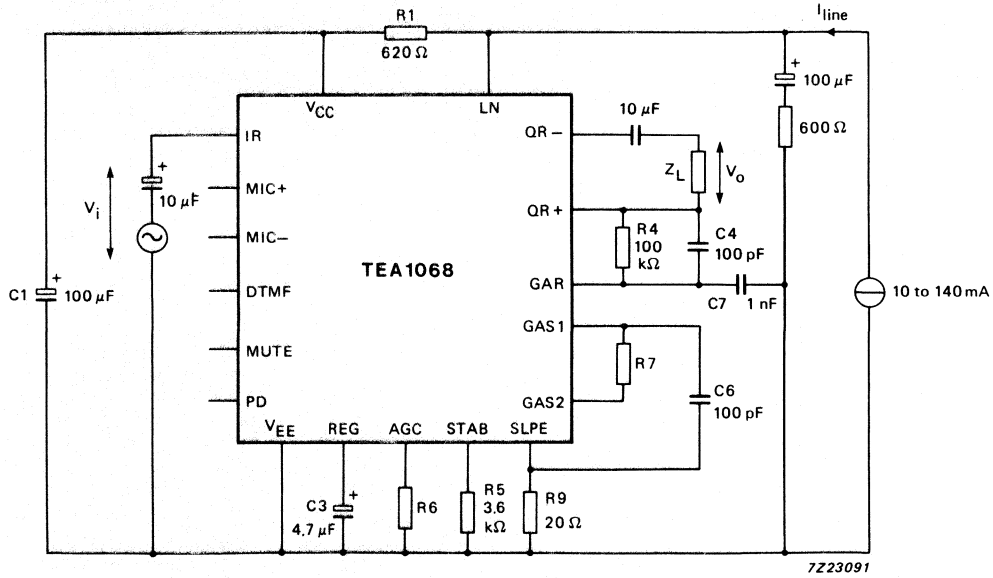


Fig. 12 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

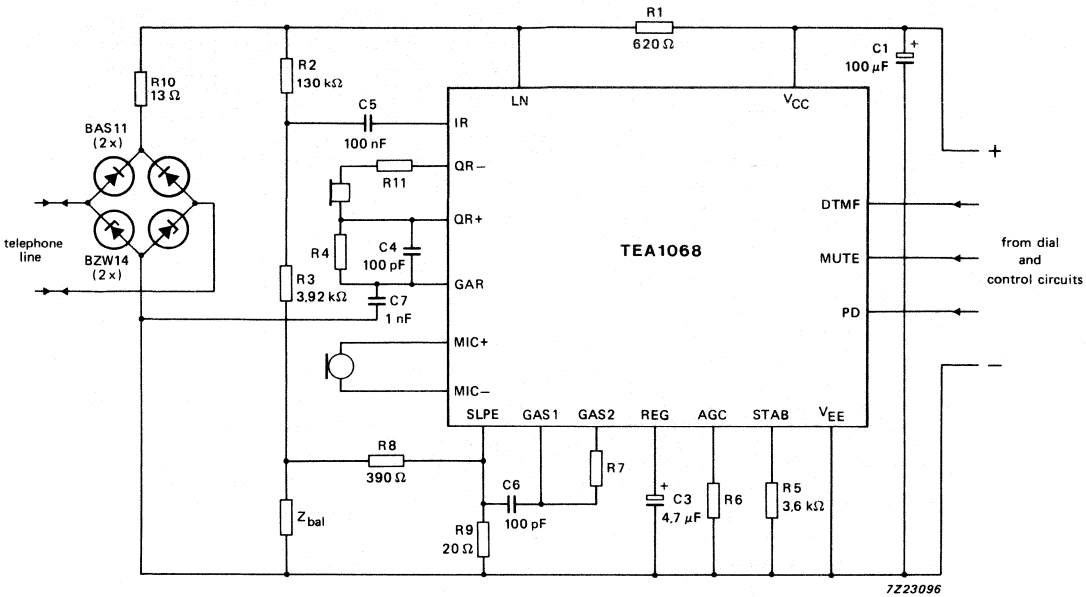


Fig. 13 Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

APPLICATION INFORMATION (continued)

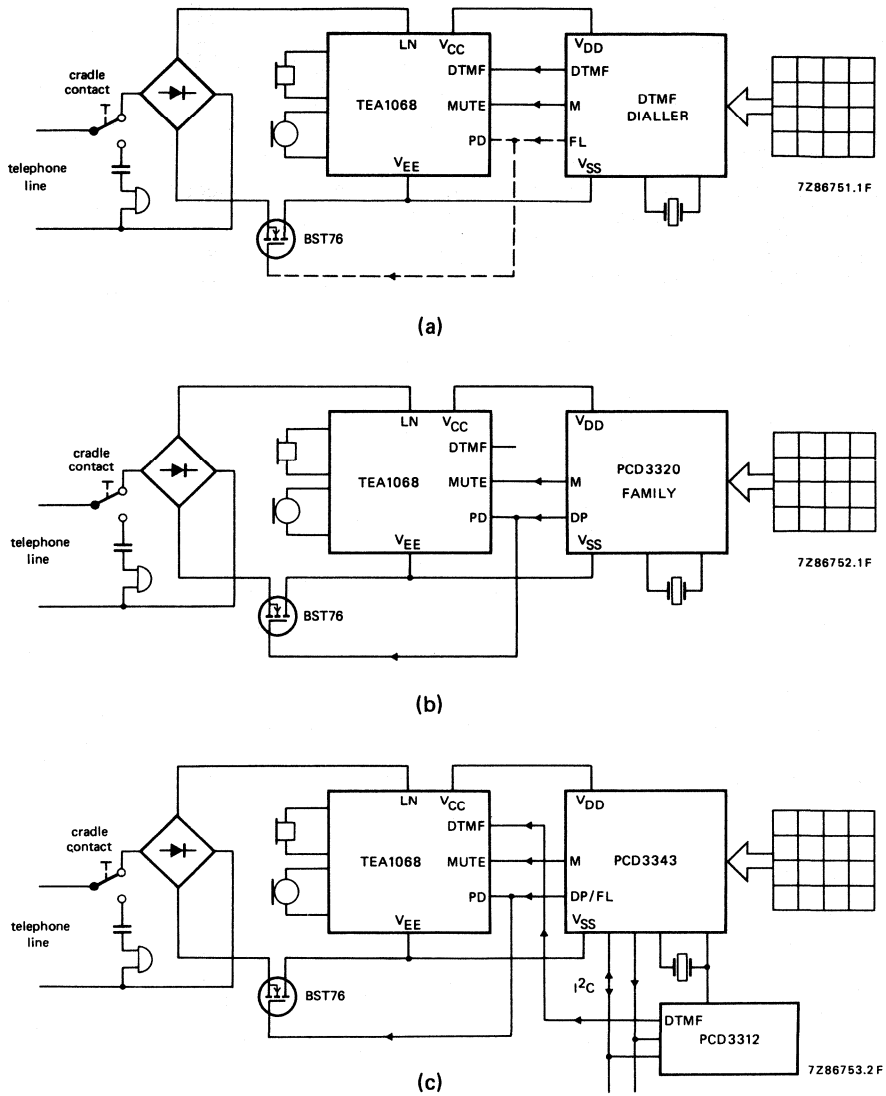


Fig. 14 Typical applications of the TEA1068 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by times loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus.

SUPPLY CIRCUIT WITH POWER-DOWN FOR TELEPHONE SET PERIPHERALS

GENERAL DESCRIPTION

The TEA1081 is a bipolar integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaking facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

Features

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
  - output voltage that follows the DC line voltage
  - regulated output voltage
- Power-down input
- Low number of external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating DC line voltage		V_{LN}	2,5	–	12	V
DC output voltage		V_O	2,0	–	10	V
Voltage drop from line to output		V_{LN}-V_O	–	0,5	–	V
Series resistance		R_S	–	20	–	Ω
Output current	V_{LN} = 4 V					
TEA1081		I_O	–	–	30	mA
TEA1081T		I_O	–	–	20	mA
AC line voltage (RMS value)	V_{LN} = 4 V; I_O = 15 mA; d = 2%	$v_{LN(rms)}$	–	1,5	–	V
Internal supply current	V_{LN} = 4 V	I_{INT}	–	0,8	–	mA
Operating ambient temperature range		T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINES

TEA1081: 8-lead dual in-line; plastic (SOT97).
TEA1081T: 8-lead mini-pack; plastic (SO8; SOT96A).

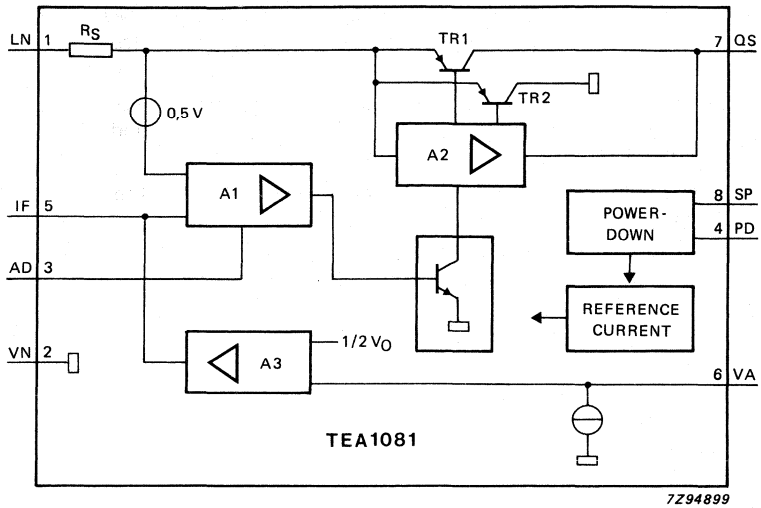


Fig. 1 Block diagram.

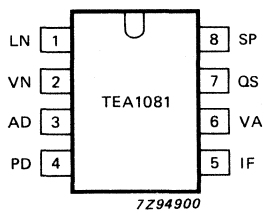


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	VN	negative line terminal
3	AD	amplifier decoupling
4	PD	power-down input
5	IF	low pass filter input
6	VA	output voltage adjustment
7	QS	power supply output
8	SP	supply input: power-down circuit

FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (Fig. 1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN, VN (pins 1, 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is given by

$$V_{LN} = I_1 \times R_S + V_{LN\,min} + v_{LN(P)} \quad (V)$$

in which

I_1 = input current
R_S = internal series resistance
$v_{LN\,min}$ = minimum instantaneous line voltage (1,4 V at I_O = 5 mA)
$v_{LN(P)}$ = required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0,8 mA at V_{LN} = 4 V and reaches a maximum of 1,4 mA at V_{LN} = 12 V.

Supply terminals: QS, VA (pins 7, 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available:

Output voltage follows line voltage (Fig. 3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (pins 6 and 7).

The output voltage follows the line voltage and is expressed by

$$V_O = V_{LN} - (I_1 \times R_S + 0{,}5) \quad (V)$$

in which

V_{LN} = line voltage
I_1 = input current
R_S = internal series resistance

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

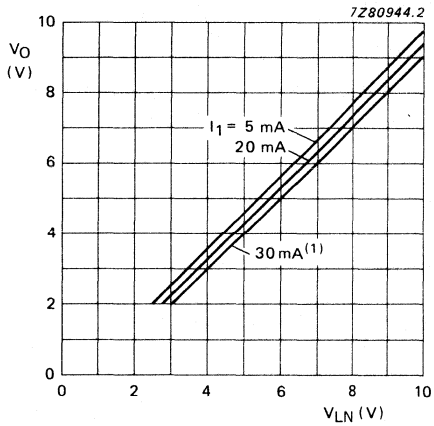
Regulated output voltage (Fig. 4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (pins 6 and 7, see Fig. 6).

The output voltage is held constant at $V_O = 2 \times I_6 \times R_V$ (V)

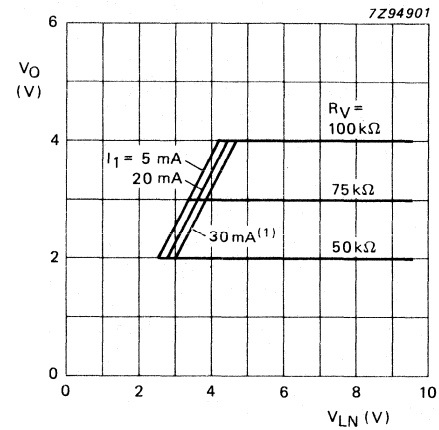
as soon as the line voltage $V_{LN} > (2 \cdot I_6 \cdot R_v + I_1 \cdot R_S + 0{,}5)$ (V)

The control current I_6 is typically 20 μA.



(1) I_1 = 30 mA; not valid for TEA1081T

Fig. 3 Output voltage as a function of line voltage (application without R_V).



(1) I_1 = 30 mA; not valid for TEA1081T

Fig. 4 Output voltage as a function of line voltage (R_V connected between QS and VA).

Input and output currents I_1, I_O (pins 1 and 7)

The maximum available current into pin 1 (I_1) is determined by:

- the minimum line current ($I_{LINE\ min}$) that is available for the telephone set;
- the specified minimum input current ($I_{LN\ min}$) for the speech/transmission circuit.

That is $I_{1\ max} = I_{LINE\ min} - I_{LN\ min}$.

At $v_{LN(rms)} < 150$ mV, the input current I_1 is approximately:

$$I_1 = I_{INT} + k \cdot I_O \quad \text{(mA)}$$

in which

I_{INT} = internal supply current (0,8 mA at V_{LN} = 4 V);
k = correction factor (k < 1,1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below $V_O + 0,4$ V. Normally (when $v_{LN} > V_O + 0,4$ V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load. When $v_{LN} < V_O + 0,4$ V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at $v_{LN(rms)} = 1$ V and without R_V approximates to

$$I_1 = I_{INT} + 2\,I_O \quad \text{(mA)}$$

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by

$$I_{O\,max} = \frac{I_{LINE\,min} - I_{LN\,min} - I_{INT}}{2}$$

in which

$I_{LINE\,min}$ is the minimum line current of the telephone set;

$I_{LN\,min}$ is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined mainly by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω). At audio frequencies the TEA1081 behaves as an inductor of the value $L_I = C_L \cdot R_L \cdot R_S$ (H). The typical value of L_I at $C_L = 2,2\ \mu$F and $R_L = 100$ kΩ is 4,4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1). If $I_{Omin} < 1,5$ mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD, SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to (typ.) 40 μA at $V_{LN} = 4$ V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where $V_O > V_{SP\,min}$ during line interruptions. When $V_O < V_{SP\,min}$, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage	continuous	V_{LN}	–	12	V
	during switch-on or line interruptions	V_{LN}	–	12,5	V
Repetitive line voltage peaks	1 ms/5 s; 12 Ω resistor in series with pin 1	V_{LN}	–	28	V
Voltage on all other terminals		V	V_{VN}–0,5	V_{LN}+0,5	V
Input current (DC)	TEA1081	I_1	–	120	mA
Input current (DC)	TEA1081T	I_1	–	80	mA
Current into all other terminals		I_I	–1	+1	mA
Total power dissipation		P_{tot}	see Fig. 5		
Storage temperature range		T_{stg}	–40	+125	°C
Operating ambient temperature range		T_{amb}	–25	+70	°C
Junction temperature		T_j	–	+125	°C

THERMAL RESISTANCE

From junction to ambient in free air

TEA1081 $R_{th\ j\text{-}a}$ = 120 K/W

TEA1081T (circuit mounted on printed circuit board of 50 x 50 x 1,5 mm) $R_{th\ j\text{-}a}$ = 260 K/W

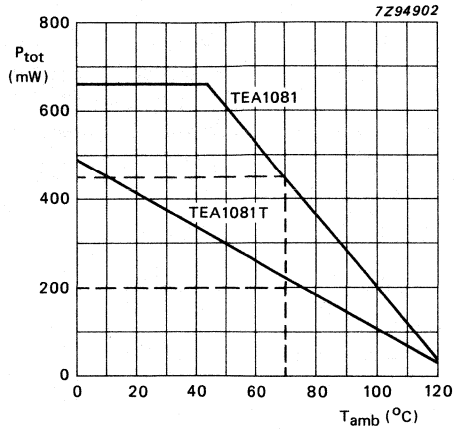


Fig. 5 Power derating curves.

DEVELOPMENT DATA

CHARACTERISTICS

V_{LN} = 4 V; $v_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 300 to 3400 Hz; R_L = 100 kΩ; C_L = 2,2 μF; R_V = 75 kΩ; T_{amb} = 25 °C; unless otherwise specified; see Fig. 6.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating DC line voltage		V_{LN}	2,5	–	12	V
Min. instantaneous line voltage		V_{LN}	–	–	1,4	V
Max. instantaneous line voltage		V_{LN}	12	–	–	V
Characteristics with R_V = 75 kΩ connected between pins 6 and 7 and C_L = 10 μF						
Input current (pin 1)						
	v_{LN} = 0 V	I_1	–	5,8	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	30	–	mA
Output voltage (pin 7)		V_O	–	3	–	V
Variation of output voltage over the ranges of:						
line voltage	V_{LN} = 4 to 6 V	ΔV_O	–	100	–	mV
temperature	T_{amb} = +25 to −25 °C	ΔV_O	–	−100	–	mV
	T_{amb} = +25 to +75 °C	ΔV_O	–	−100	–	mV
output current	I_O = 5 to 20 mA	ΔV_O	–	−100	–	mV
Control current (pin 6)		I_6	–	20	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Characteristics without R_V						
Input current (pin 1)	v_{LN} = 0 V	I_1	–	6,0	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	31	–	mA
Voltage drop (pin 1 to pin 7)	I_O = 0 mA	V_{LN}-V_O	–	0,5	–	V
	I_O = 15 mA; $v_{LN(rms)}$ = 1,5 V	V_{LN}-V_O	–	1,1	–	V
Output current (pin 7)						
	TEA1081	I_O	–	–	30	mA
	TEA1081T	I_O	–	–	20	mA
Internal series resistance		R_S	–	20	–	Ω
Internal supply current	I_O = 0 mA; PD = LOW; V_{SP} = V_O	I_{INT}	–	0,8	1,4	mA
	PD = HIGH (note 1); V_{SP} > 2 V	I_{INT}	–	40	60	μA
Total distortion	$v_{LN(rms)}$= 1,5 V	d_{tot}	–	–	2	%
Balance return loss	600 Ω reference	BRL	25	–	–	dB
Harmonic levels of line voltage	f = 500 Hz; v_{LN} = 0 dBm; Z_{line} = 600 Ω					
	second harmonic	v_{LN}–2H	–	–58	–	dBm
	third harmonic	v_{LN}–3H	–	–60	–	dBm
Noise voltage on input terminal	v_{LN} = 0 mV; R_L = 600 Ω; P53 curve	$v_{ni(rms)}$	–	–83	–	dBmp
Power-down input (pin 4)						
Input voltage HIGH		V_{IH}	1,5	–	V_{SP}	V
Input voltage LOW		V_{IL}	–	–	0,3	V
Input current		I_4	–	–	10	μA
Power-down input (pin 8)						
Supply voltage for power-down		V_8	2	–	V_{LN}	V
Supply current to power-down circuit	V_8 = 3 V	I_8	–	–	70	μA

Note 1. Power-down circuit supplied via external source.

APPLICATION INFORMATION

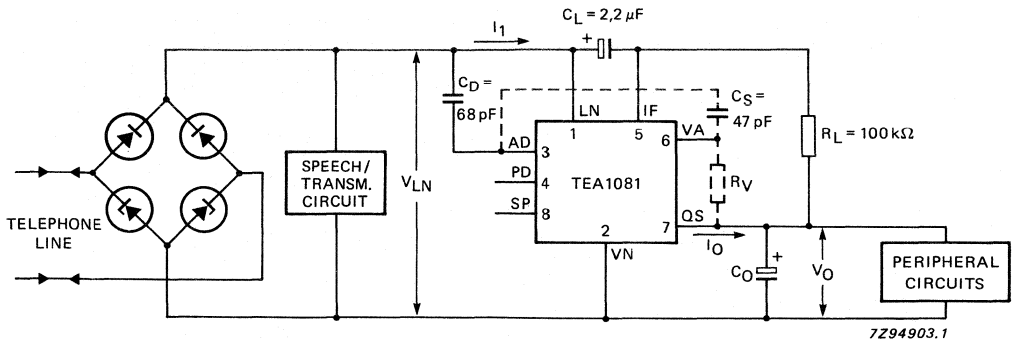


Fig. 6 Application diagram.

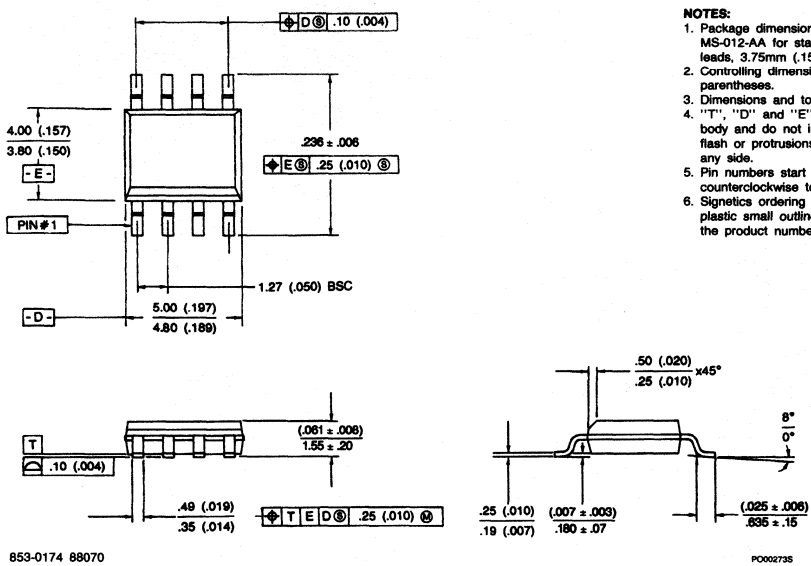
DEVELOPMENT DATA

PACKAGE INFORMATION

Package outlines

Soldering

8-PIN PLASTIC SO (D PACKAGE)

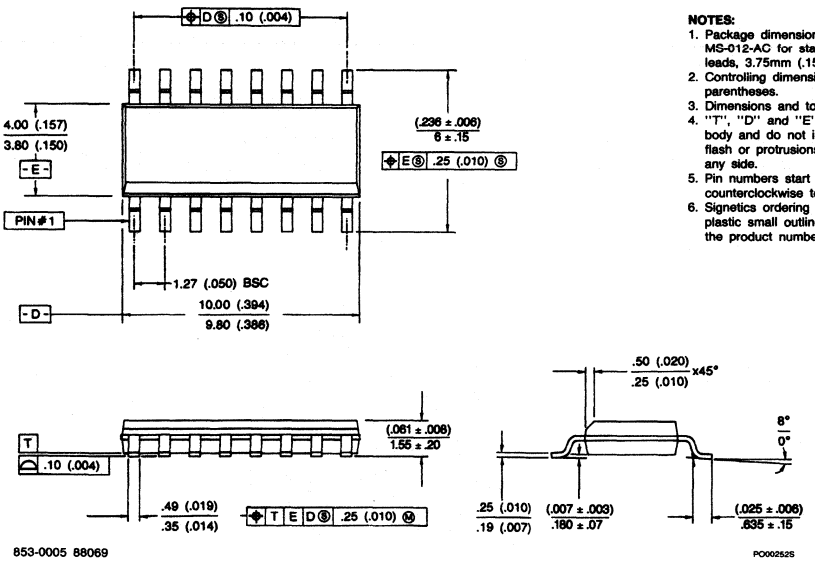


853-0174 88070

PO00273S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE)

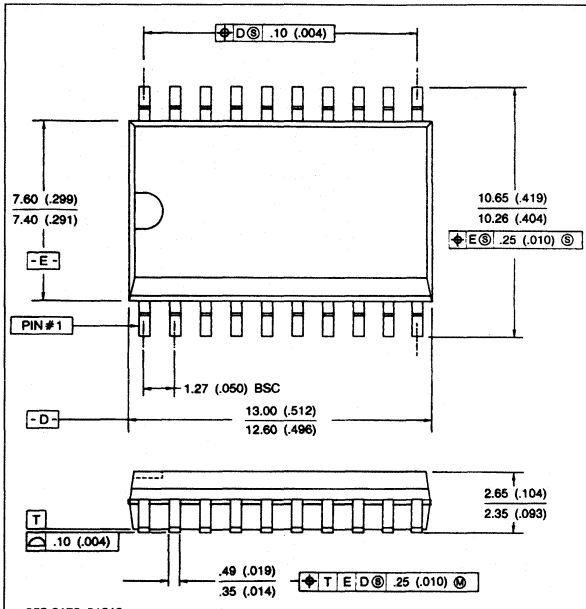


853-0005 88069

PO00252S

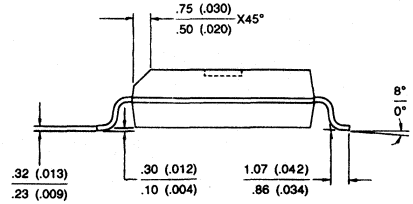
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

20-PIN PLASTIC SOL (D PACKAGE)



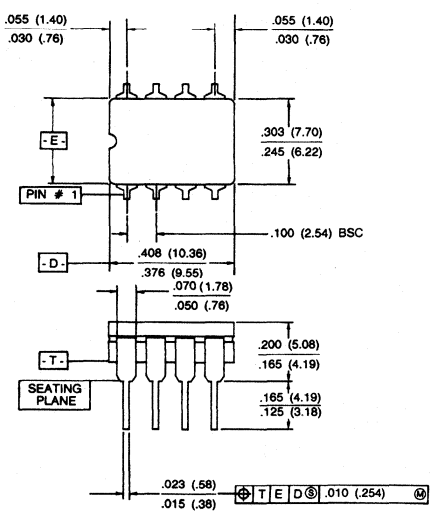
853-0172 81219

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



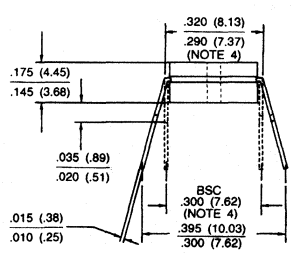
PO00231S

8-PIN CERDIP (FE PACKAGE)



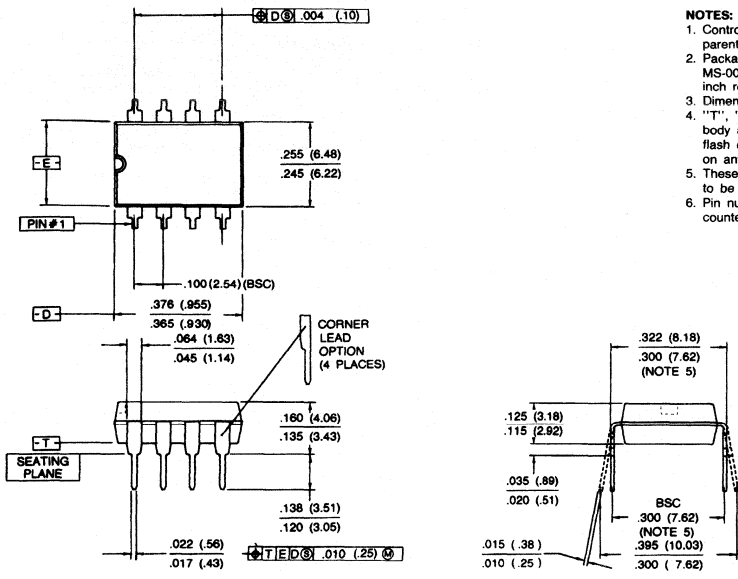
853-0580 81594

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.



PO00480S

8-PIN PLASTIC PDIP (N PACKAGE)

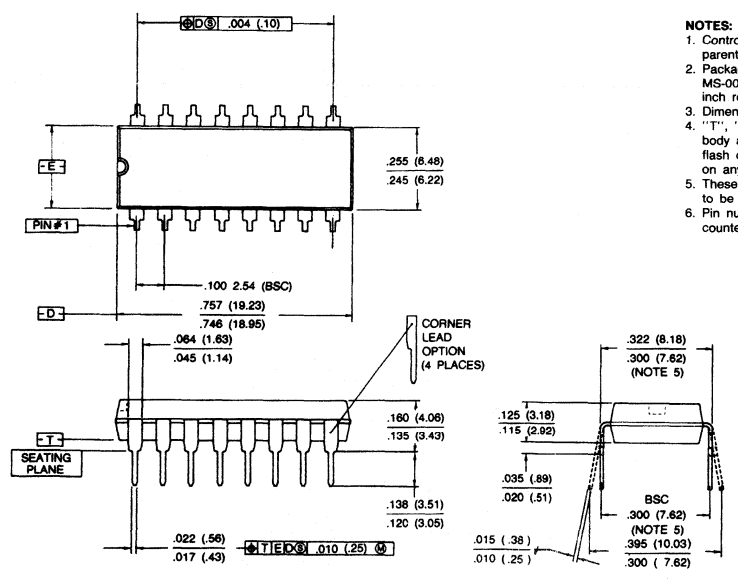


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

16-PIN PLASTIC DIP (N PACKAGE)

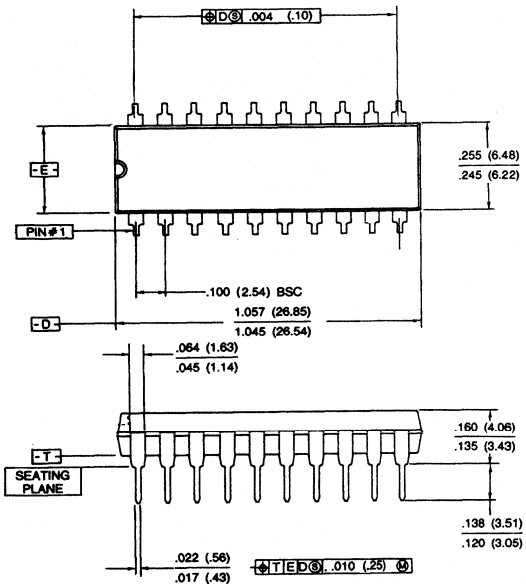


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO00280S

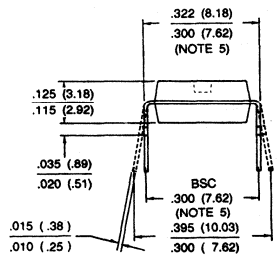
20-PIN PLASTIC DIP (N PACKAGE)



853-0408 81234

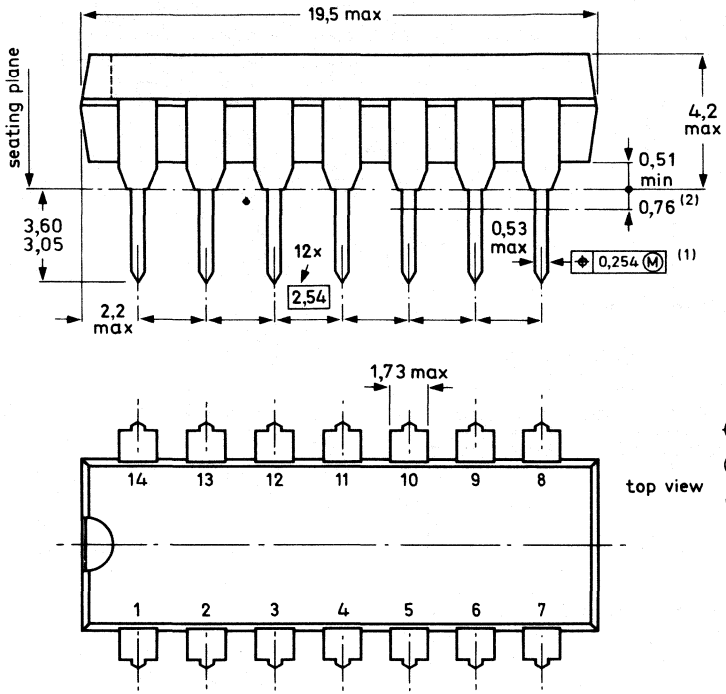
NOTES:

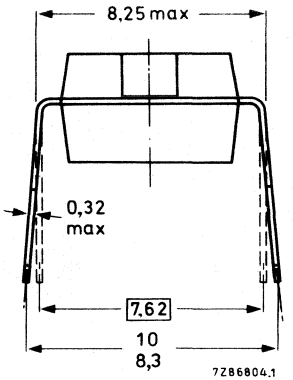
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.



PO00290S

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)





Dimensions in mm

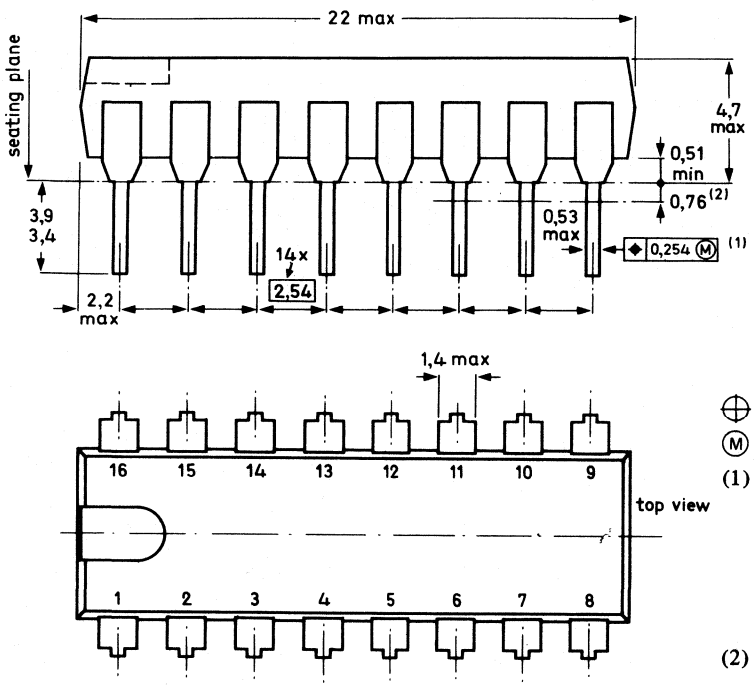
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



Dimensions in mm

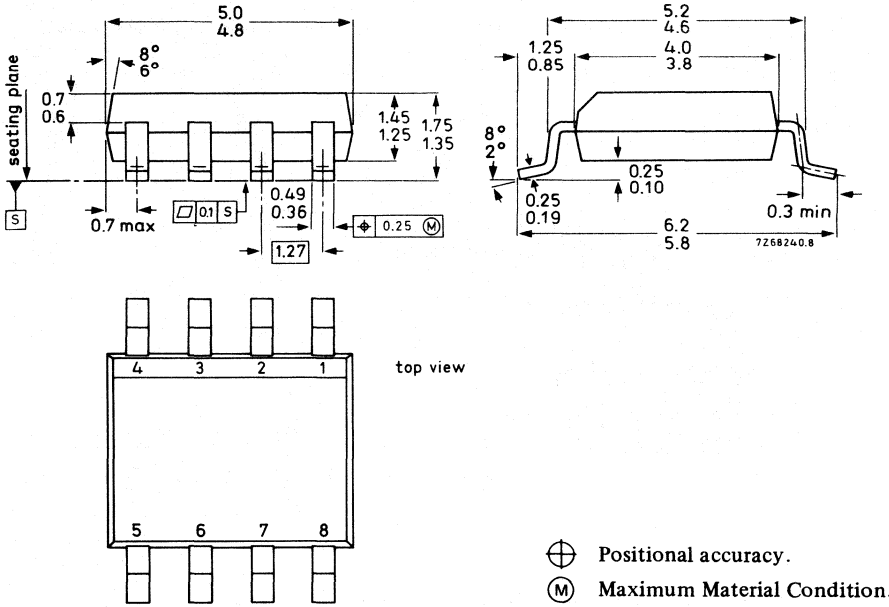
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

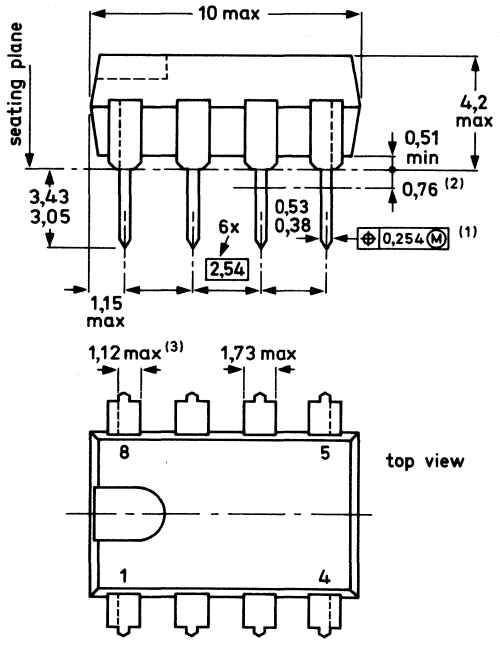


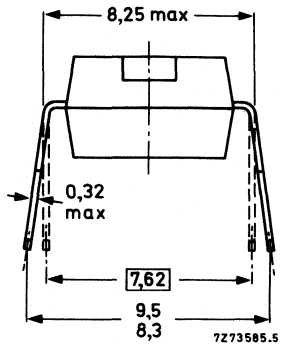
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

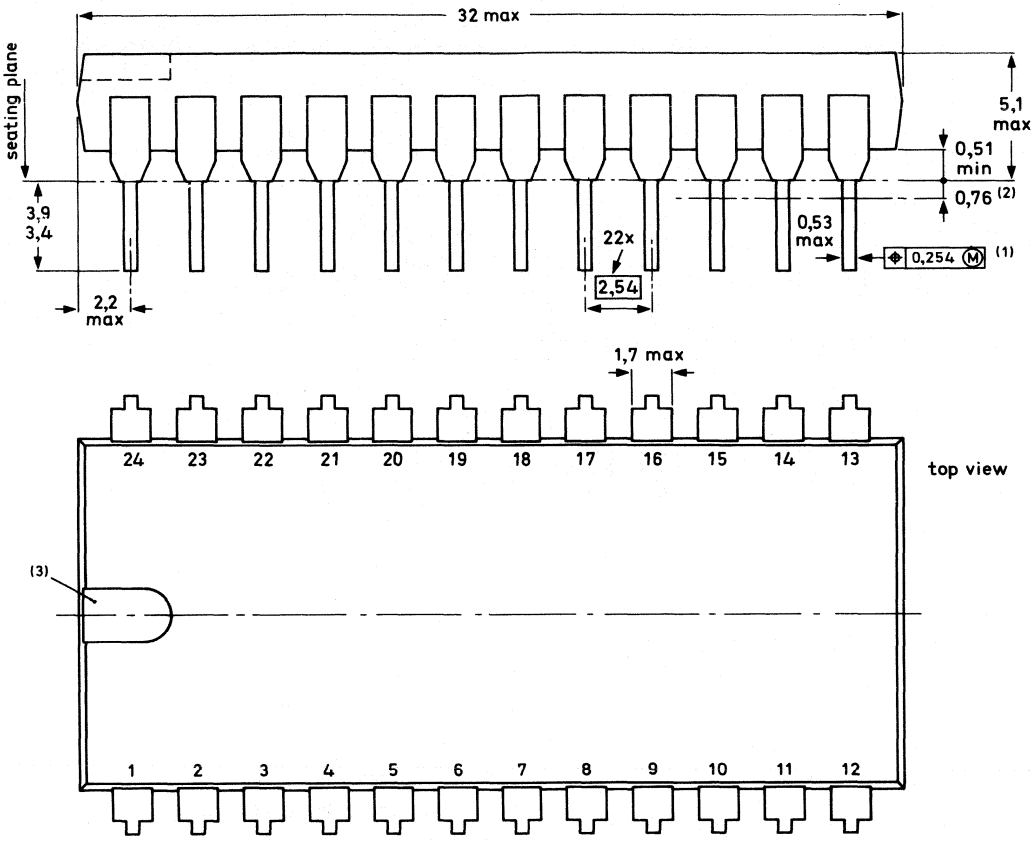
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

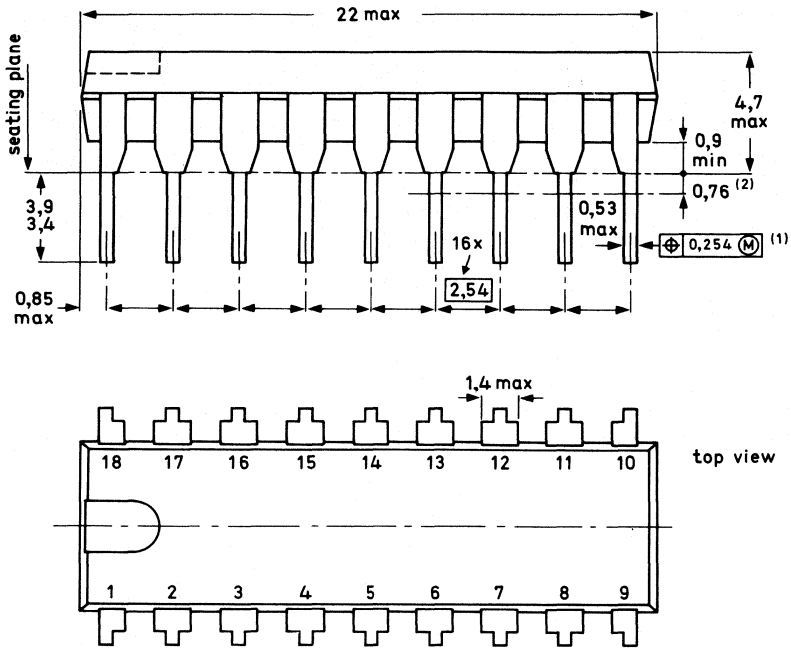
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

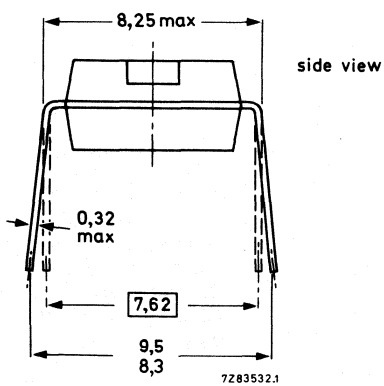
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)





⊕ Positional accuracy.

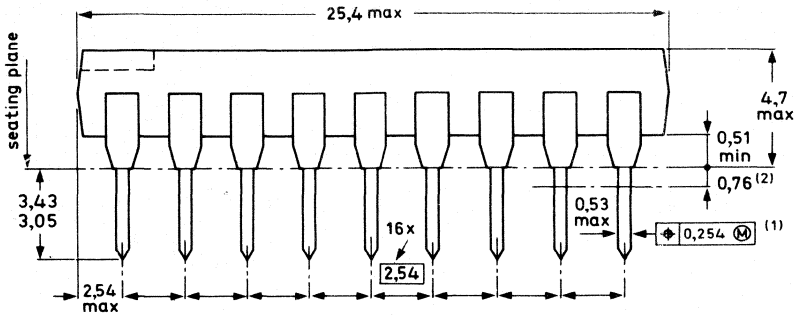
Ⓜ Maximum Material Condition.

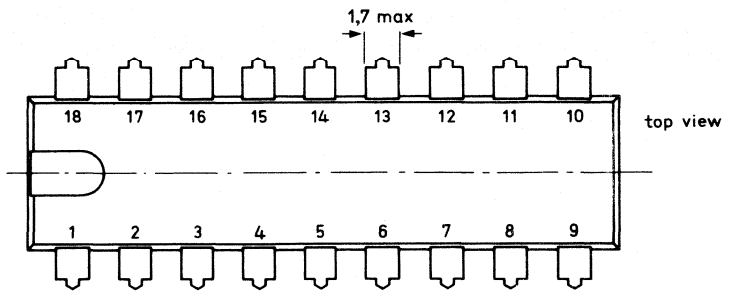
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

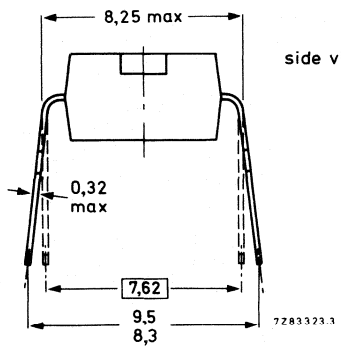
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102G, N, PE)







⊕ Positional accuracy.

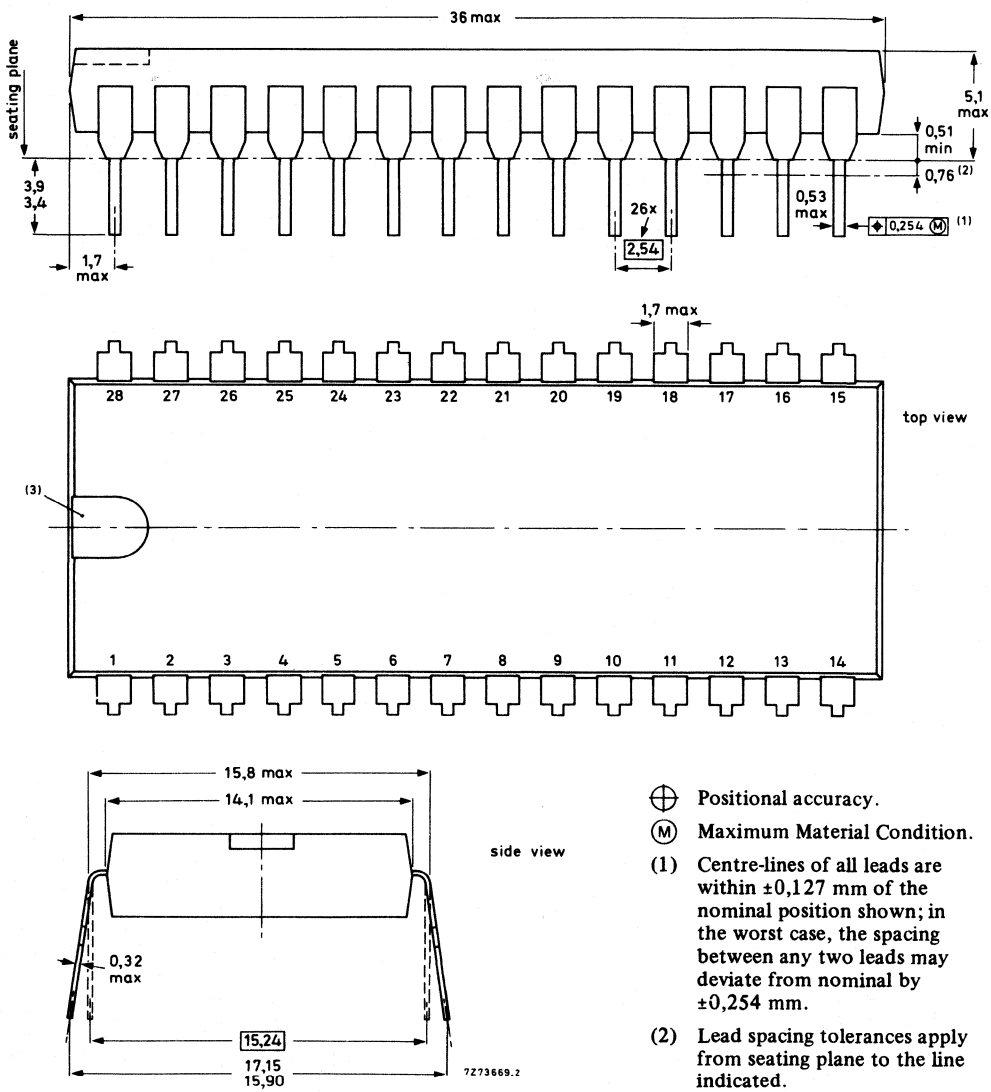
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

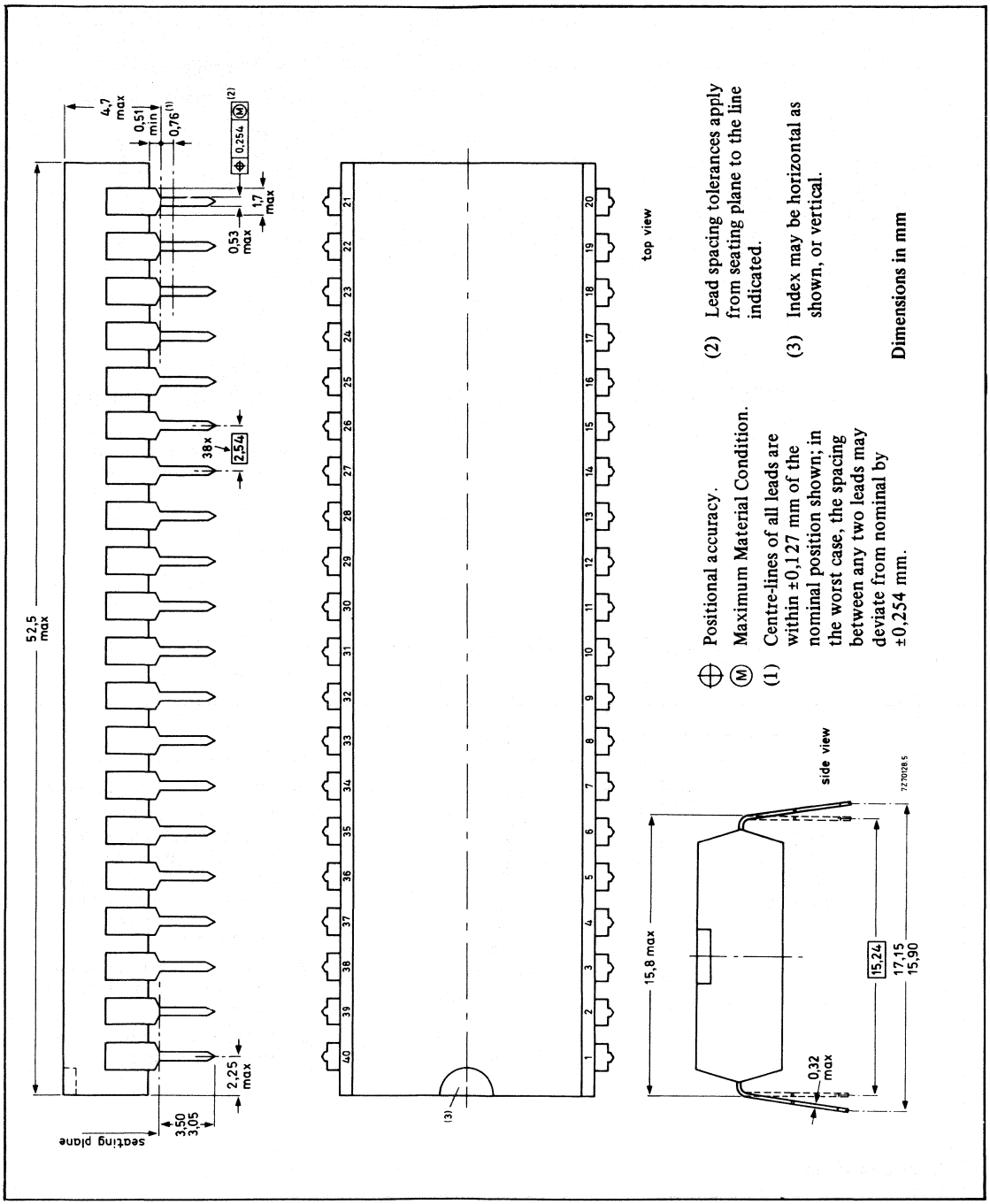
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

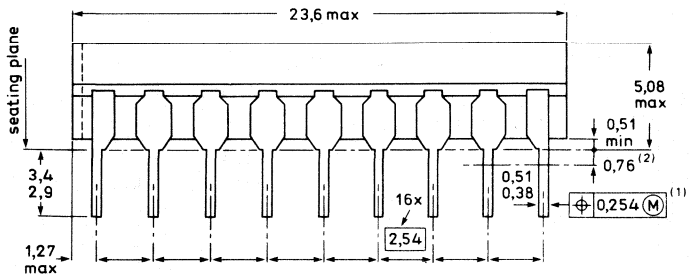
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

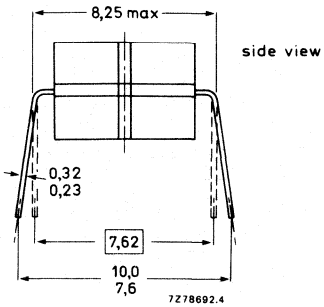
(2) Lead spacing tolerances apply from seating plane to the line indicated.

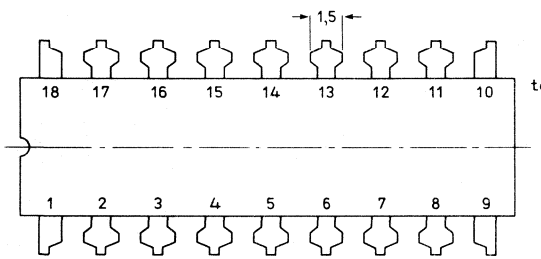
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT133B)







⊕ Positional accuracy.

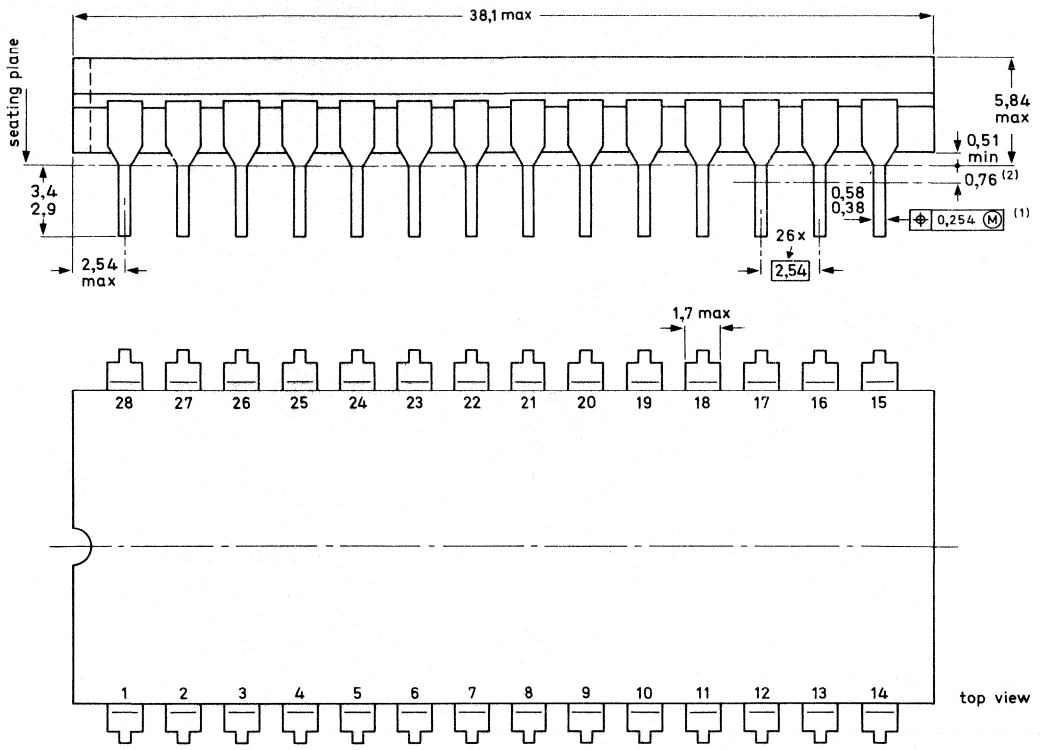
Ⓜ Maximum Material Condition.

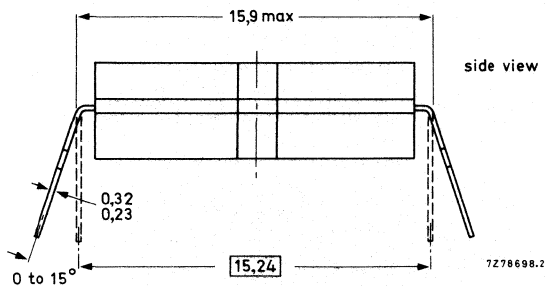
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT135A)





⊕ Positional accuracy.

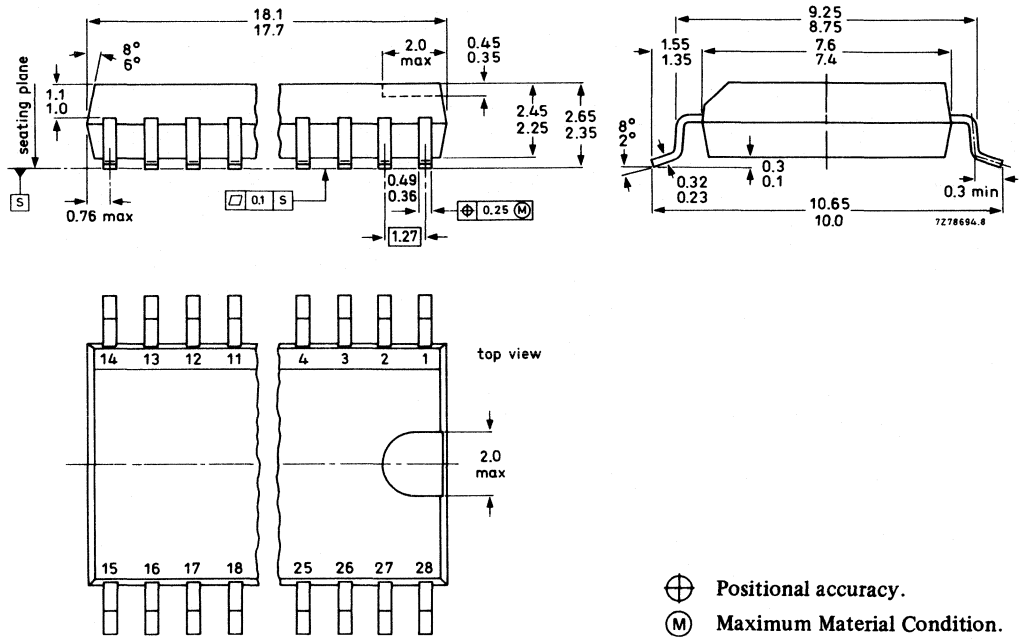
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)

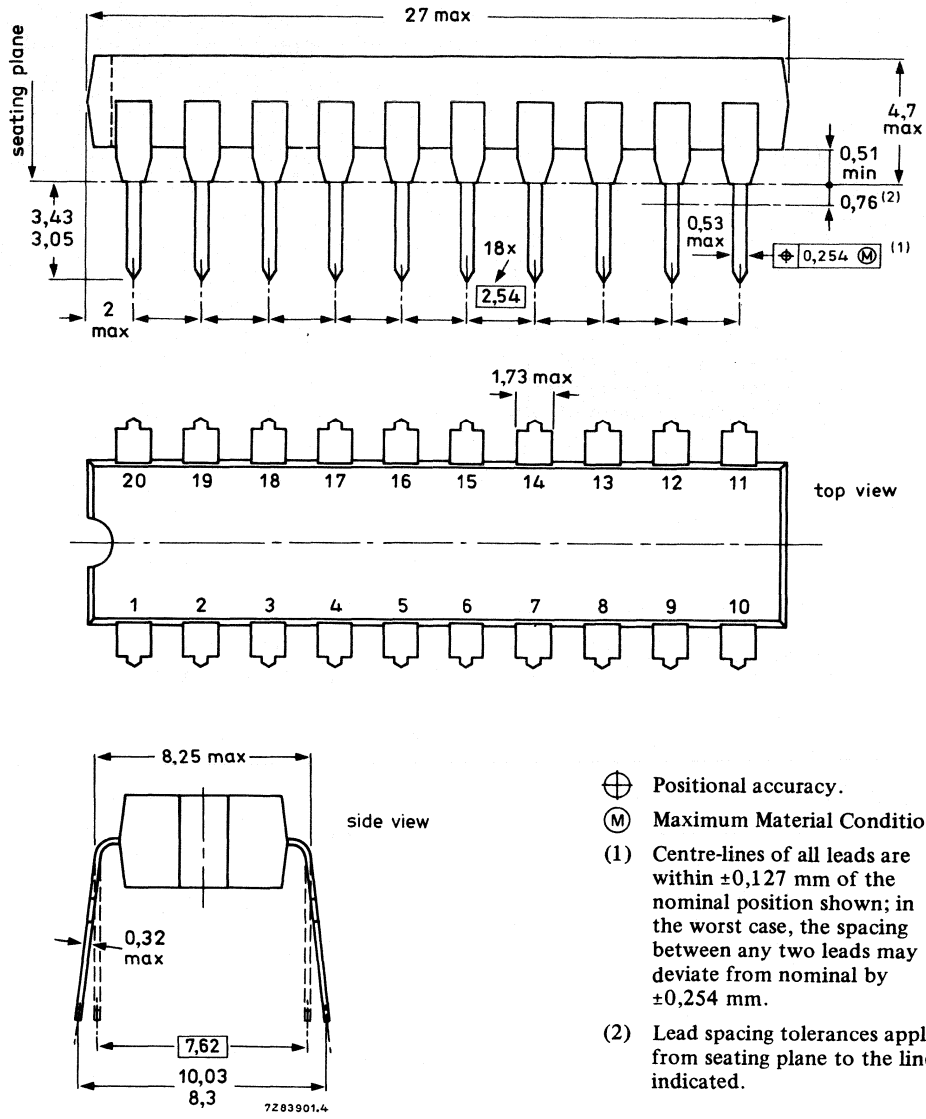


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

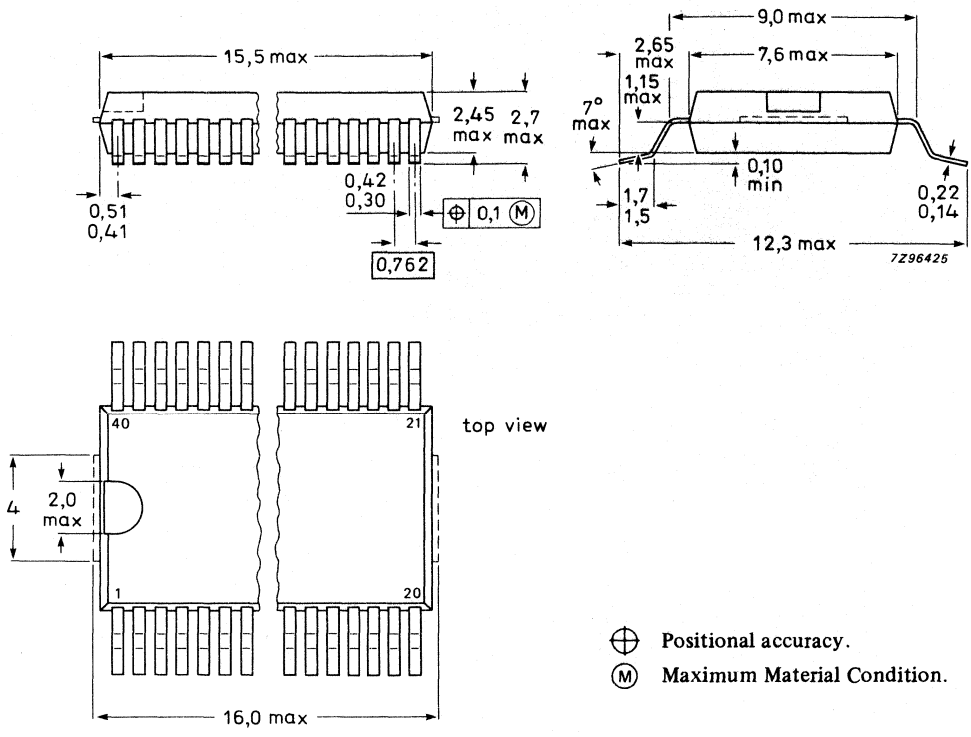
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

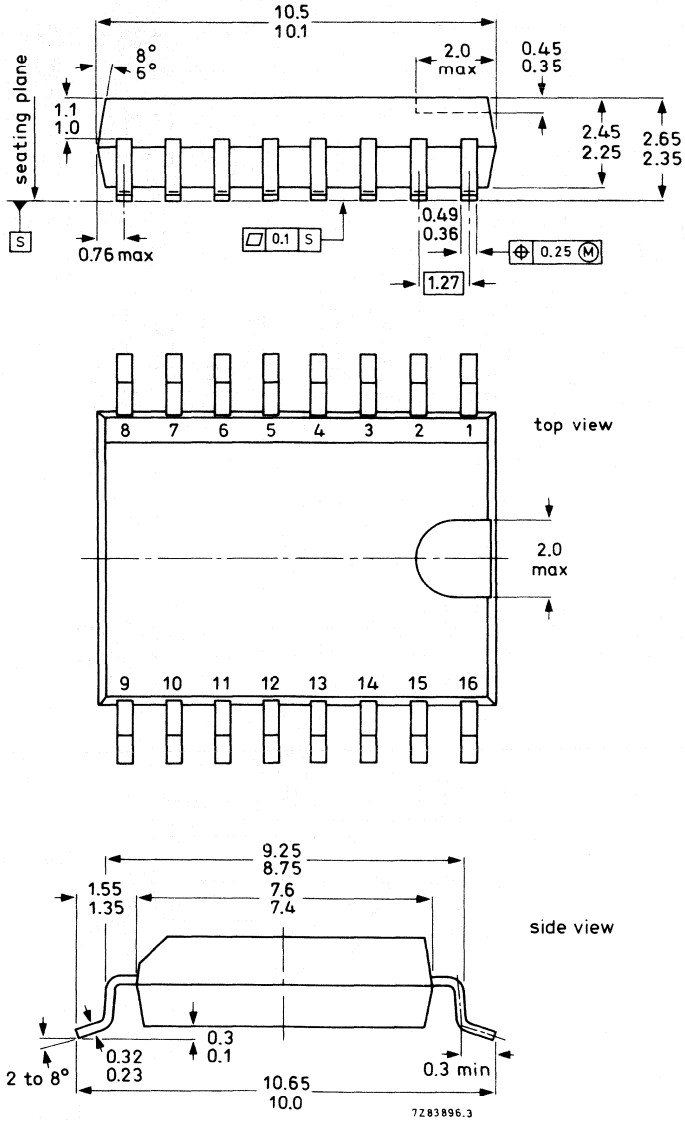
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

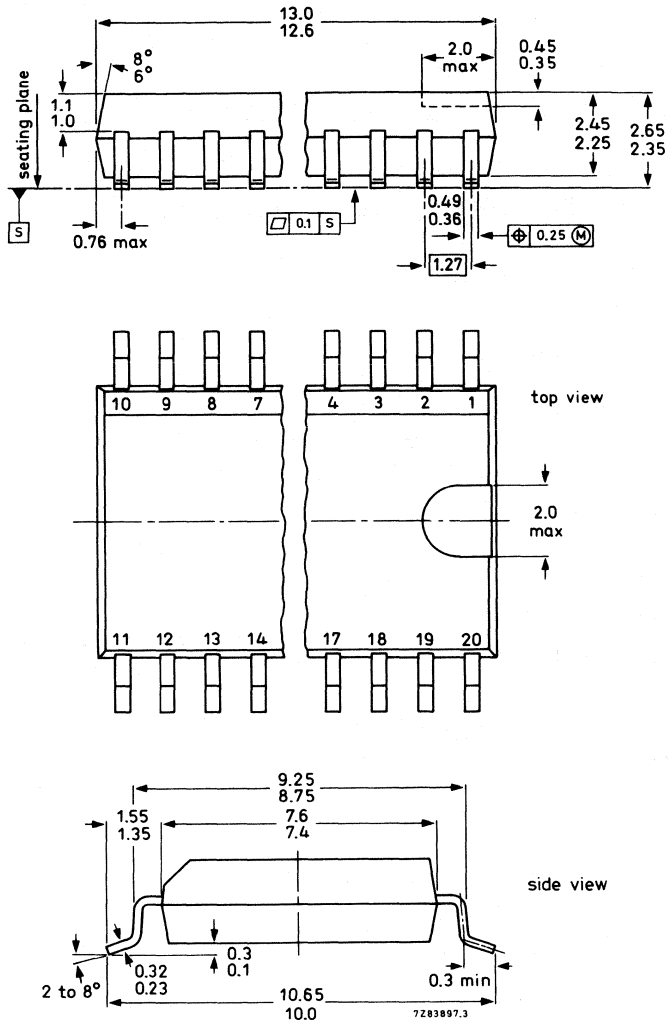


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

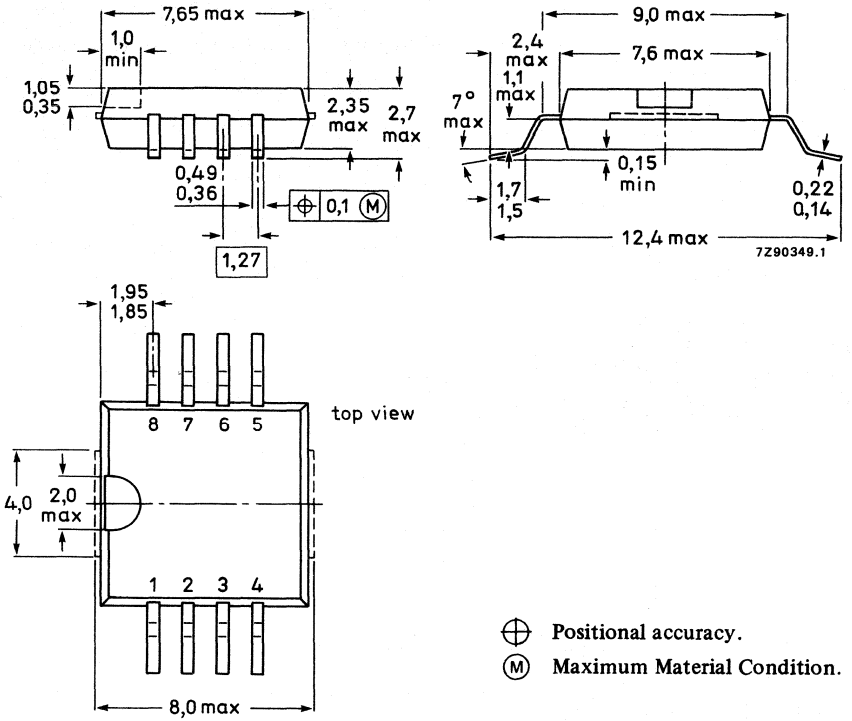


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

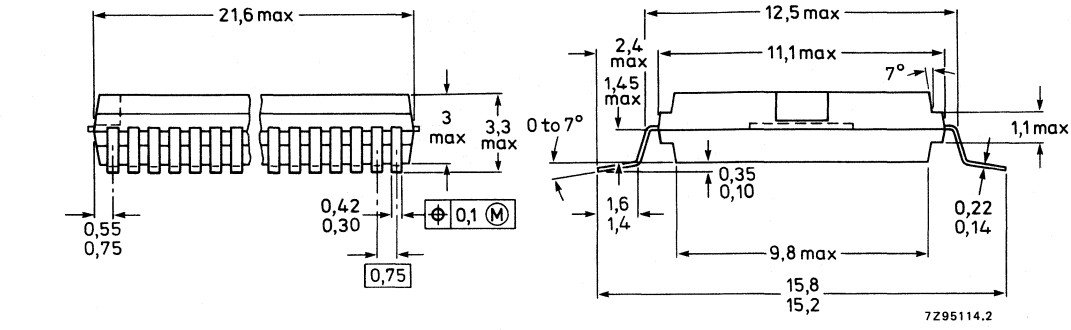
Dimensions in mm

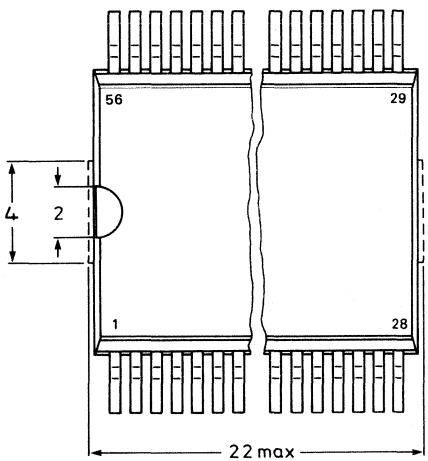
8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176)



Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)





top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

NOTES

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DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 70 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

PROFESSIONAL COMPONENTS*

DISCRETE SEMICONDUCTORS

INTEGRATED CIRCUITS

PASSIVE COMPONENTS**

MATERIALS**

DISPLAY COMPONENTS

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Electron tubes (blue) series of handbooks.
** Will replace the Components and materials (green) series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

T1 **Power tubes for RF heating and communications**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8* **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switched**

T16** **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

* Handbook T8 will be issued in a new series of handbooks (Display Components) and will have the new handbook code DC01.

** Handbook T16 will be re-issued in the future in the new series of handbooks (Display Components).

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

S1 **Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1.5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

SC06 **High-voltage and switching power transistors**

S5 **Small-signal field-effect transistors**

S6 **RF power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optoelectronics, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **PowerMos transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

SC15 **Microwave transistors**

SC17 **Semiconductor sensors**

S14 **Liquid Crystal Displays**

INTEGRATED CIRCUITS

This series of handbooks comprises:

IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05N	**HE4000B logic family – uncased ICs** CMOS
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers and peripherals** Bipolar, MOS
IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

PASSIVE COMPONENTS

This series of handbooks comprises:

current code		new handbook code
C2	Television tuners, coaxial aerial input assemblies	DC01*
C3	Loudspeakers	DC04*
C4	Ferroxcube potcores, square cores and cross cores	MA01**
C5	Ferroxcube for power, audio/video and accelerators	
C7	Variable capacitors	PA04△
C8	Variable mains transformers	PC10△△
C9	Piezoelectric quartz devices	PA07△
C11	Varistors, thermistors and sensors	PA02△
C12	Potentiometers, encoders and switches	PA03△
C13	Fixed resistors	PA08△
C14	Electrolytic capacitors; solid and non-solid	PA01
C15	Ceramic capacitors	PA06△
C16	Permanent magnet materials	MA02**
C19	Piezoelectric ceramics	MA03**
C20	Wire-wound components for TVs and monitors	DC05*
C22	Film capacitors	PA05△

* These handbooks will be re-issued in the future in the new series of handbooks (Display Components).

** These handbooks will be re-issued in the future in the new series of handbooks (Materials).

△ These handbooks will be re-issued in the future in the new series of handbooks (Passive Components).

△△ These handbooks will be re-issued in the future in the new series of handbooks (Professional Components).

MATERIALS

This series of handbooks comprises:

MA01* **Ferrites (the current issue are handbooks C4 and C5)**

MA02* **Permanent magnet materials**

MA03* **Piezoelectric ceramics**

* Not yet issued in the Materials series of handbooks.

DISPLAY COMPONENTS

This series of handbooks comprises:

DC01 **Colour display systems**

DC02* **Monochrome tubes and deflection units**

DC03* **Television tuners, coaxial aerial input assemblies**

DC04* **Loudspeakers**

DC05* **Wire-wound components for TVs and monitors**

* Not yet issued in the Display Components series of handbooks.

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